

MOSFET – N-Channel, POWERTRENCH®

60 V, 300 A, 1.1 mΩ

FDBL86561-F085

Features

- Typical $R_{DS(on)}$ = 0.85 mΩ at $V_{GS} = 10$ V, $I_D = 80$ A
- Typical $Q_{g(tot)}$ = 170 nC at $V_{GS} = 10$ V, $I_D = 80$ A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

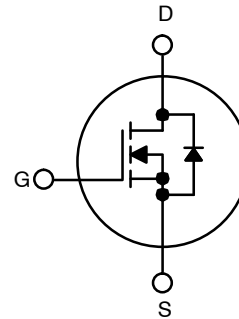
- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS ($T_J = 25$ °C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current – Continuous ($V_{GS} = 10$), $T_C = 25$ °C (Note 1)	300	A
	Pulsed Drain Current, $T_C = 25$ °C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	1167	mJ
P_D	Power Dissipation	429	W
	Derate Above 25 °C	2.86	
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.35	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction-to-Ambient (Note 3)	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25$ °C, $L = 0.57$ mH, $I_{AS} = 64$ A, $V_{DD} = 40$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

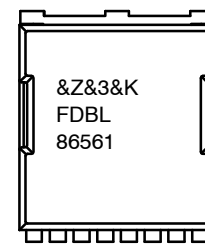


N-Channel



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86561	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDBL86561-F085	H-PSOF8L	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

FDBL86561–F085

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	60			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		1	μA
			$T_J = 175\text{ }^\circ\text{C}$ (Note 4)		3	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain-to-Source on Resistance	$I_D = 80\text{ A}$, $V_{GS} = 10\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$	0.85	1.1	$\text{m}\Omega$
			$T_J = 175\text{ }^\circ\text{C}$ (Note 4)	1.5	2.2	$\text{m}\Omega$

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		13650		pF
C_{oss}	Output Capacitance			3375		pF
C_{rss}	Reverse Transfer Capacitance			255		pF
R_g	Gate Resistance	$f = 1\text{ MHz}$		2.3		Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	$V_{GS} = 0$ to 10 V	$V_{DD} = 48\text{ V}$ $I_D = 80\text{ A}$	170	220	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2 V		24	32	nC
Q_{gs}	Gate-to-Source Gate Charge			56		nC
Q_{gd}	Gate-to-Drain "Miller" Charge			24		nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 30\text{ V}$, $I_D = 80\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$			137	ns
$t_{d(on)}$	Turn-On Delay			45		ns
t_r	Rise Time			61		ns
$t_{d(off)}$	Turn-Off Delay			80		ns
t_f	Fall Time			41		ns
t_{off}	Turn-Off Time				156	ns

DRAIN-SOURCE DIODE CHARACTERISTIC

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0\text{ V}$			1.25	V
		$I_{SD} = 40\text{ A}$, $V_{GS} = 0\text{ V}$			1.2	V
t_{rr}	Reverse-Recovery Time	$I_F = 80\text{ A}$, $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 48\text{ V}$		107	139	ns
Q_{rr}	Reverse-Recovery Charge			183	265	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175\text{ }^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

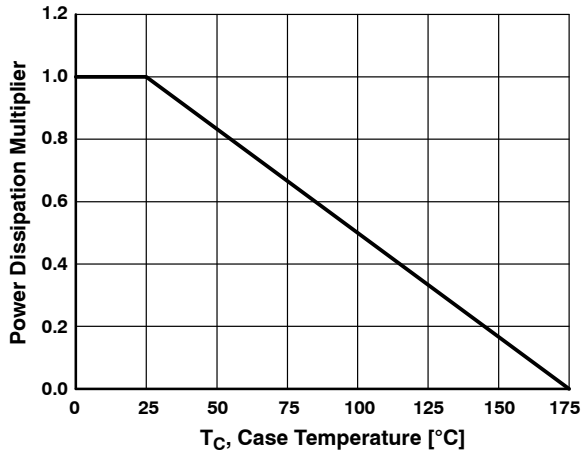


Figure 1. Normalized Power Dissipation vs. Case Temperature

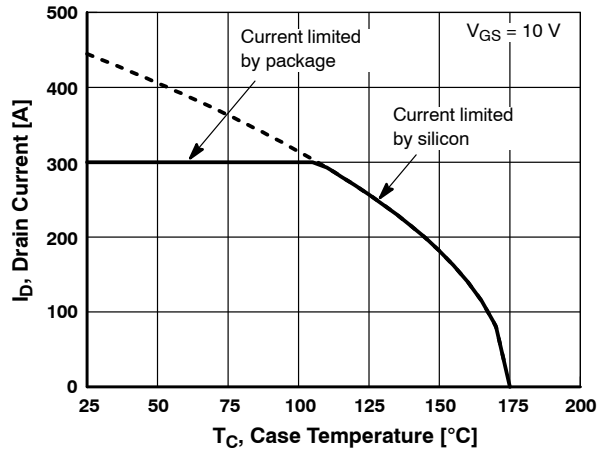


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

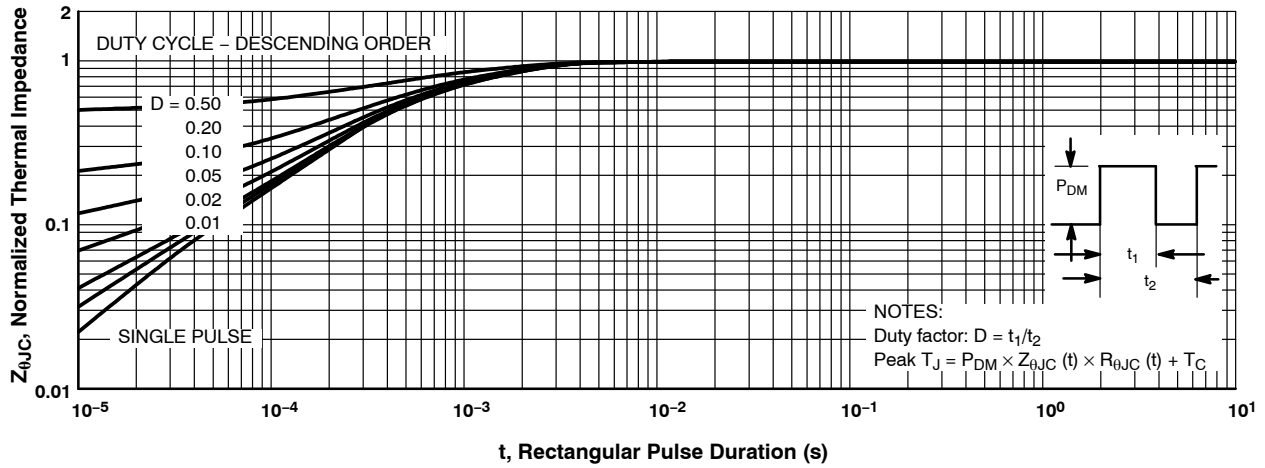


Figure 3. Normalized Maximum Transient Thermal Impedance

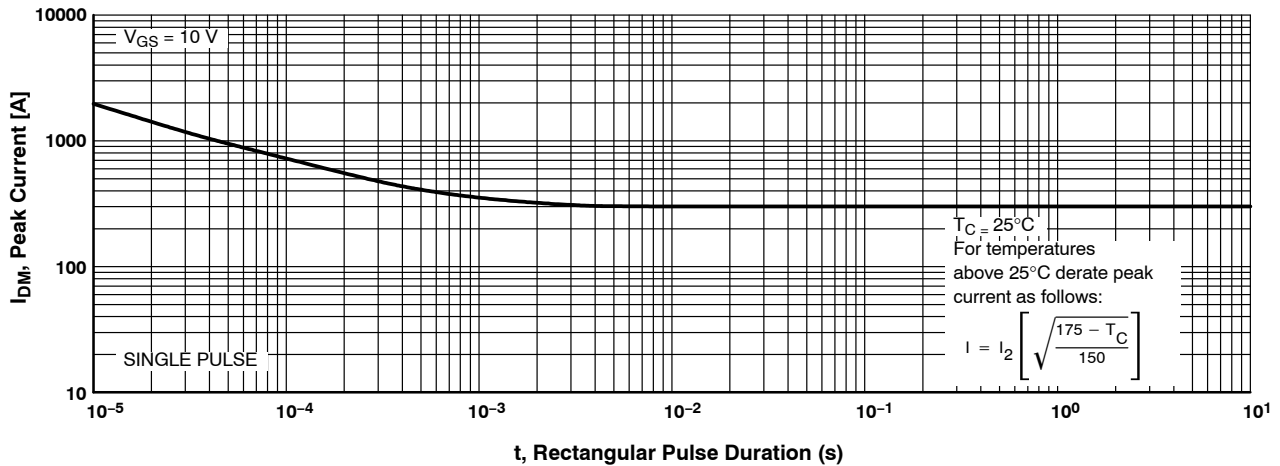


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

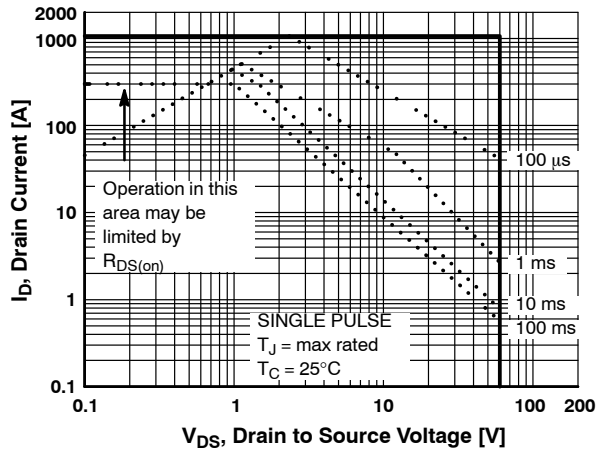


Figure 5. Forward Bias Safe Operating Area

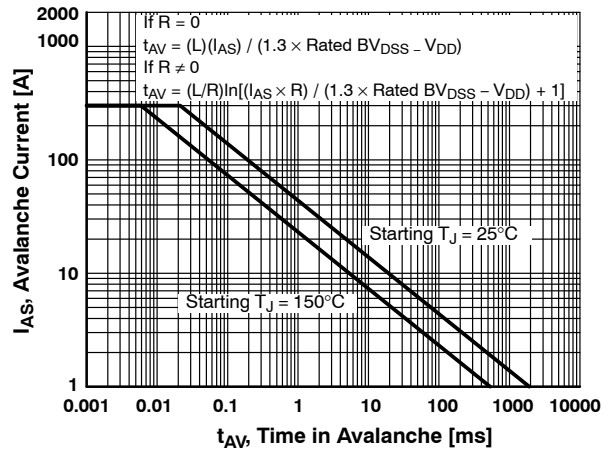


Figure 6. Unclamped Inductive Switching Capability
Refer to onsemi Application Notes AN7514 and AN7515.

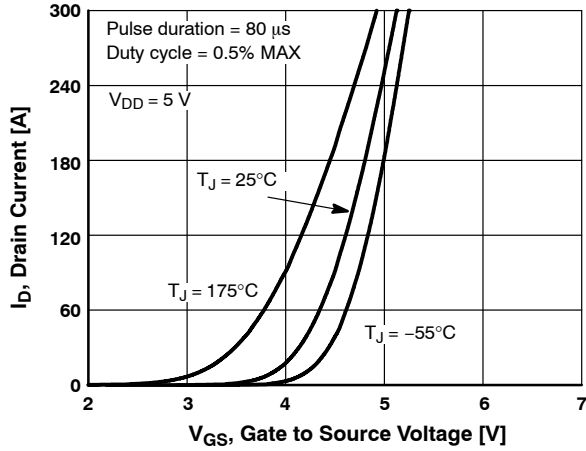


Figure 7. Transfer Characteristics

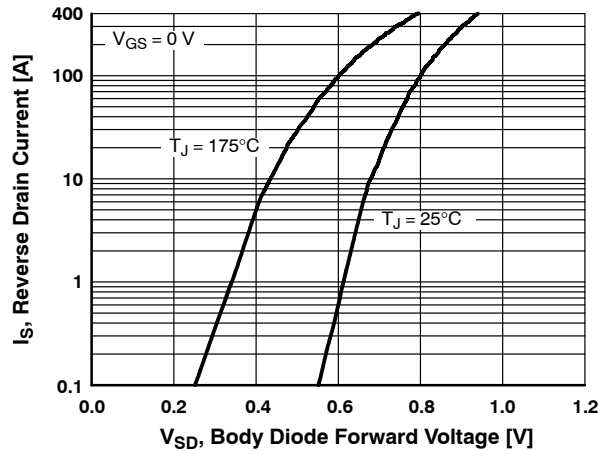


Figure 8. Forward Diode Characteristics

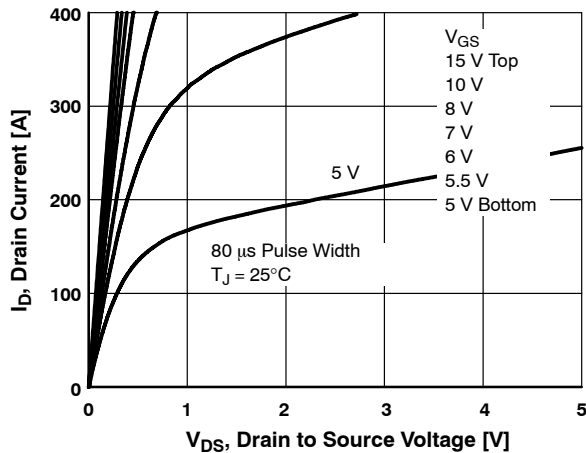


Figure 9. Saturation Characteristics

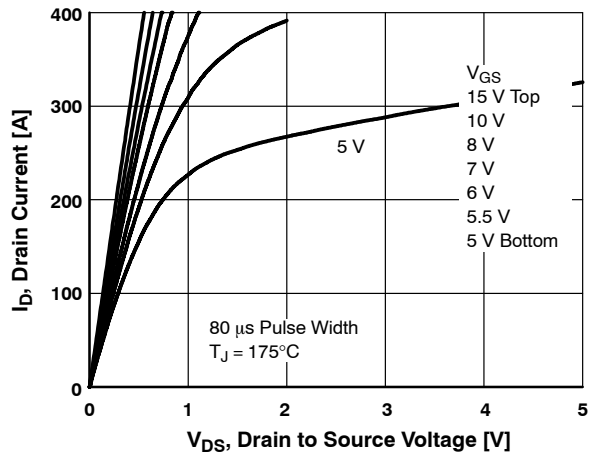


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

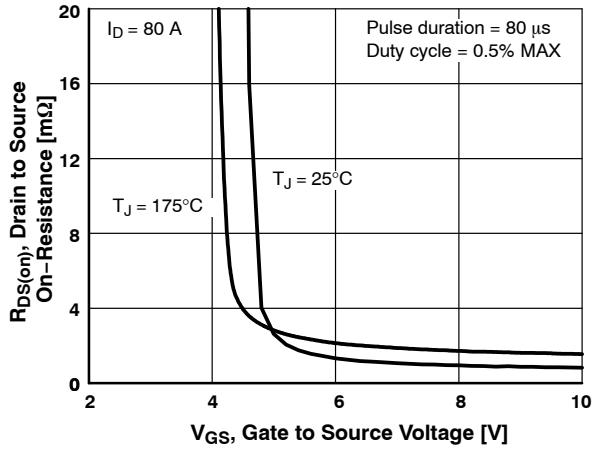


Figure 11. $R_{DS(ON)}$ vs. Gate Voltage

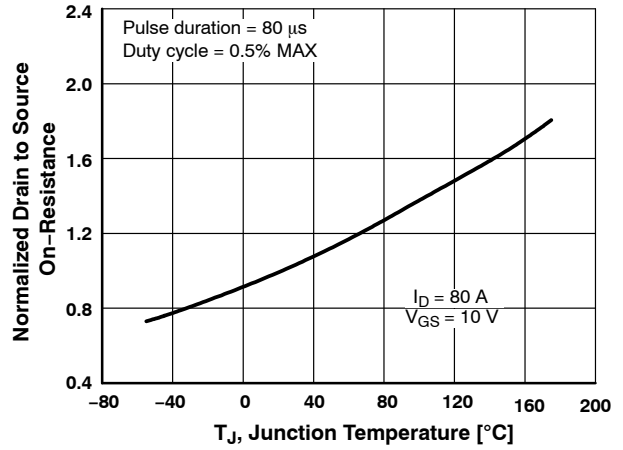


Figure 12. Normalized $R_{DS(ON)}$ vs. Junction Temperature

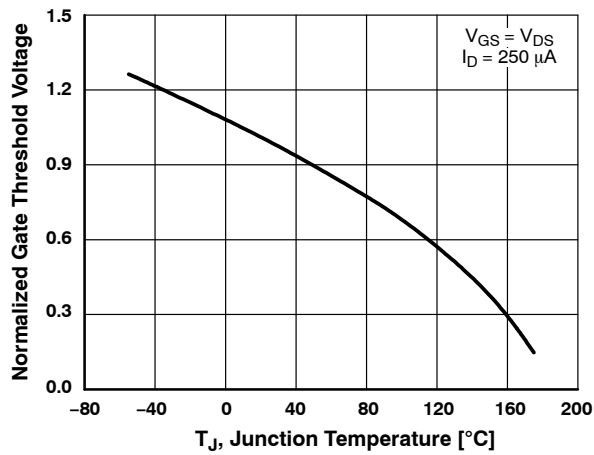


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

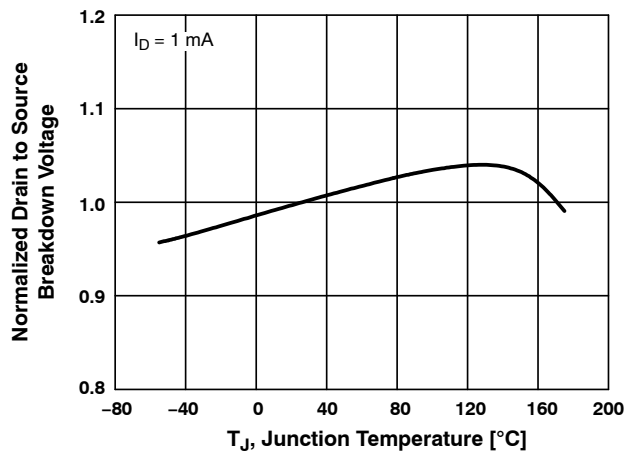


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

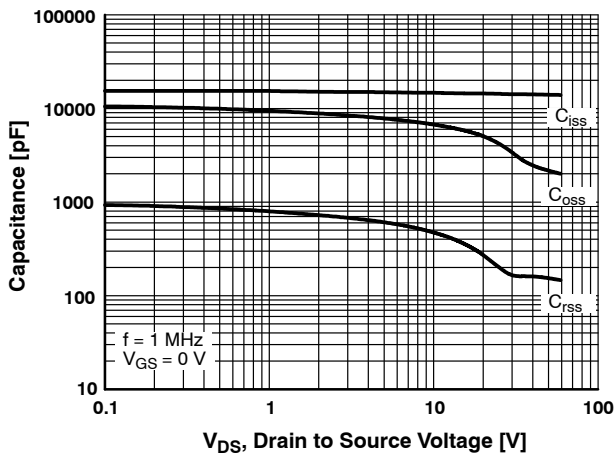


Figure 15. Capacitance vs. Drain to Source Voltage

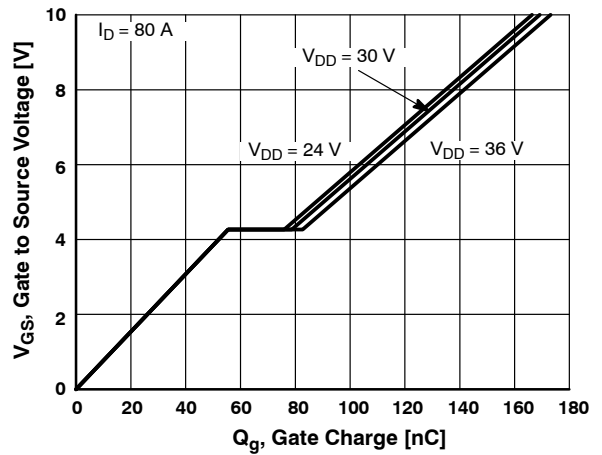


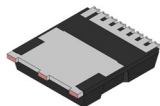
Figure 16. Gate Charge vs. Gate to Source Voltage

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REVISION HISTORY

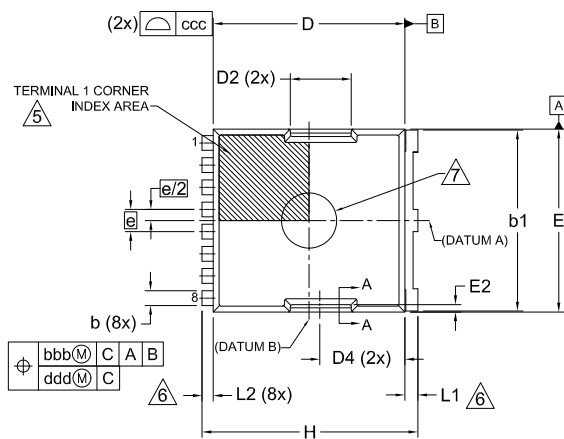
Revision	Description of Changes	Date
5	Add pinout information to page 1	12/2/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

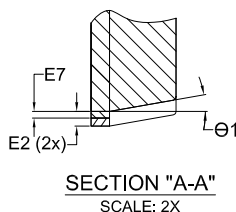


H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

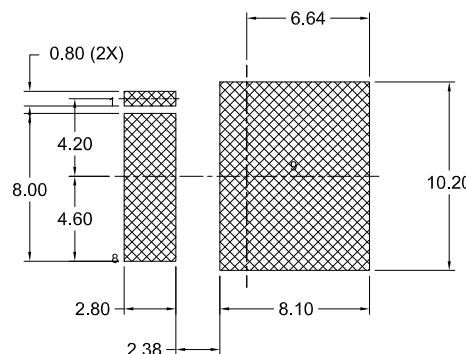
DATE 30 JUL 2024



TOP VIEW

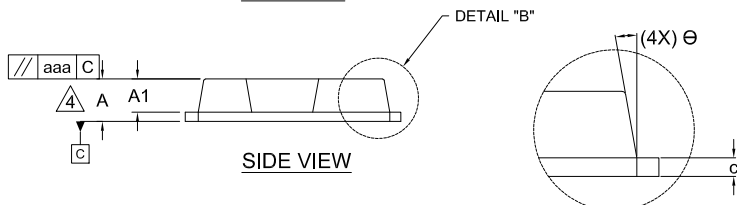


SECTION "A-A"
SCALE: 2X



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

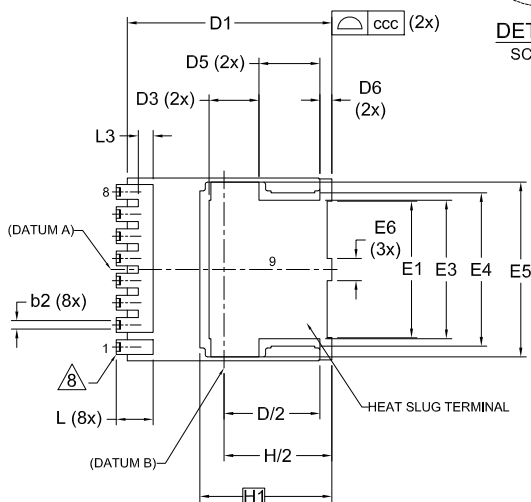


SIDE VIEW

DETAIL "B"
SCALE: 2X

NOTES:

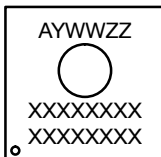
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.



BOTTOM VIEW

GENERIC
MARKING DIAGRAM*

- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	10° REF		
theta 1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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DESCRIPTION:	H-PSOF8L 11.68x9.80x2.30, 1.20P	PAGE 1 OF 1

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