

MOSFET – N-Channel, SUPERFET II, FRFET 600 V, 37 A, 104 mΩ

FCH104N60F-F085

Description

SUPERFET[®] II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently SUPERFET II is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.

SUPERFET II FRFET[®] MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

Features

- Typical $R_{DS(on)}$ = 91 mΩ at V_{GS} = 10 V, I_D = 18.5 A
- Typical $Q_{g(tot)}$ = 109 nC at V_{GS} = 10 V, I_D = 18.5 A
- UIS Capability
- Qualified to AEC Q101 and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

Applications

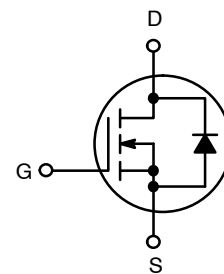
- Automotive On Board Charger
- Automotive DC/DC Converter for HEV



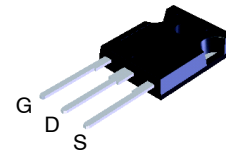
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V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
600 V	104 mΩ	37 A

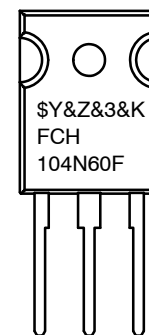


N-Channel MOSFET



**TO-247
CASE 340CK**

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot Code
FCH104N60F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH104N60F–F085

MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain to Source Voltage	600	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current – Continuous (V _{GS} = 10) (Note 1)	T _C = 25°C T _C = 100°C	A
	Pulsed Drain Current	See Fig. 4	
E _{AS}	Single Pulsed Avalanche Rating (Note 2)	809	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P _D	Power Dissipation	357	W
	Derate Above 25°C	2.85	W/°C
T _J , T _{STG}	Operating and Storage Temperature	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 35 mH, I_{AS} = 6.8 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. I_{SD} ≤ 18.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 380 V, starting T_J = 25°C.
4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJC}	Maximum Thermal Resistance, Junction to Case	0.35	°C/W
R _{θJA}	Maximum Thermal Resistance, Junction to Ambient	40	

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FCH104N60F–F085	FCH104N60F	TO–247	–	–	30

FCH104N60F–F085

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	600	–	–	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 600 V, V _{GS} = 0 V, T _J = 25°C	–	–	10	μA
		V _{DS} = 600 V, V _{GS} = 0 V, T _J = 150°C (Note 5)	–	–	1	mA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	3	4	5	V
r _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10 V, I _D = 18.5 A, T _J = 25°C	–	91	104	mΩ
		V _{GS} = 10 V, I _D = 18.5 A, T _J = 150°C (Note 5)	–	217	275	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	–	4302	–	pF
C _{oss}	Output Capacitance		–	134	–	pF
C _{rss}	Reverse Transfer Capacitance		–	1.7	–	pF
R _g	Gate Resistance	f = 1 MHz	–	0.49	–	Ω
Q _{g(TOT)}	Total Gate Charge	V _{DD} = 380 V, I _D = 18.5 A, V _{GS} = 10 V	–	109	139	nC
Q _{g(th)}	Threshold Gate Charge		–	8	11	nC
Q _{gs}	Gate to Source Gate Charge		–	23	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	46	–	nC

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 380 V, I _D = 18.5 A, V _{GS} = 10 V, R _G = 4.7 Ω	–	58	78	ns
t _{d(on)}	Turn-On Delay Time		–	35	–	ns
t _r	Rise Time		–	23	–	ns
t _{d(off)}	Turn-Off Delay Time		–	94	–	ns
t _f	Fall Time		–	5	–	ns
t _{off}	Turn-Off Time		–	98	131	ns

DRAIN–SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 18.5 A, V _{GS} = 0 V	–	–	1.2	V
T _{rr}	Reverse Recovery Time	I _F = 18.5 A, dI _{SD} /dt = 100 A/μs V _{DD} = 480 V	–	162	–	ns
Q _{rr}	Reverse Recovery Charge		–	1223	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

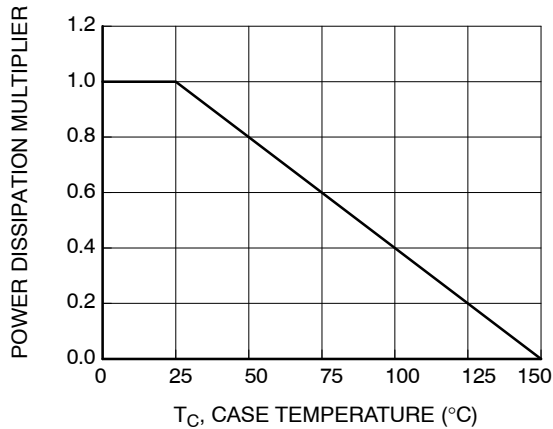


Figure 1. Normalized Power Dissipation vs. Case Temperature

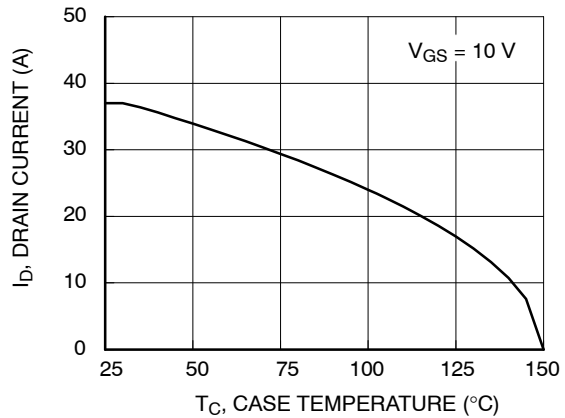


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

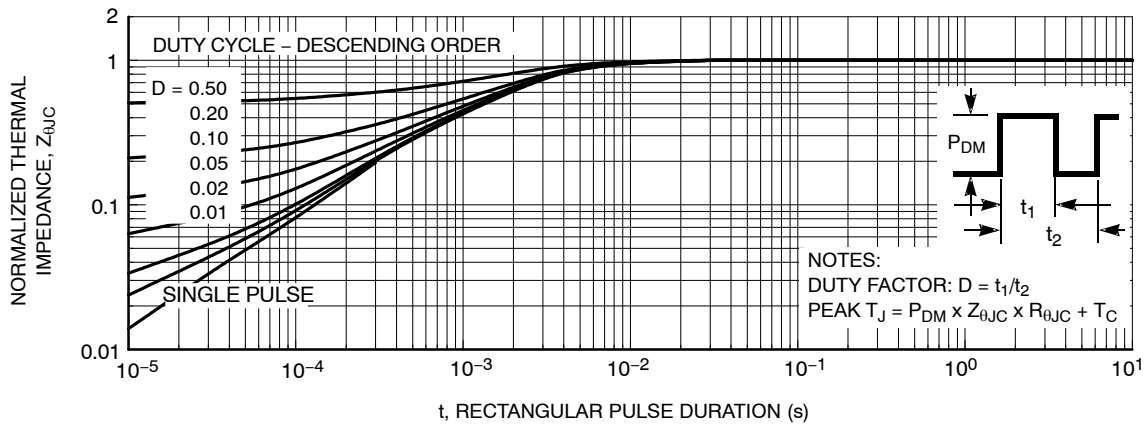


Figure 3. Normalized Maximum Transient Thermal Impedance

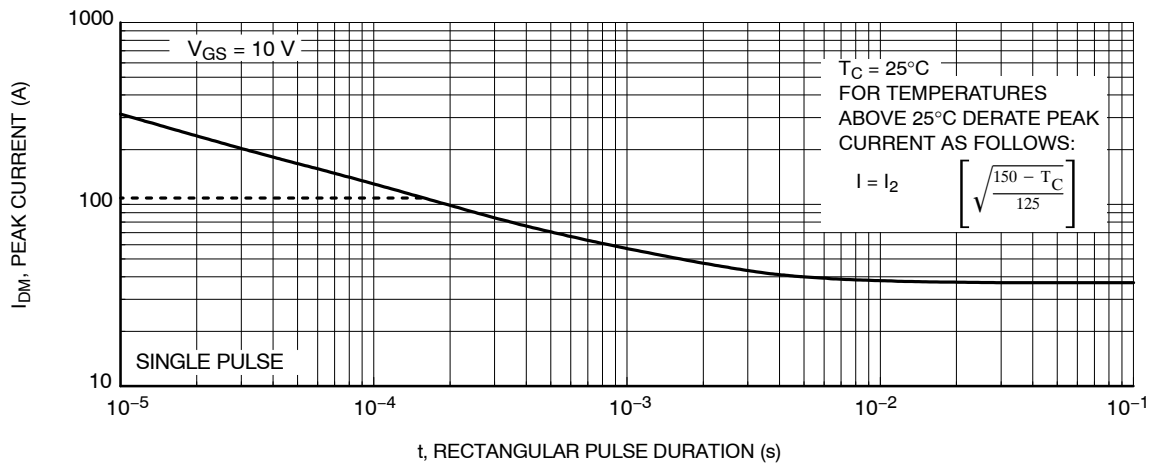


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

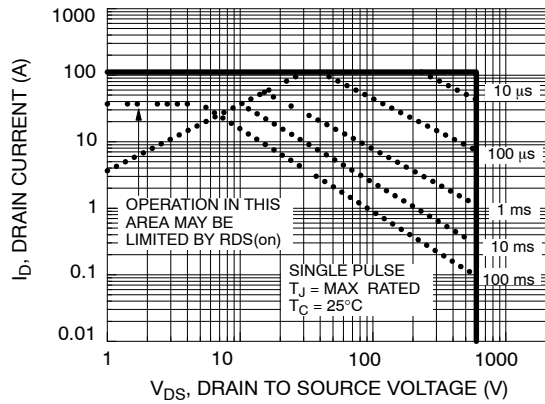


Figure 5. Forward Bias Safe Operating Area

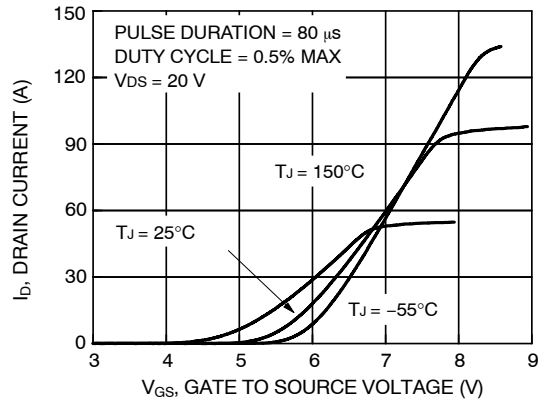


Figure 6. Transfer Characteristics

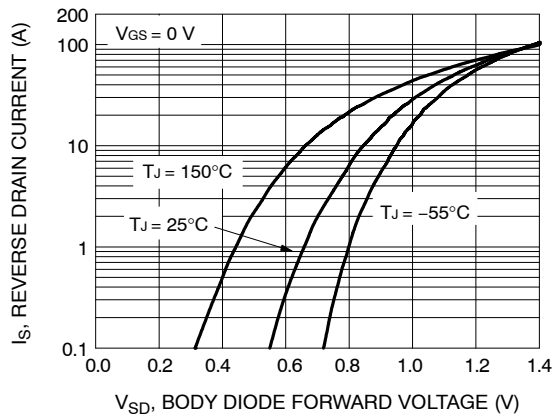


Figure 7. Forward Diode Characteristics

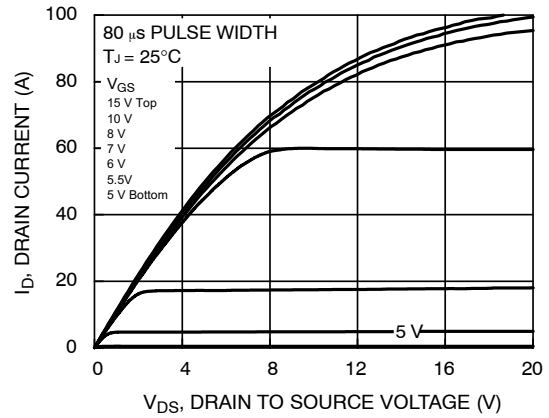


Figure 8. Forward Diode Characteristics

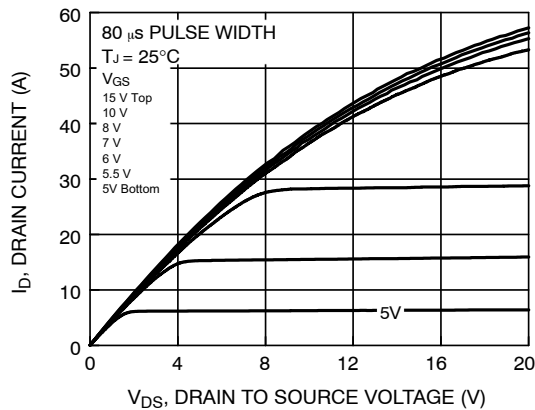


Figure 9. Saturation Characteristics

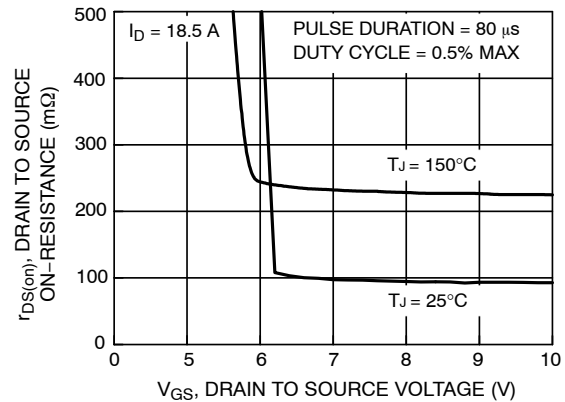


Figure 10. $R_{DS(on)}$ vs. Gate Voltage

TYPICAL CHARACTERISTICS (continued)

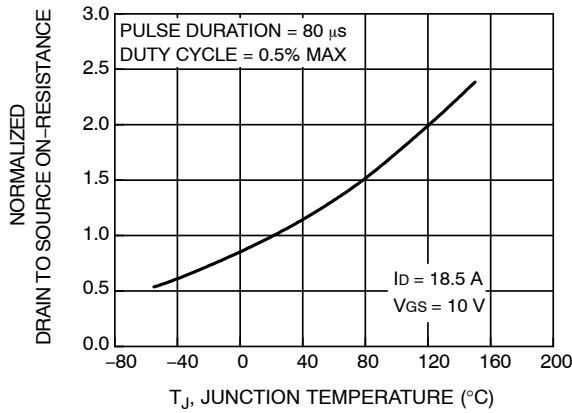


Figure 11. Normalized $R_{DS(on)}$ vs. Junction Temperature

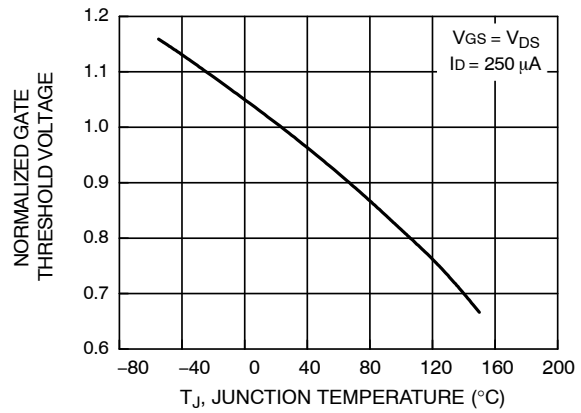


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

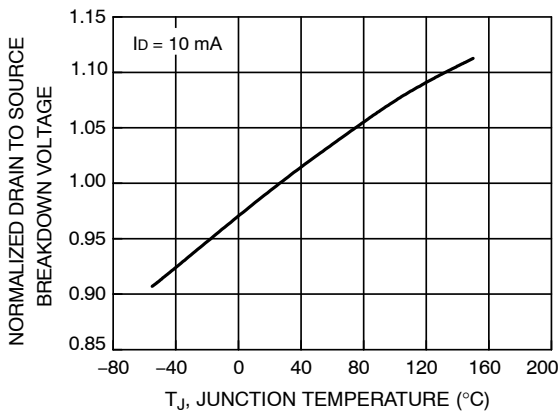


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

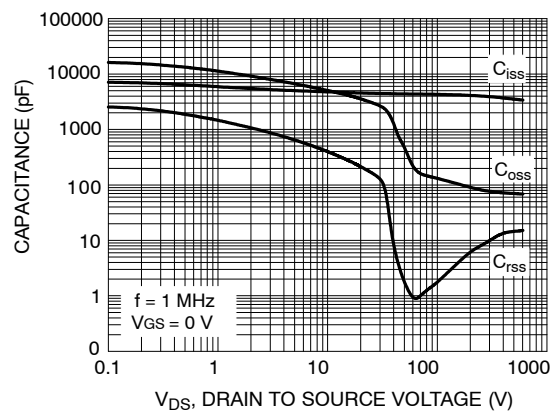


Figure 14. Capacitance vs. Drain to Source Voltage

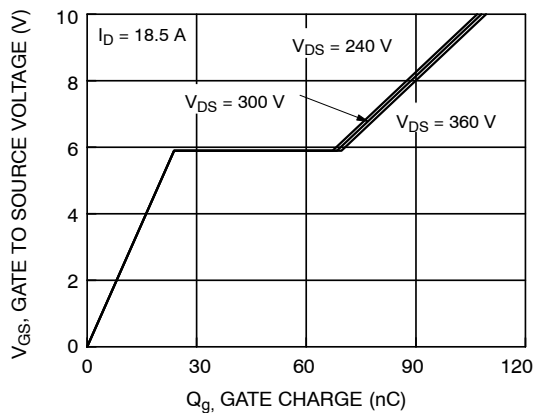


Figure 15. Gate Charge vs. Gate to Source Voltage

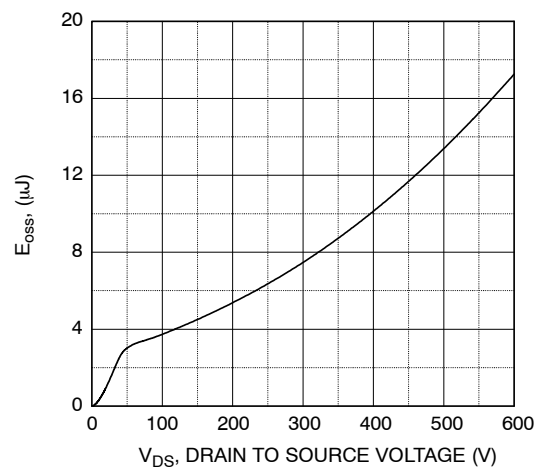


Figure 16. E_{oss} vs. Drain to Source Voltage

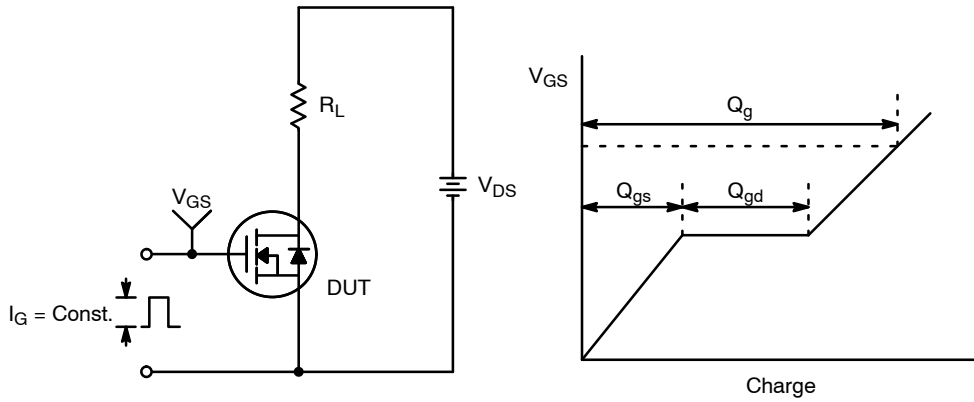


Figure 17. Gate Charge Test Circuit & Waveform

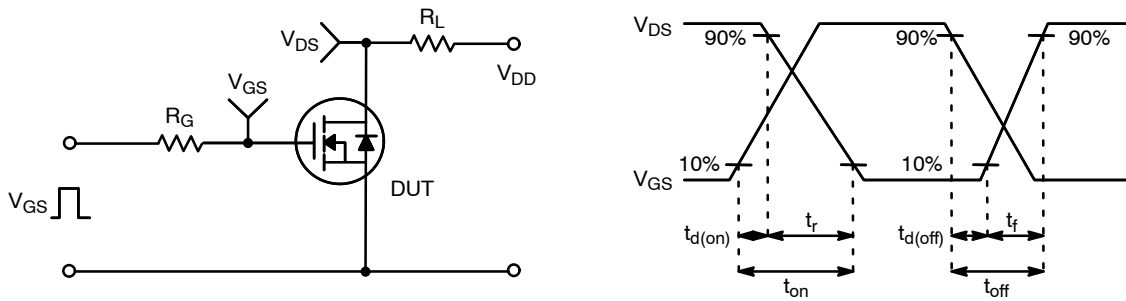


Figure 18. Resistive Switching Test Circuit & Waveforms

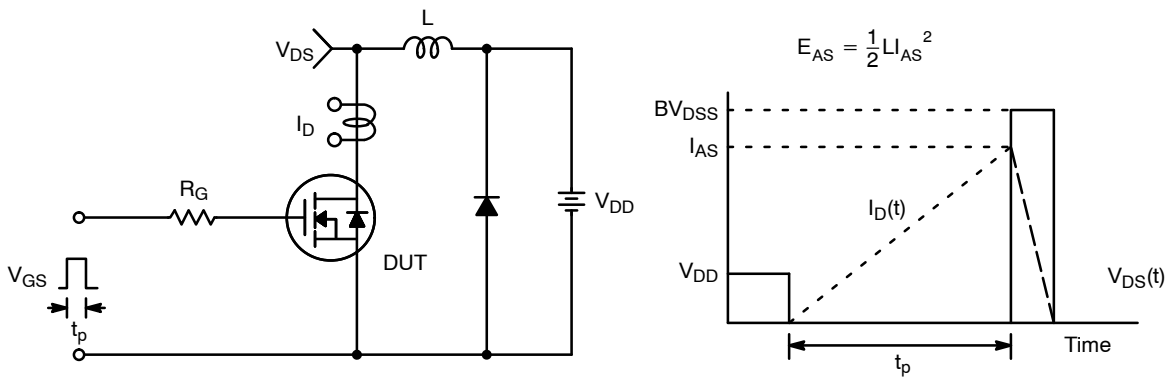


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

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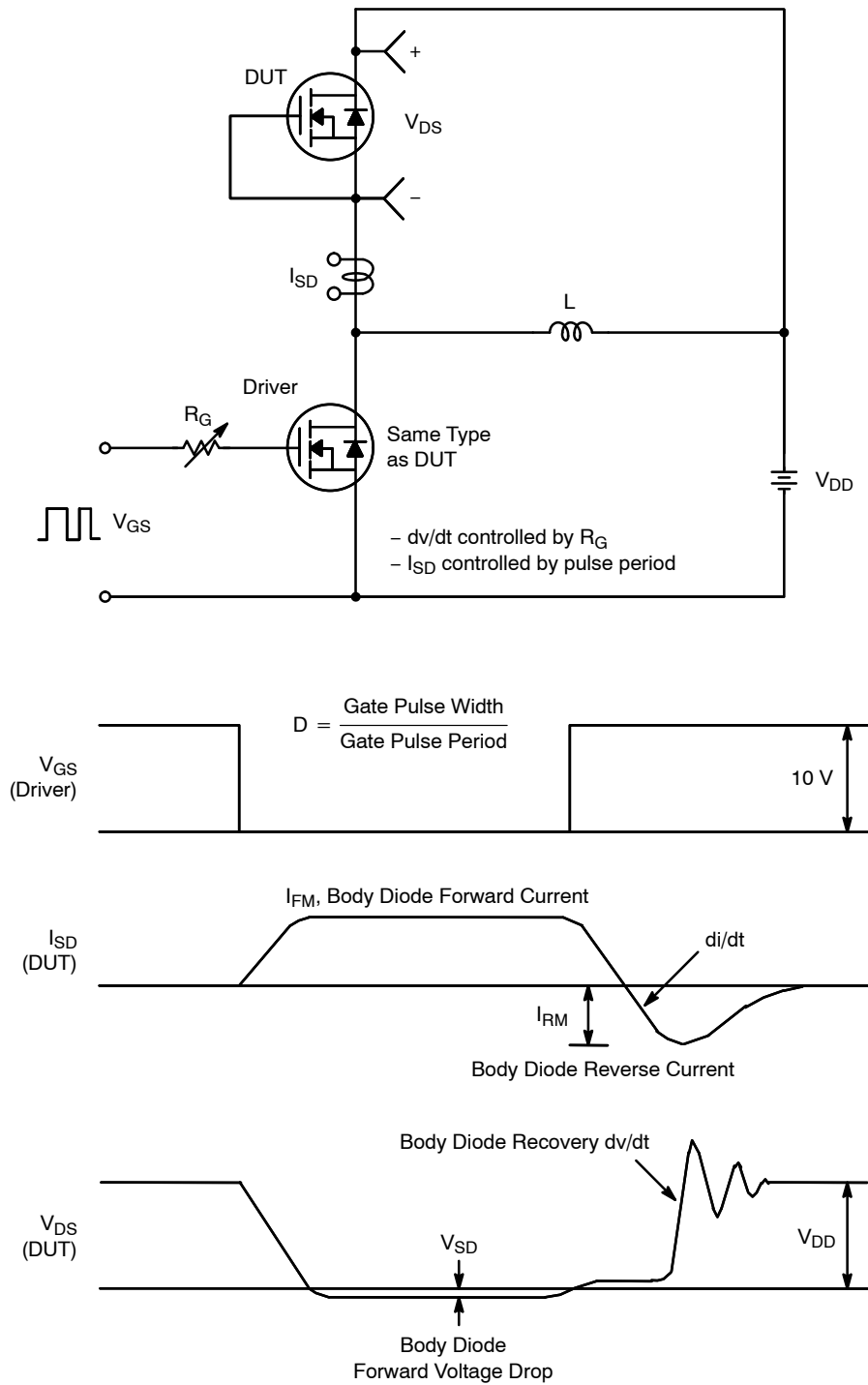
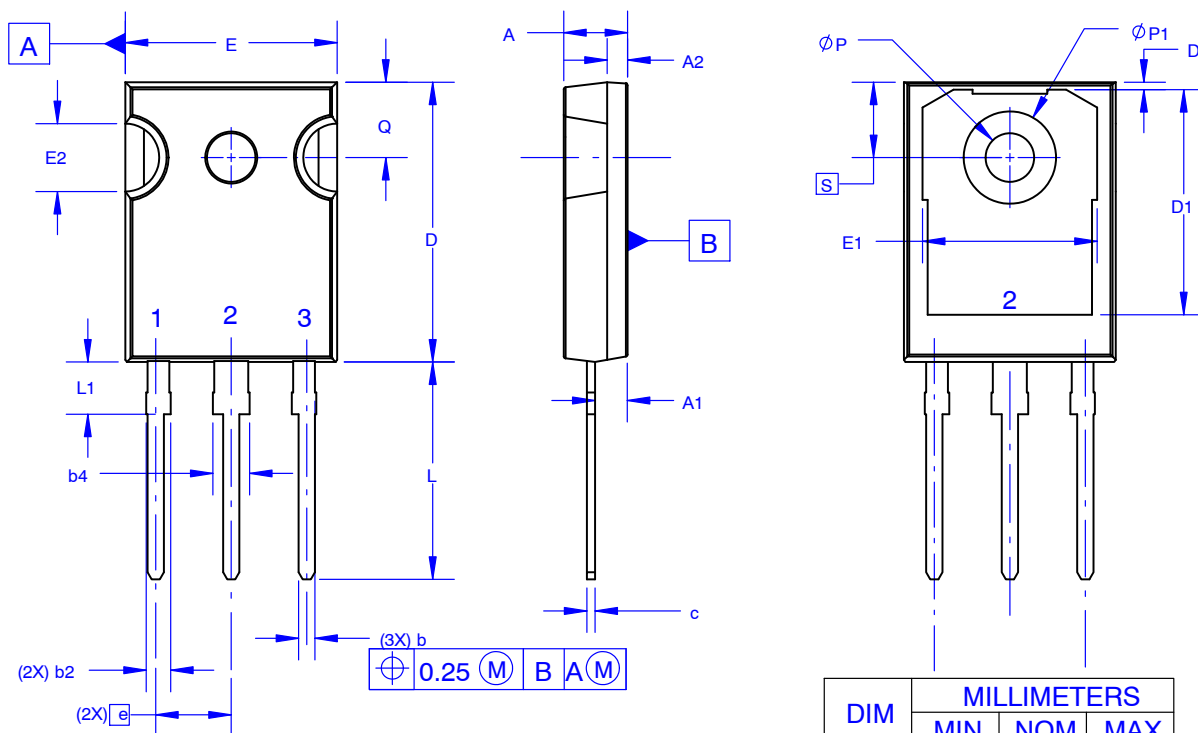


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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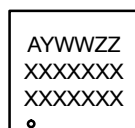
TO-247-3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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