

# MOSFET – N-Channel, SUPERFET<sup>®</sup> II, FRFET<sup>®</sup>

**650 V, 41 mΩ, 76 A**

## FCH041N65F-F085

### Description

SuperFET II Mosfet is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.

SuperFET II FRFET MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

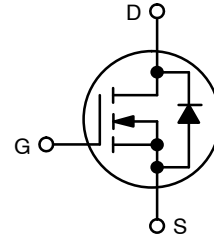
### Features

- Typ.  $R_{DS(on)}$  = 34 mΩ at  $V_{GS} = 10$  V,  $I_D = 38$  A
- Typ.  $Q_{g(tot)}$  = 234 nC at  $V_{GS} = 10$  V,  $I_D = 38$  A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

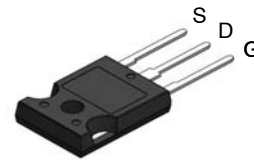
### Applications

- Automotive On Board Charger
- Automotive DC-DC Converter for HEV

$V_{DS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
650 V	41 mΩ @ 10 V	76 A

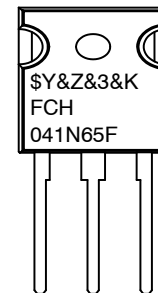


**N-CHANNEL MOSFET**



**TO-247-3LD  
CASE 340CK**

### MARKING DIAGRAM



- \$Y = onsemi Logo
- &Z = Assembly Plant Code
- &3 = Numeric Date Code
- &K = Lot Code
- FCH041N65F = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# FCH041N65F-F085

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	650	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous ( $V_{GS} = 10$ ) (Note 1)	$T_C = 25\text{ }^\circ\text{C}$	76 A
		$T_C = 100\text{ }^\circ\text{C}$	48 A
	Pulsed Drain Current	See Fig. 4	A
$E_{AS}$	Single Pulsed Avalanche Rating (Note 2)	2025	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
$P_D$	Power Dissipation	595	W
	Derate Above $25\text{ }^\circ\text{C}$	4.76	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2.  $I_{AS} = 15\text{ A}$ ,  $R_G = 25\ \Omega$ , starting  $T_J = 25\text{ }^\circ\text{C}$ .

3.  $I_{SD} \leq 38\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 380\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ .

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.21	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. (Note 4)	40	

4.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2 oz copper.

# FCH041N65F-F085

## ELECTRICAL CHARACTERISTICS ( $T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain-to-Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	650	-	-	V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (Note 5)	-	-	1	$\text{mA}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	$\text{nA}$

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	3	-	5	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$I_D = 38\text{ A}$ , $V_{GS} = 10\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$	-	34	41	$\text{m}\Omega$
		$I_D = 38\text{ A}$ , $V_{GS} = 10\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (Note 5)	-	80	96	

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	-	10200	13566	$\text{pF}$
$C_{oss}$	Output Capacitance		-	10529	14004	
$C_{rss}$	Reverse Transfer Capacitance		-	227	-	
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 520\text{ V}$ , $V_{GS} = 0\text{ V}$	-	843	-	$\text{pF}$
$R_g$	Gate Resistance	$f = 1\text{ MHz}$	-	0.5	2.18	$\Omega$
$Q_{g(tot)}$	Total Gate Charge	$V_{DD} = 380\text{ V}$ , $I_D = 38\text{ A}$ , $V_{GS} = 10\text{ V}$	-	234	304	$\text{nC}$
$Q_{g(th)}$	Threshold Gate Charge		-	17	22	
$Q_{gs}$	Gate-to-Source Gate Charge		-	50	-	
$Q_{gd}$	Gate-to-Drain "Miller" Charge		-	90	-	

### SWITCHING CHARACTERISTICS

$t_{on}$	Turn-On Time	$V_{DD} = 380\text{ V}$ , $I_D = 38\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_G = 4.7\text{ }\Omega$	-	94	207	$\text{ns}$
$t_{d(on)}$	Turn-On Delay Time		-	55	-	
$t_r$	Turn-On Rise Time		-	39	-	
$t_{d(off)}$	Turn-Off Delay Time		-	183	-	
$t_f$	Turn-Off Fall Time		-	8	-	
$t_{off}$	Turn-Off Time		-	191	402	

### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source-to-Drain Diode Voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 38\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{DD} = 480\text{ V}$ , $I_F = 38\text{ A}$ , $di_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	235	-	$\text{ns}$
$Q_{rr}$	Reverse Recovery Charge		-	2	-	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The maximum value is specified by design at  $T_J = 150\text{ }^\circ\text{C}$ . Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

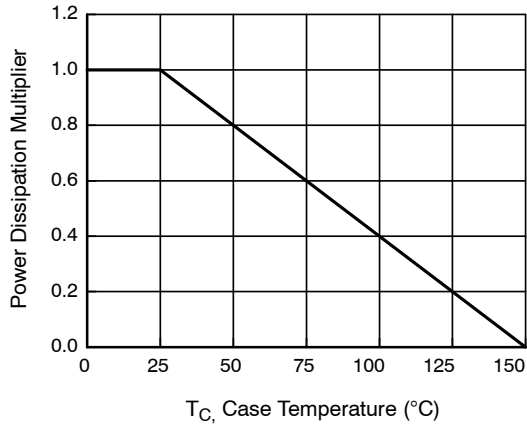


Figure 1. Normalized Power Dissipation vs. Case Temperature

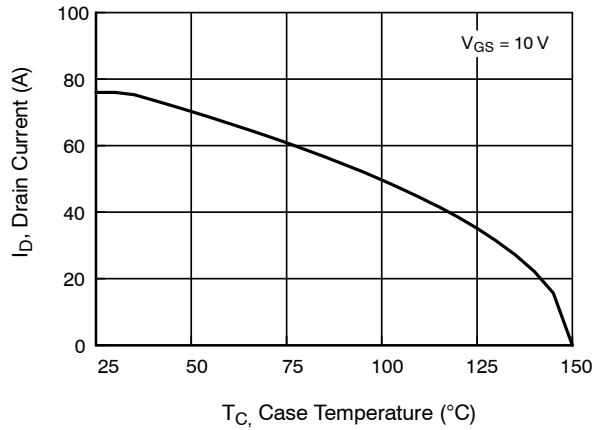


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

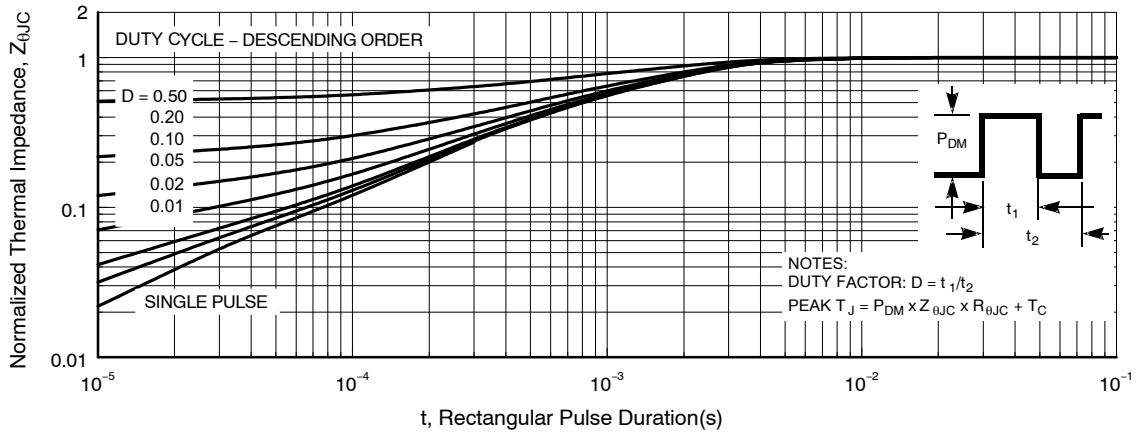


Figure 3. Normalized Maximum Transient Thermal Impedance

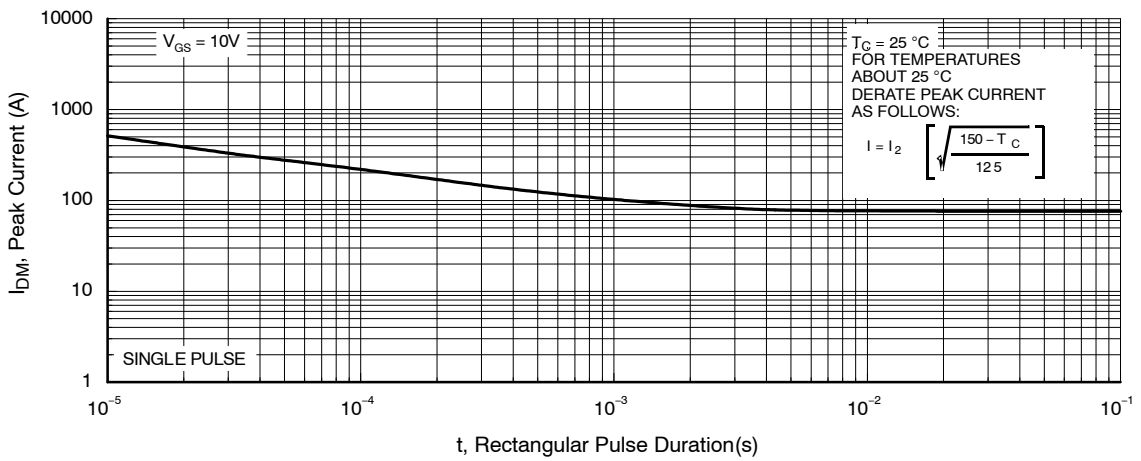


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

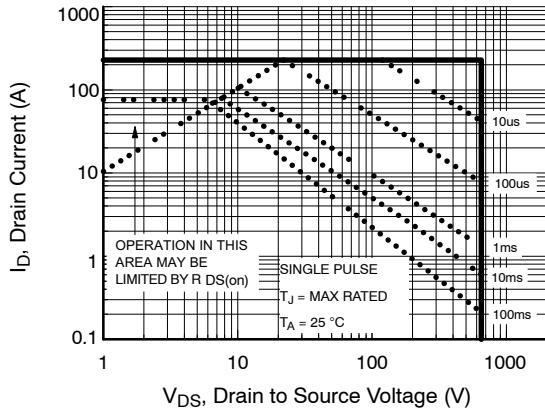


Figure 5. Forward Bias Safe Operating Area

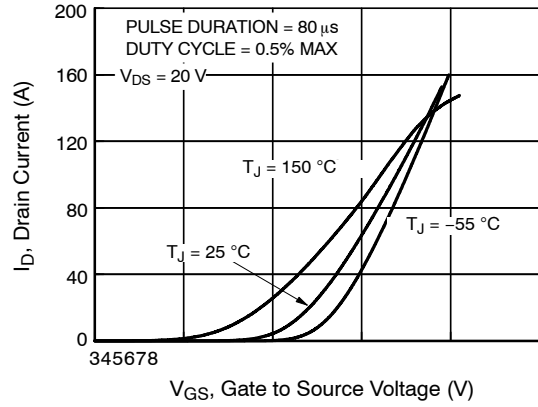


Figure 6. Transfer Characteristics

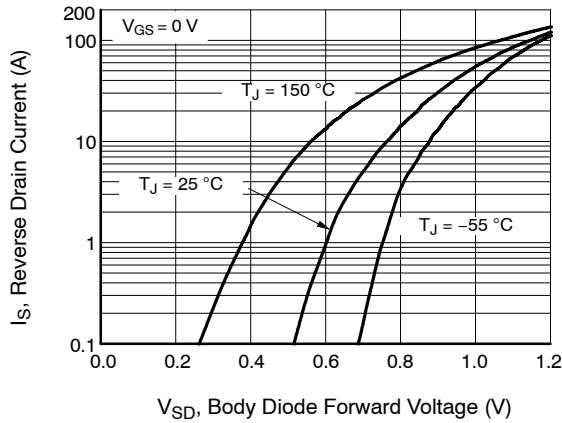


Figure 7. Forward Diode Characteristics

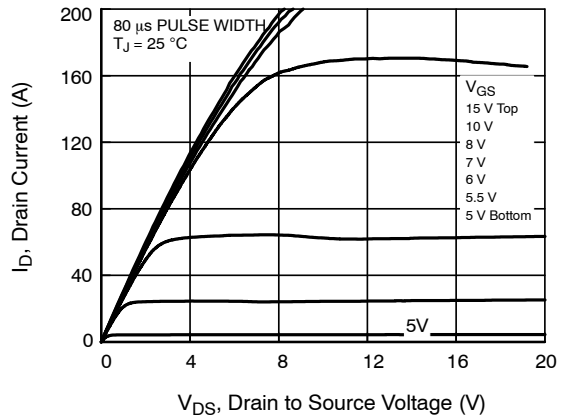


Figure 8. Saturation Characteristics

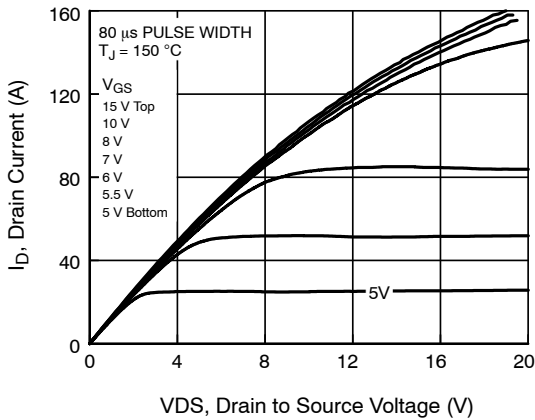


Figure 9. Saturation Characteristics

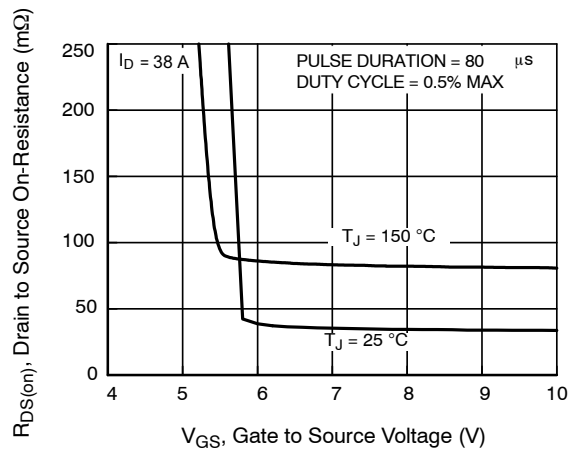


Figure 10.  $R_{DS(on)}$  vs. Gate Voltage

TYPICAL CHARACTERISTICS (continued)

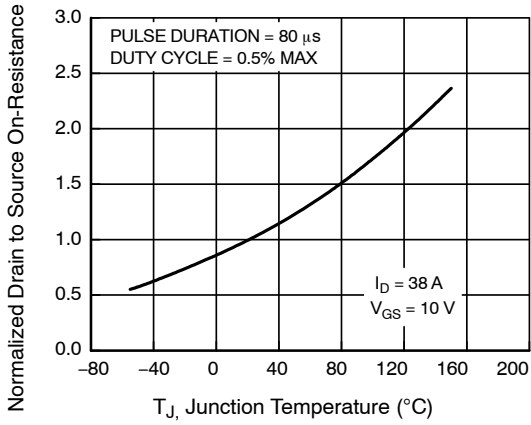


Figure 11. Normalized  $R_{DS(on)}$  vs. Junction Temperature

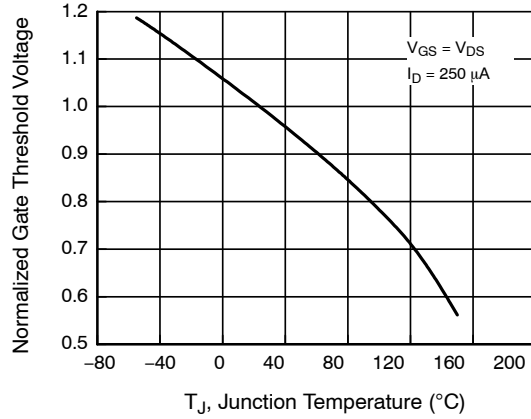


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

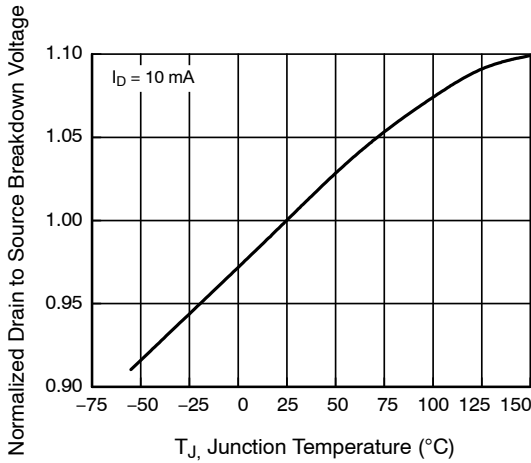


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

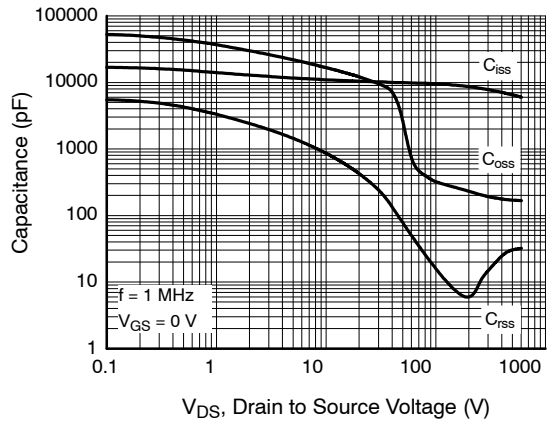


Figure 14. Capacitance vs. Drain to Source Voltage

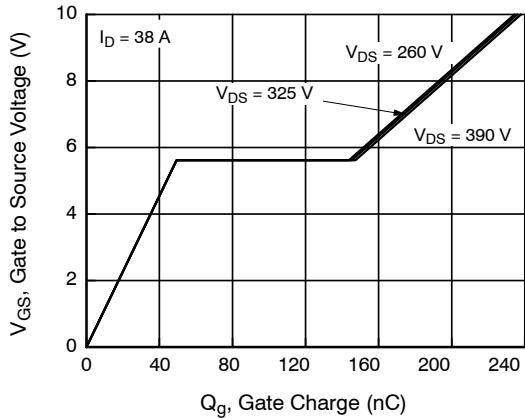


Figure 15. Gate Charge vs. Gate to Source Voltage

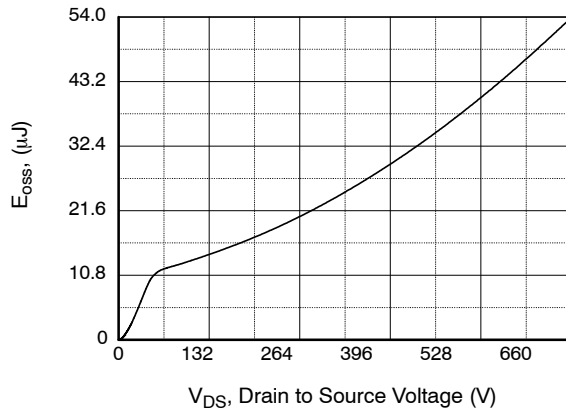


Figure 16.  $E_{oss}$  vs. Drain to Source Voltage

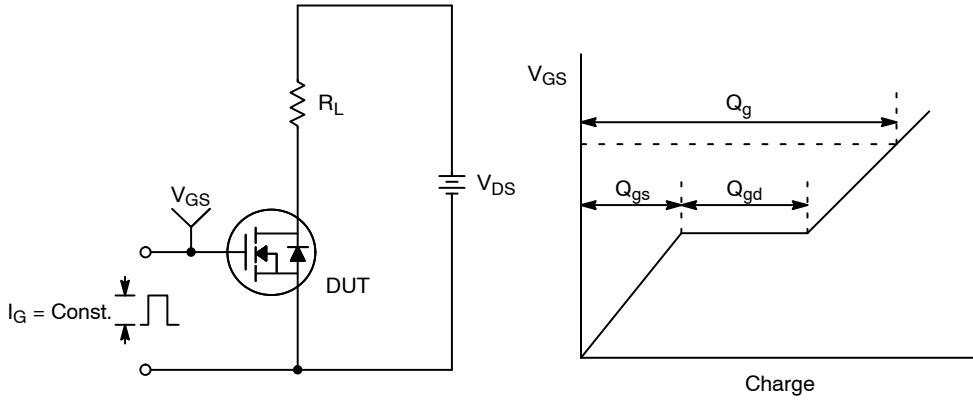


Figure 17. Gate Charge Test Circuit & Waveform

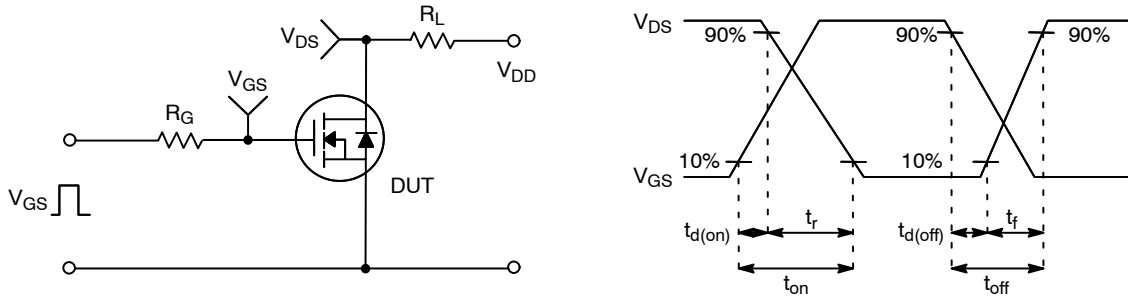


Figure 18. Resistive Switching Test Circuit & Waveforms

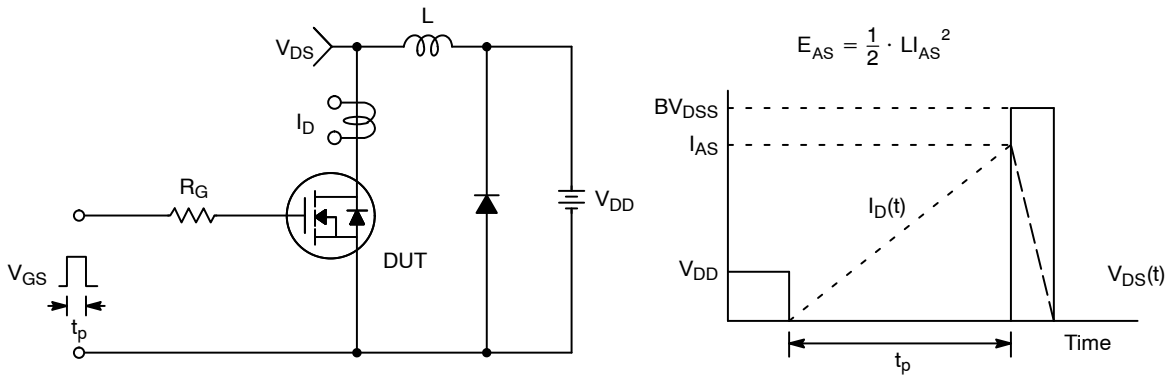


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

## FCH041N65F-F085

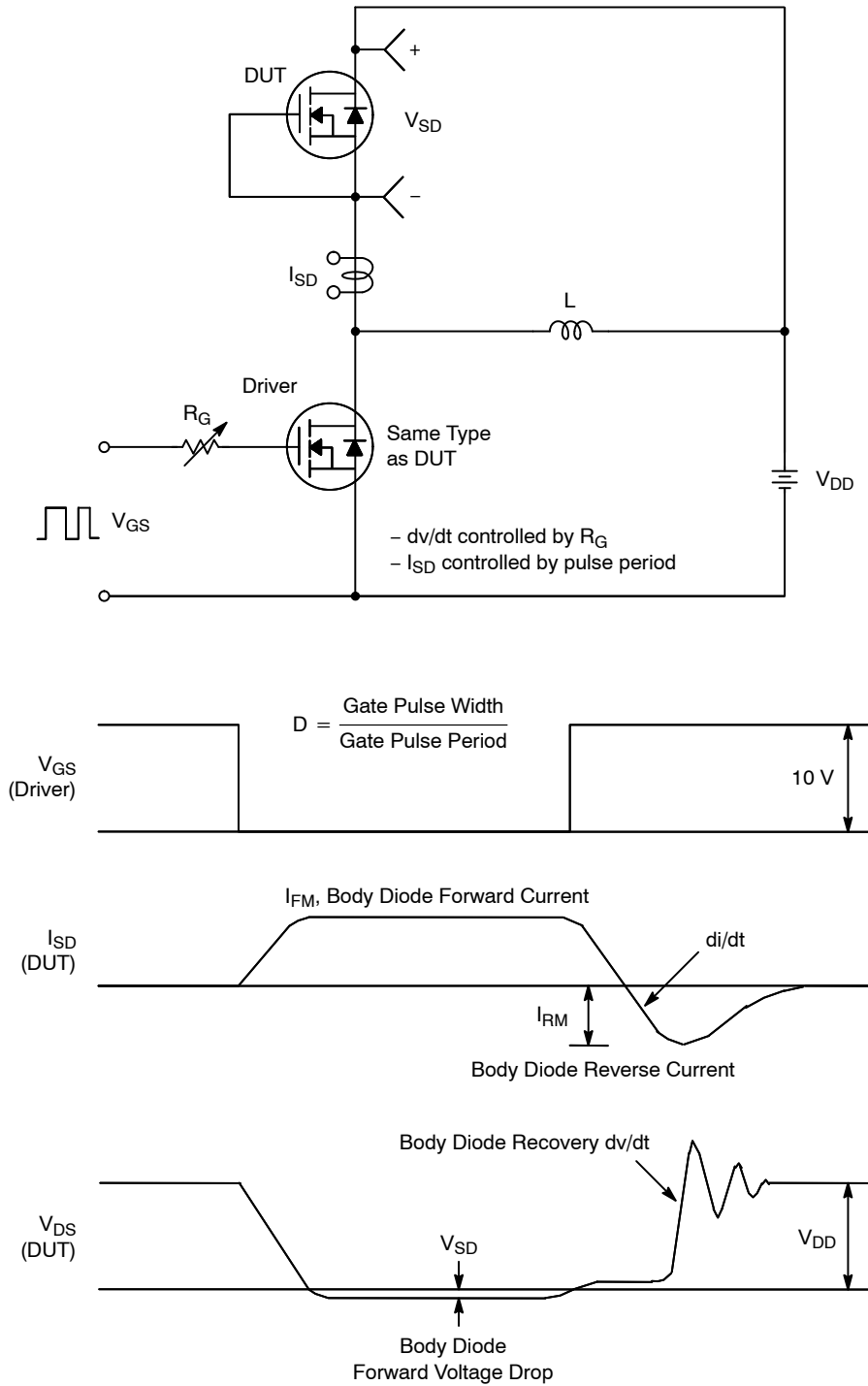


Figure 20. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FCH041N65F-F085	FCH041N65F	TO-247-3	-	-	30 Units

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# FCH041N65F-F085

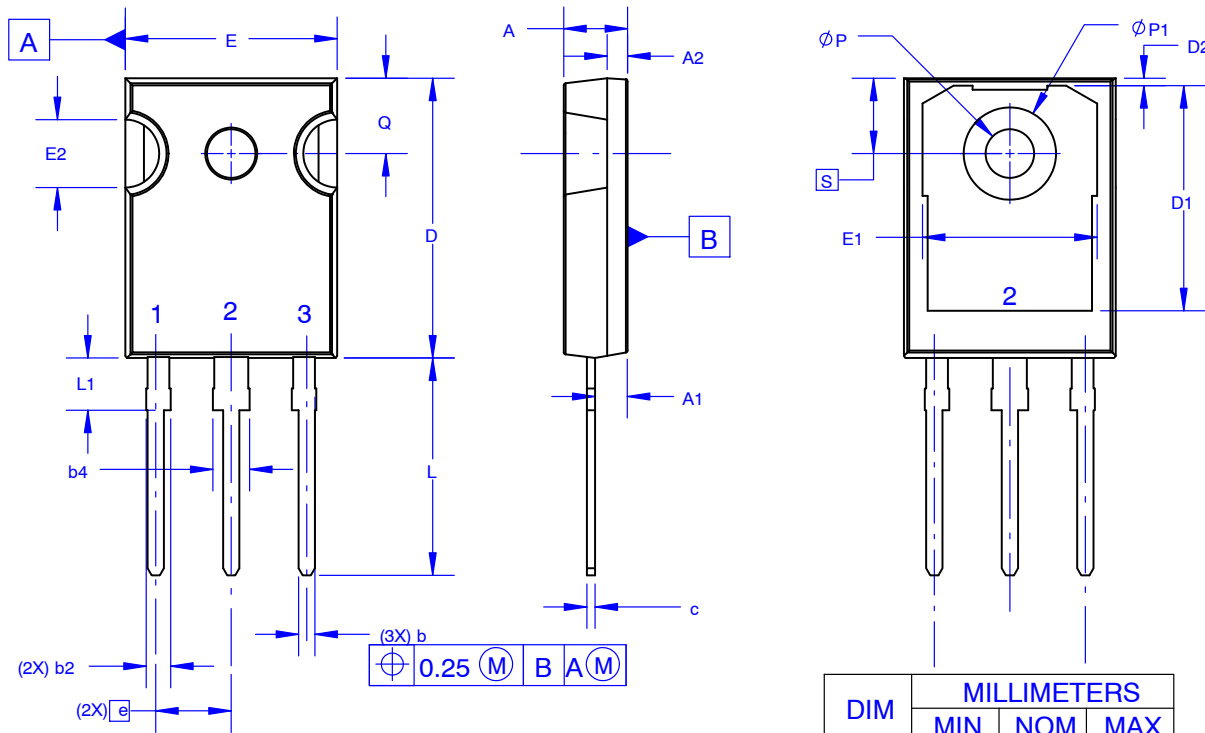
## REVISION HISTORY

Revision	Description of Changes	Date
7	Add $R_g$ max limit to 2.18 ohm.	11/26/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

**TO-247-3LD SHORT LEAD**  
**CASE 340CK**  
**ISSUE A**

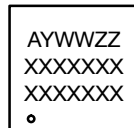
DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
φP	3.51	3.58	3.65
φP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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<b>DESCRIPTION:</b>	<b>TO-247-3LD SHORT LEAD</b>	<b>PAGE 1 OF 1</b>

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