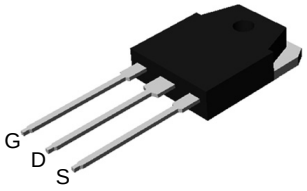
MOSFET – N-Channel, SUPERFET®

600 V, 47 A, 70 mΩ

FCA47N60, FCA47N60-F109

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
600 V	70 mΩ @ 10 V	47 A



TO−3P−3LD / EIAJ SC−65, ISOLATED
CASE 340BZ

Description

SUPERFET MOSFET is **onsemi**'s first generation of high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SUPERFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

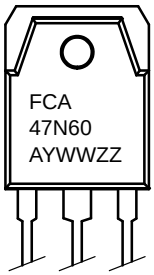
Features

- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 58 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 210 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 420 pF)
- 100% Avalanche Tested

Applications

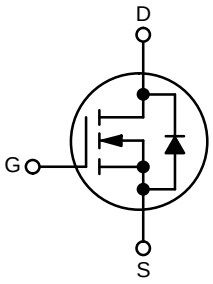
- Solar Inverter
- AC−DC Power Supply

MARKING DIAGRAM



FCA47N60	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot

N−CHANNEL MOSFET



ORDERING INFORMATION

Part Number	Package	Shipping
FCA47N60	TO−3P−3LD (Pb−Free)	450 Units / Tube
FCA47N60−F109		450 Units / Tube

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		FCA47N60	FCA47N60−F109	Unit
V_{DSS}	Drain−Source Voltage		600		V
I_D	Drain Current	− Continuous (T_C = 25°C)	47		A
		− Continuous (T_C = 100°C)	29.7		
I_{DM}	Drain Current	− Pulsed (Note 1)	141		A
V_{GSS}	Gate−Source Voltage		±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1800		mJ
I_{AR}	Avalanche Current (Note 1)		47		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		41.7		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_D	Power Dissipation	(T_C = 25°C)	417		W
		− Derate above 25°C	3.33		W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150		°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8” from Case for 5 Seconds		300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse−width limited by maximum junction temperature.
2. I_{AS} = 18 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 47 A, di/dt ≤ 200 A/μs, V_{DD} = 380 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	−	0.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	−	41.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_J = 25°C	600	−	−	V
		V_{GS} = 0 V, I_D = 250 μA, T_J = 150°C	−	650	−	
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	−	0.6	−	V/°C
BV_{DS}	Drain−Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 47 A	−	700	−	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	−	−	10	μA
		V_{DS} = 480 V, T_C = 125°C	−	−	100	
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	−	−	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	−	−	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	−	5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 23.5 A	−	0.058	0.07	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 23.5 A	−	40	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	−	5900	8000	pF
C_{oss}	Output Capacitance		−	3200	4200	pF
C_{rss}	Reverse Transfer Capacitance		−	250	−	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1.0 MHz	−	160	−	pF
C_{oss} eff.	Effective Output Capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	−	420	−	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 300 V, I_D = 47 A, R_G = 25 Ω (Note 4)	−	185	430	ns
t_r	Turn−On Rise Time		−	210	450	ns
$t_{d(off)}$	Turn−Off Delay Time		−	520	1100	ns
t_f	Turn−Off Fall Time		−	75	160	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 47 A, V_{GS} = 10 V (Note 4)	−	210	270	nC
Q_{gs}	Gate−Source Charge		−	38	−	nC
Q_{gd}	Gate−Drain Charge		−	110	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	47	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		−	−	141	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 47 A	−	−	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 47 A, dI_F/dt = 100 A/μs (Note 4)	−	590	−	ns
Q_{rr}	Reverse Recovery Charge		−	25	−	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

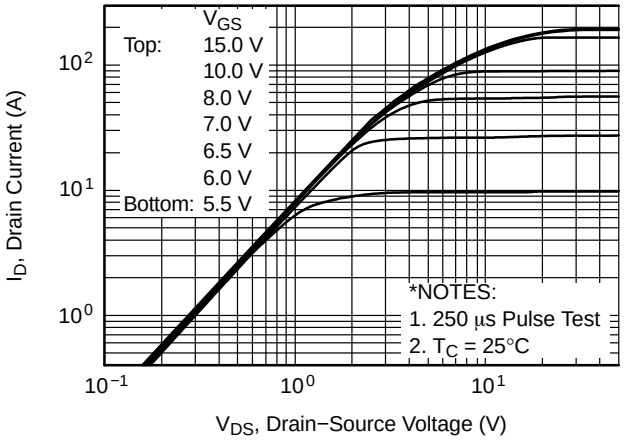


Figure 1. On−Region Characteristics

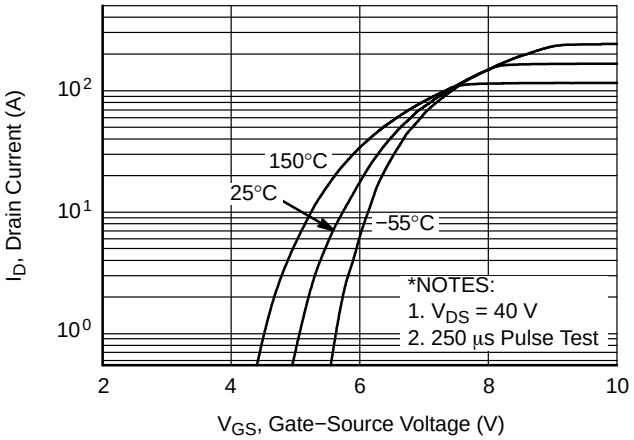


Figure 2. Transfer Characteristics

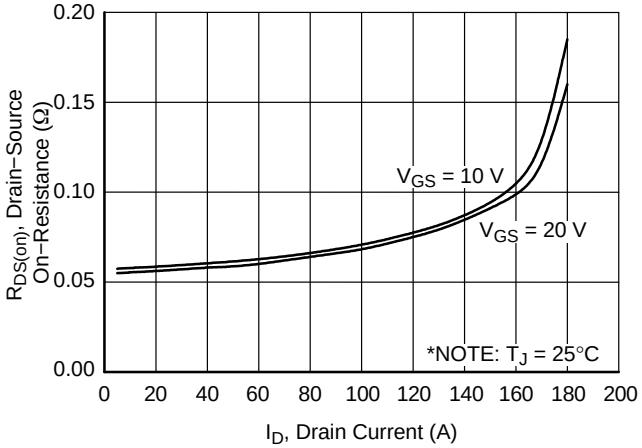


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

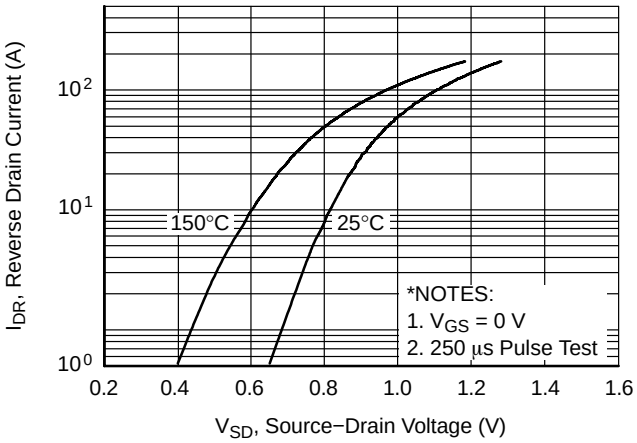


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

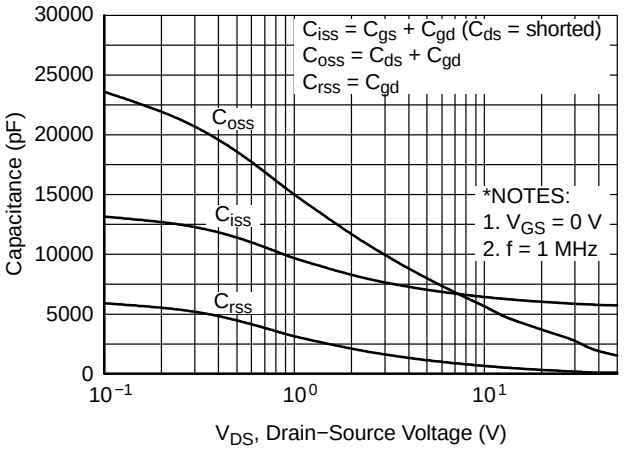


Figure 5. Capacitance Characteristics

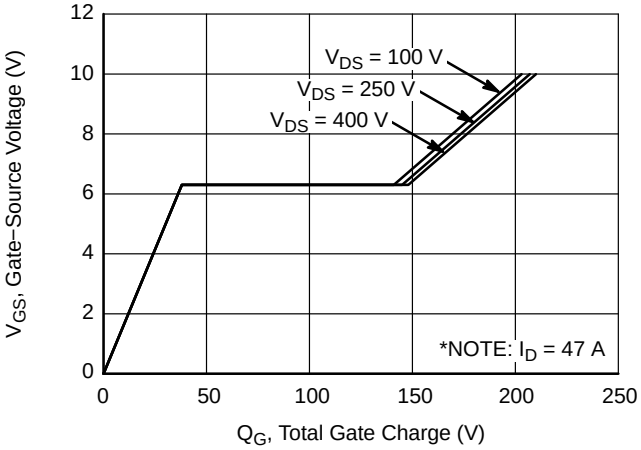


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

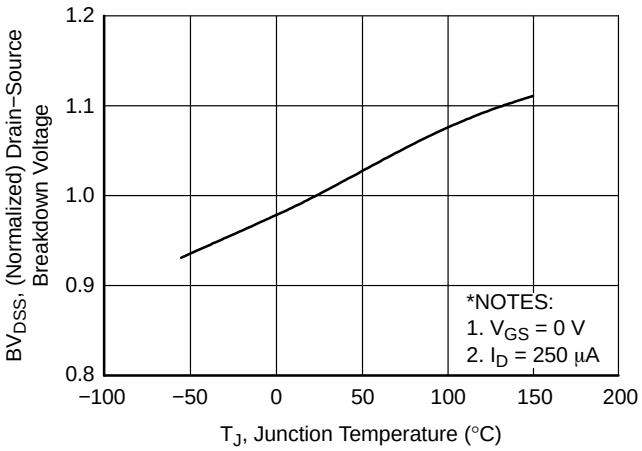


Figure 7. Breakdown Voltage Variation vs. Temperature

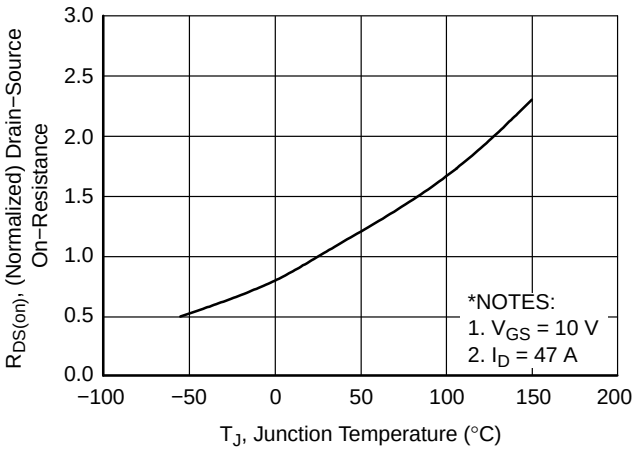


Figure 8. On−Resistance Variation vs. Temperature

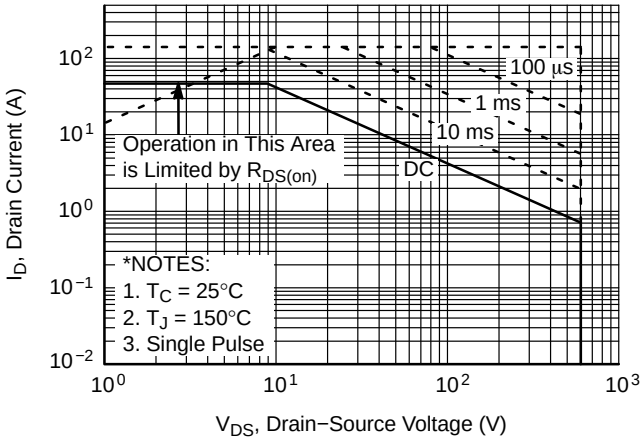


Figure 9. Safe Operating Area

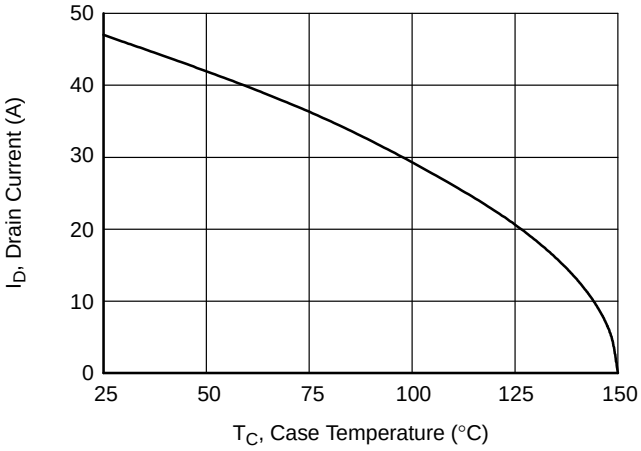


Figure 10. Maximum Drain Current vs. Case Temperature

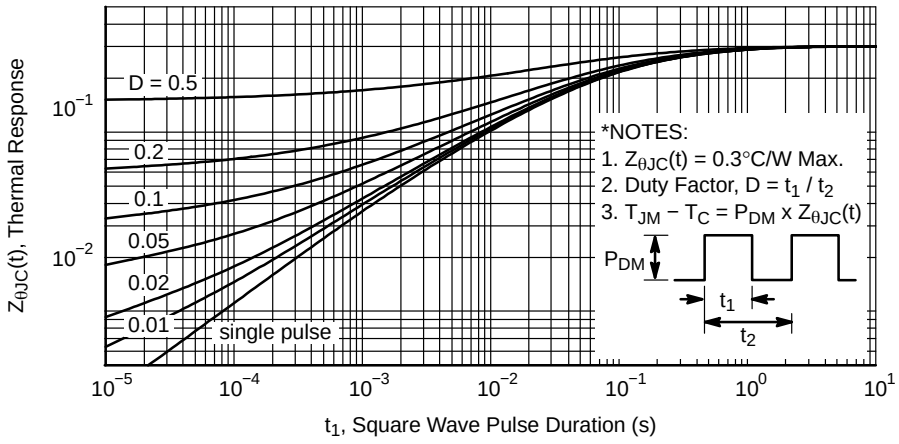


Figure 11. Transient Thermal Response Curve

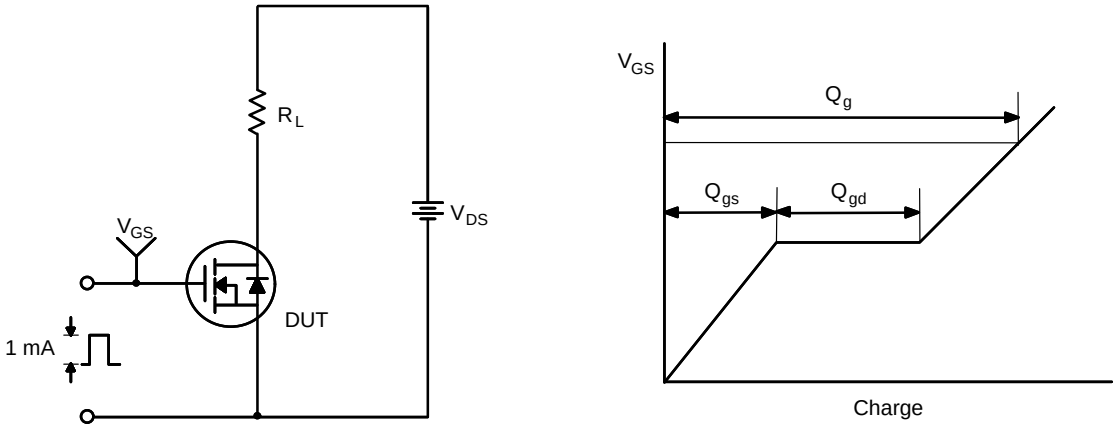


Figure 12. Gate Charge Test Circuit & Waveform

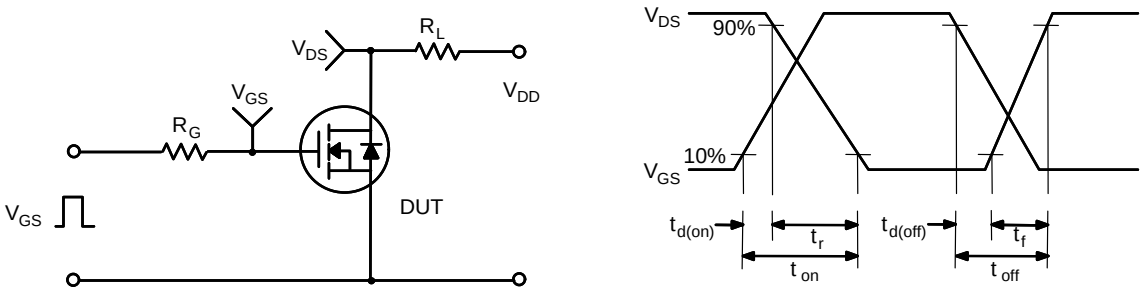


Figure 13. Resistive Switching Test Circuit & Waveforms

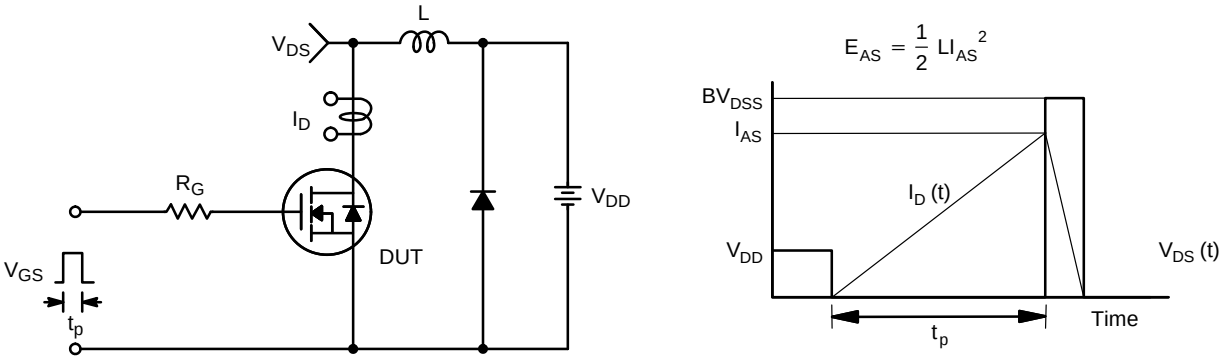


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

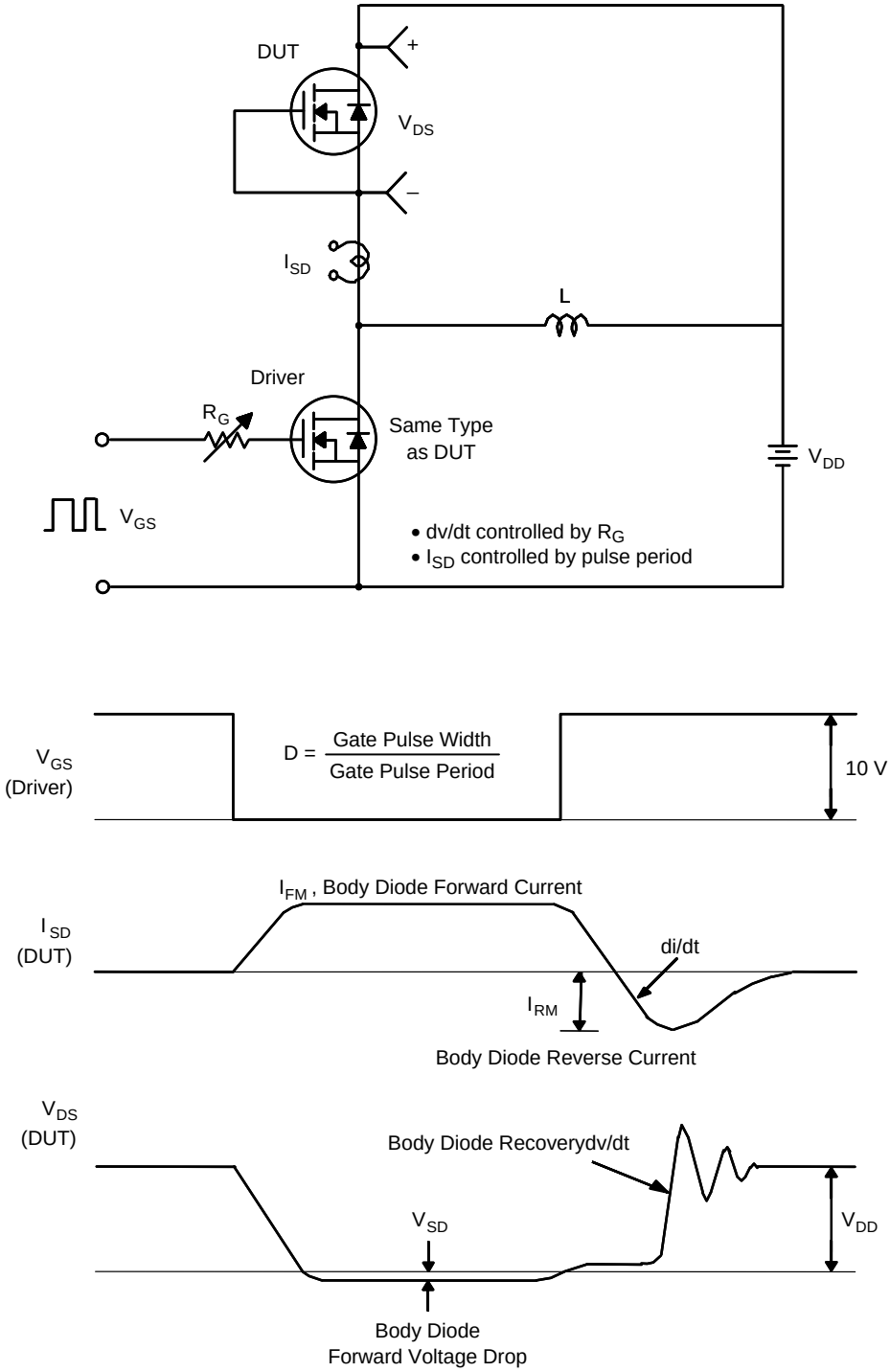


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO−3P−3LD / EIAJ SC−65, ISOLATED
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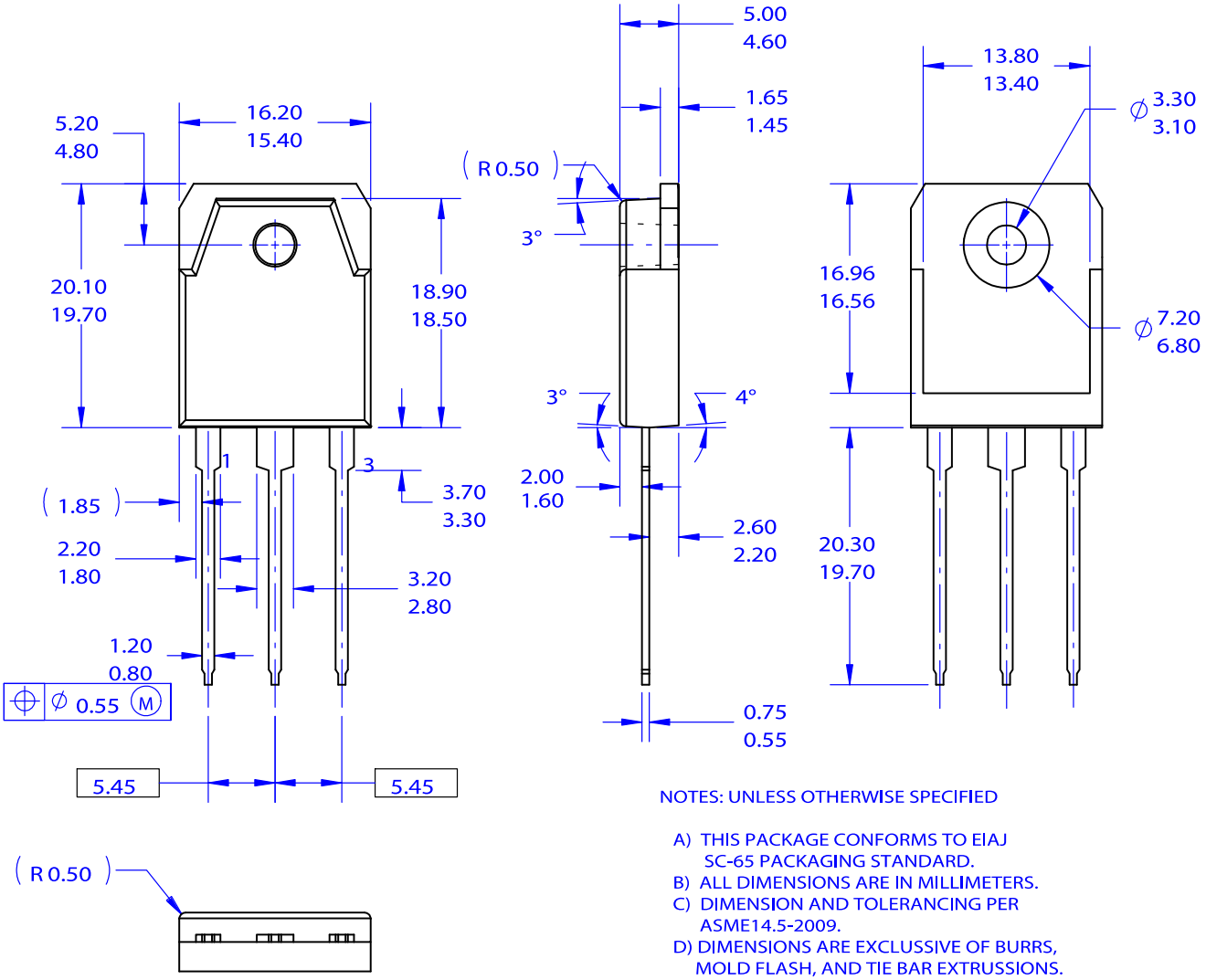
DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.

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