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DATA SHEET
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SD Protection Diode

Low Capacitance ESD Protection Diode for High Speed Data Line

ESD7004, SZESD7004

The ESD7004 surge protection is designed to protect high speed data lines from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0 and HDMI.

Features

- Low Capacitance (0.4 pF Typical, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

Typical Applications

- USB 3.0
- HDMI
- Display Port
- eSATA

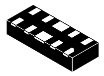
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +125	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact (ESD) IEC 61000-4-2 Air (ESD) ISO 10605 Contact (330 pF / 330 Ω) ISO 10605 Contact (330 pF / 2 kΩ) ISO 10605 Contact (150 pF / 2 kΩ)	ESD	±8 ±0.4 ±15 ±15 ±14 ±30 ±30	kV

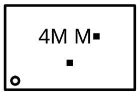
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

MARKING DIAGRAM

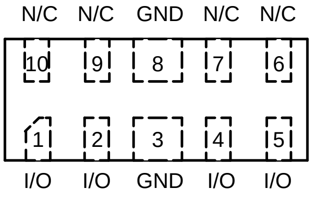


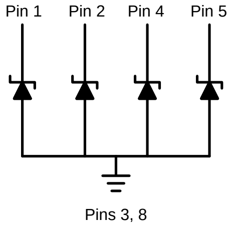
UDFN10
CASE 517BB

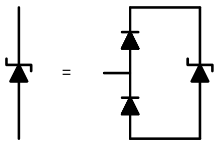


4M = Specific Device Code (tbd)
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION AND SCHEMATIC







ORDERING INFORMATION

Device	Package	Shipping†
ESD7004MUTAG	UDFN10 (Pb-Free)	3000 / Tape & Reel
SZESD7004MUTAG	UDFN10 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

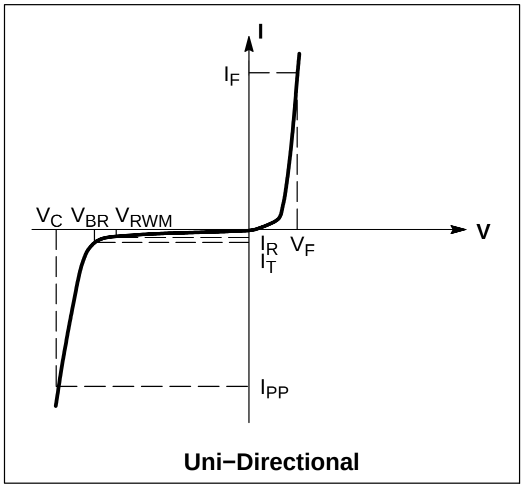
May, 2026 − Rev. 7

ELECTRICAL CHARACTERISTICS

(T_A = 25 °C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @ V_R = 0 and f = 1.0 MHz

* See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.5			V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND			1.0	µA
Clamping Voltage (Note 1)	V_C	I_{PP} = 1 A, I/O Pin to GND (8 x 20 µs pulse)			10	V
Clamping Voltage (Note 2)	V_C	IEC61000-4-2, ±8 KV Contact	See Figures 7 and 8			V
Clamping Voltage TLP (Note 3) See Figures 11 and 12	V_C	I_{TLP} = 8 A I_{TLP} = 16 A I_{TLP} = −8 A I_{TLP} = −16 A		11.4 15.6 −4.5 −8.1		V
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins		0.2	0.3	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.4	0.5	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Surge current waveform per Figure 15.
2. For test procedure see Figures 13 and 14 and application note AND8307/D.
3. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

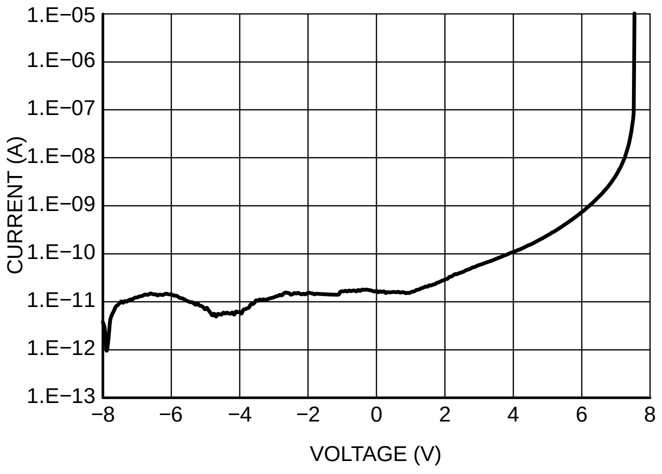


Figure 1. IV Characteristics

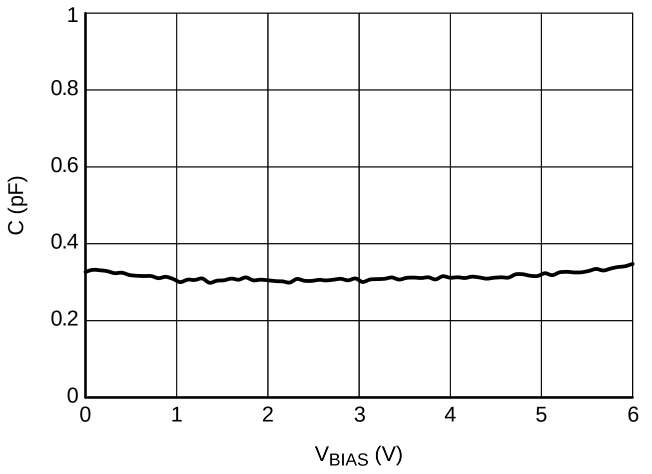


Figure 2. CV Characteristics

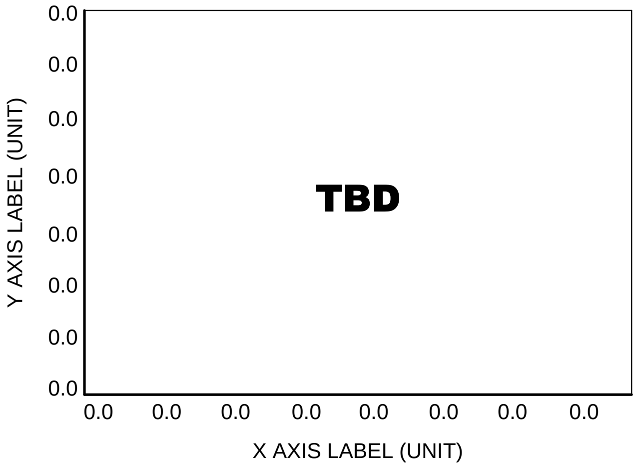


Figure 3. I_R vs. Temperature Characteristics

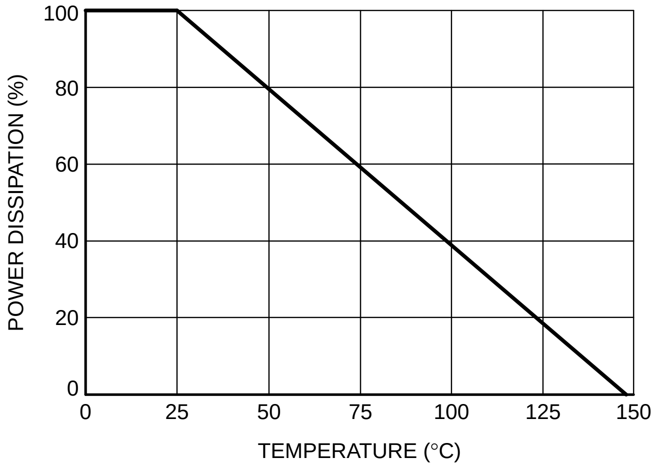


Figure 4. Steady State Power Derating

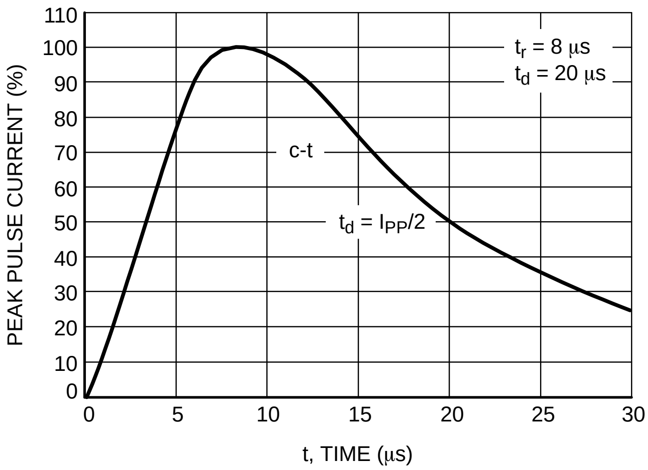


Figure 5. Pulse Waveform (8/20 µs)

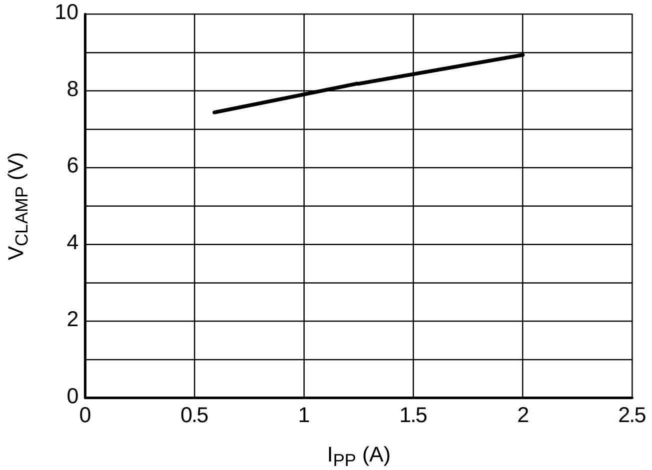


Figure 6. Clamping Voltage vs. Peak Pulse Current (8/20 µs)

TYPICAL CHARACTERISTICS (T$_J$ = 25 °C unless otherwise noted)

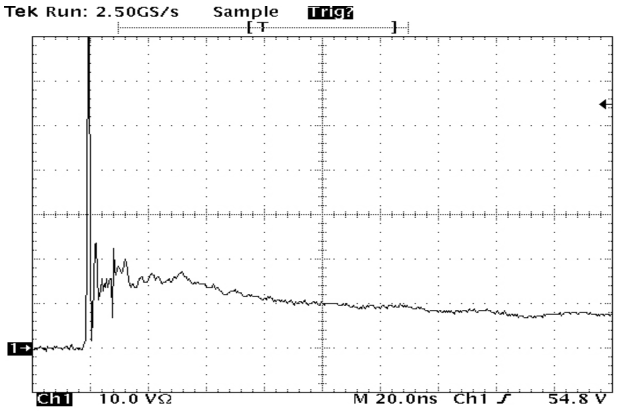


Figure 7. IEC61000-4-2 +8 KV Contact ESD Clamping Voltage

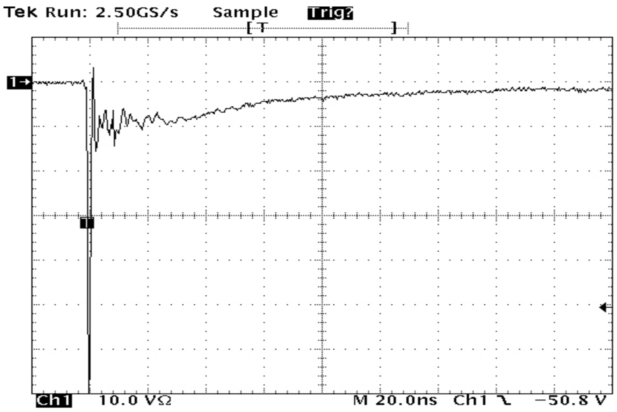


Figure 8. IEC61000-4-2 −8 KV Contact Clamping Voltage

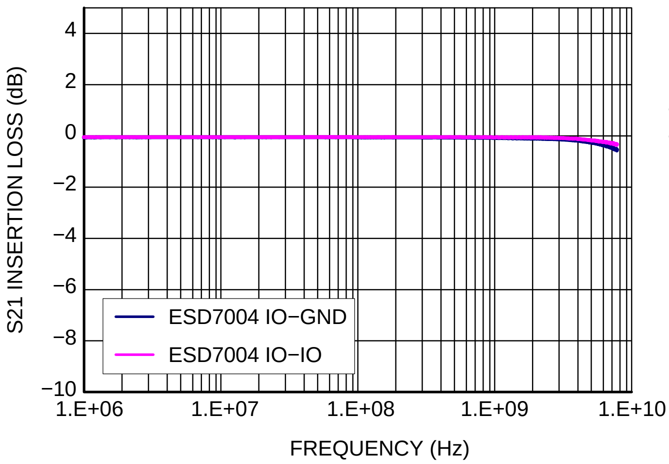


Figure 9. ESD7004 Insertion Loss

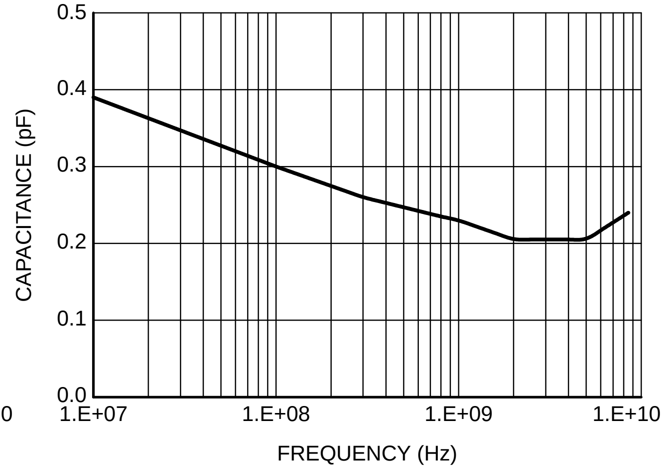


Figure 10. Typical Capacitance vs. Frequency

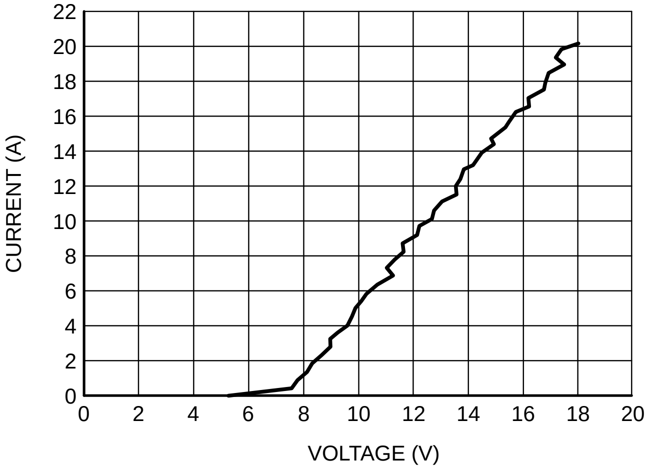


Figure 11. Positive TLP I-V Curve

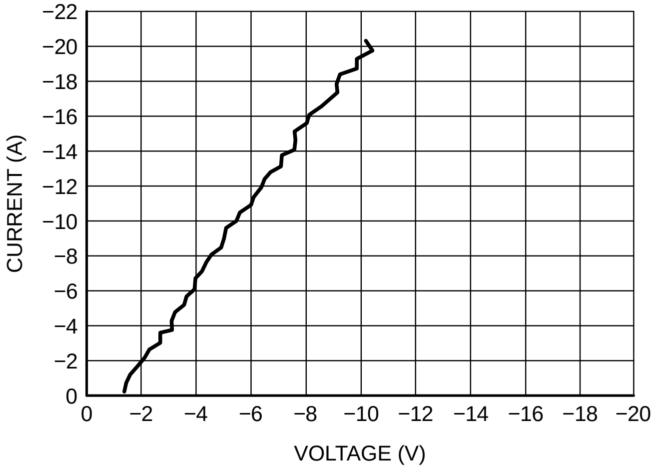


Figure 12. Negative TLP I-V Curve

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

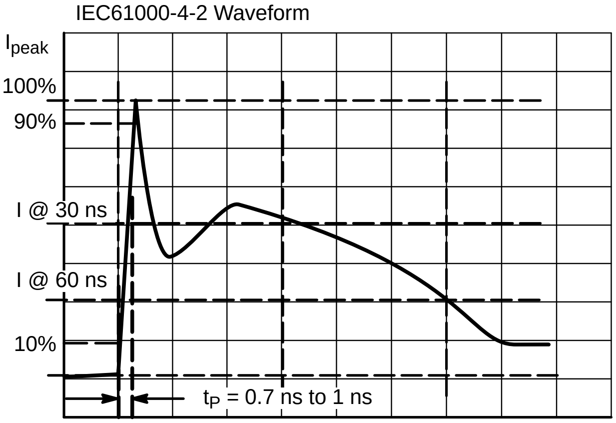


Figure 13. IEC61000-4-2 Spec

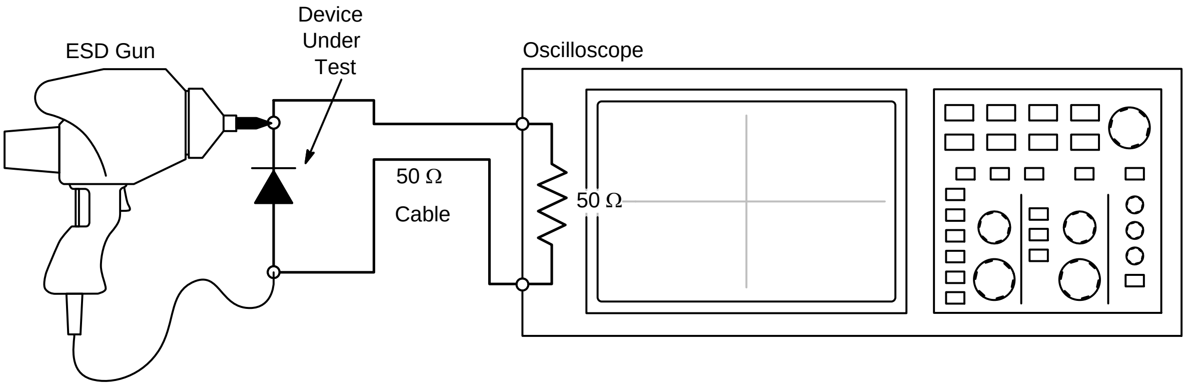


Figure 14. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

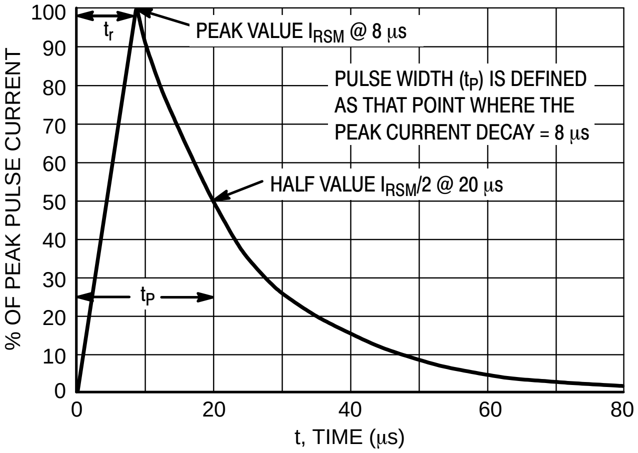


Figure 15. 8 x 20 μs Pulse Waveform

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 16. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 17 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. A typical TLP I-V curve for the ESD7004 is shown in Figures 11 and 12.

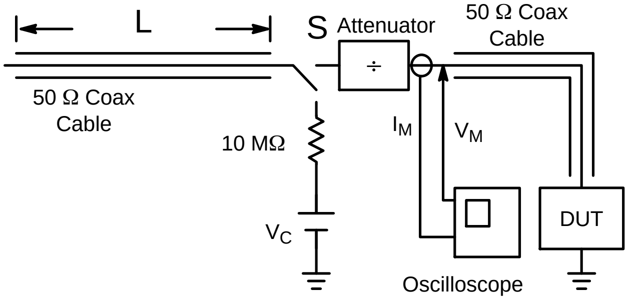


Figure 16. Simplified Schematic of a Typical TLP System

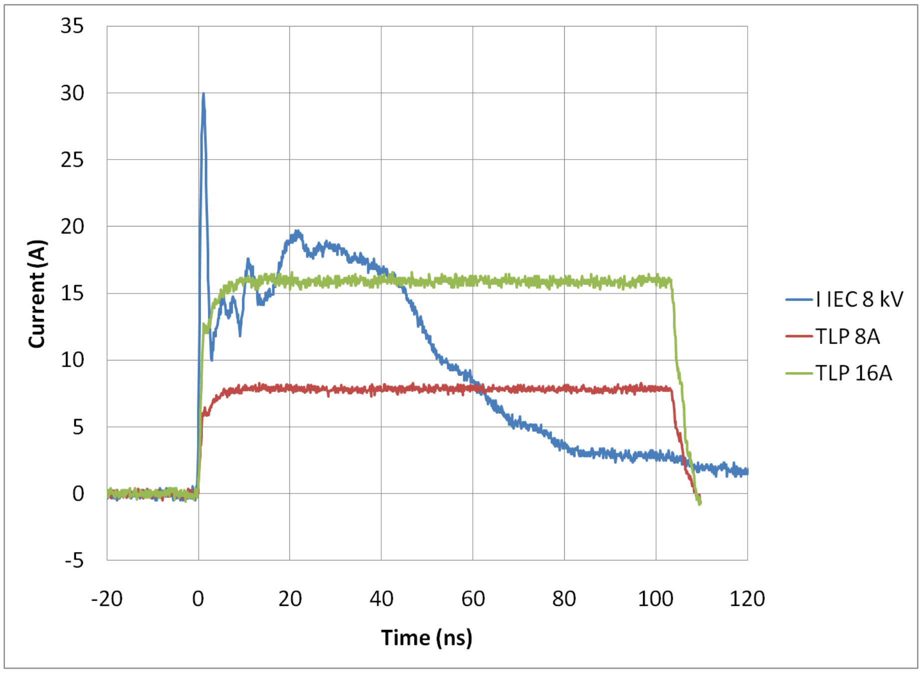
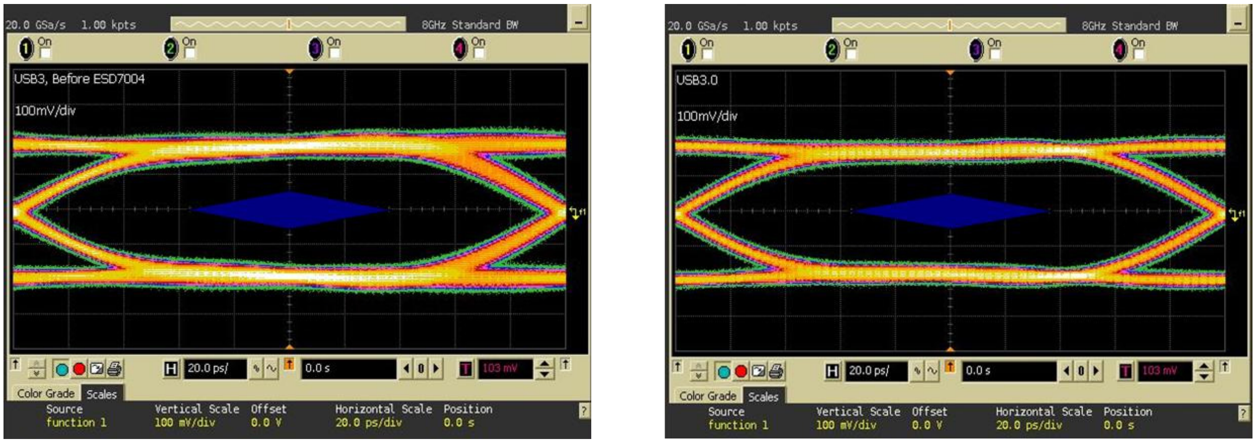
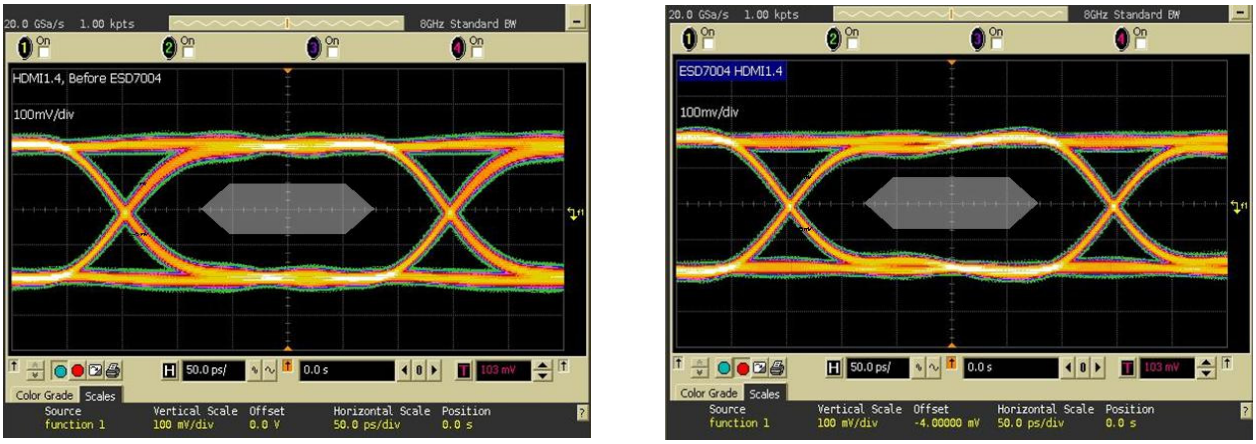


Figure 17. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms



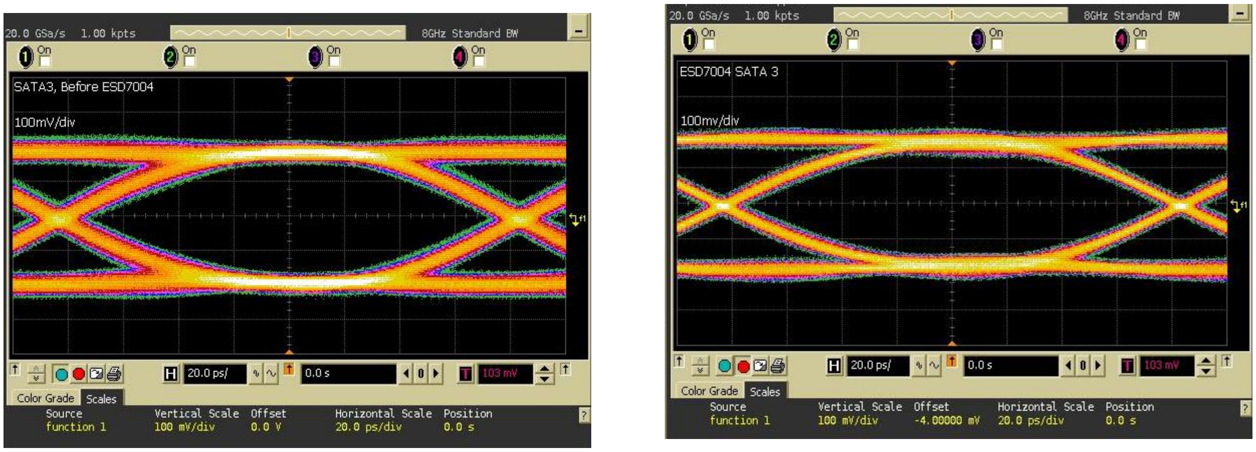
Without ESD **With ESD7004**

Figure 18. USB3.0 Eye Diagram with and without ESD7004. 5.0 Gb/s, 400 mV_{PP}



Without ESD **With ESD7004**

Figure 19. HDMI1.4 Eye Diagram with and without ESD7004. 3.4 Gb/s, 400 mV_{PP}



Without ESD **With ESD7004**

Figure 20. ESATA3.0 Eye Diagram with and without ESD7004. 6 Gb/s, 400 mV_{PP}

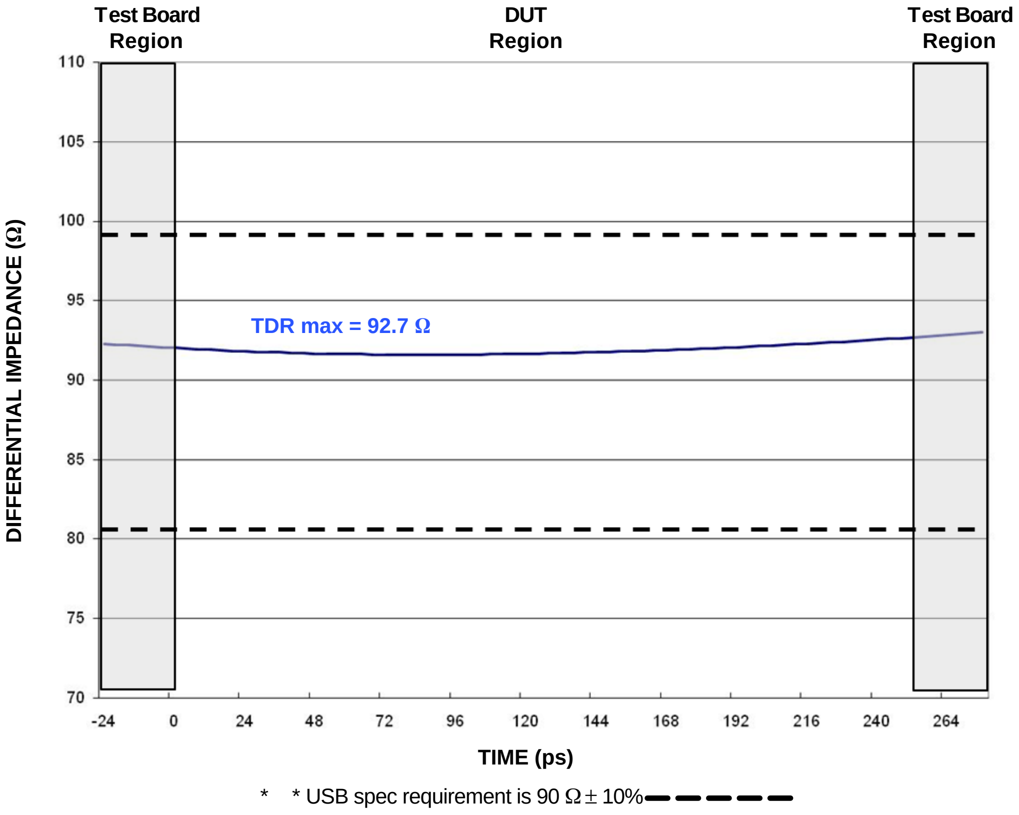


Figure 21. USB TDR Measurement. 90 Ω Differential Impedance Target, 200 ps Rise Time

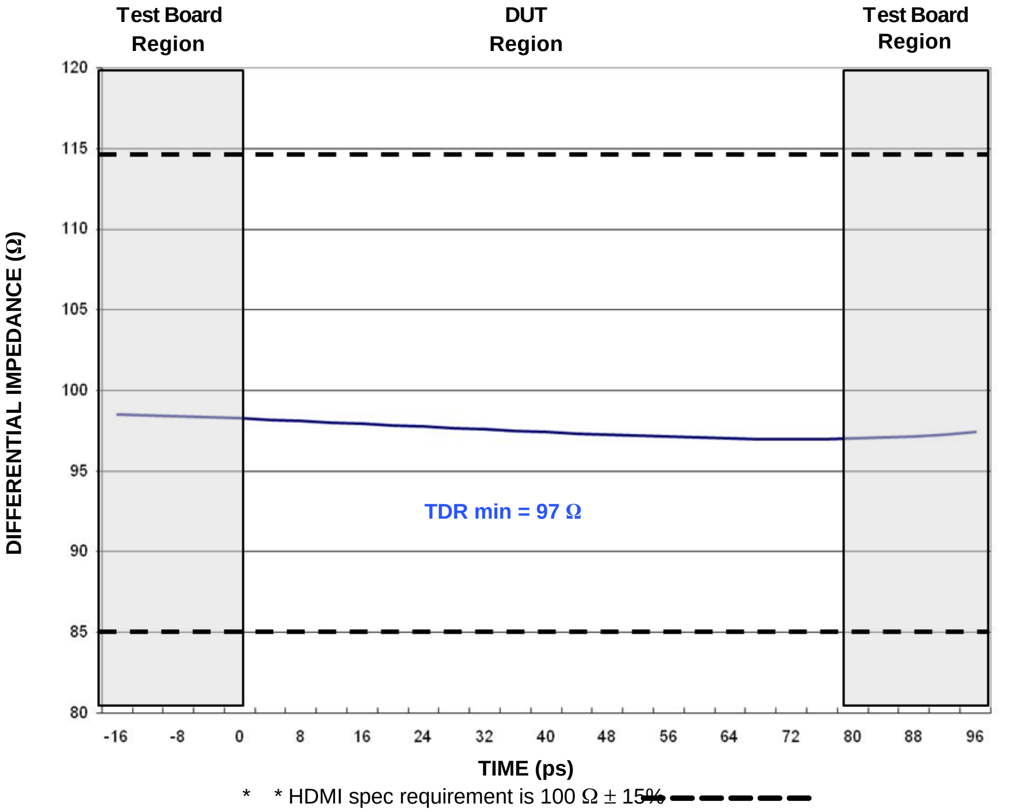


Figure 22. HDMI TDR Measurement. 100 Ω Differential Impedance Target, 200 ps Rise Time

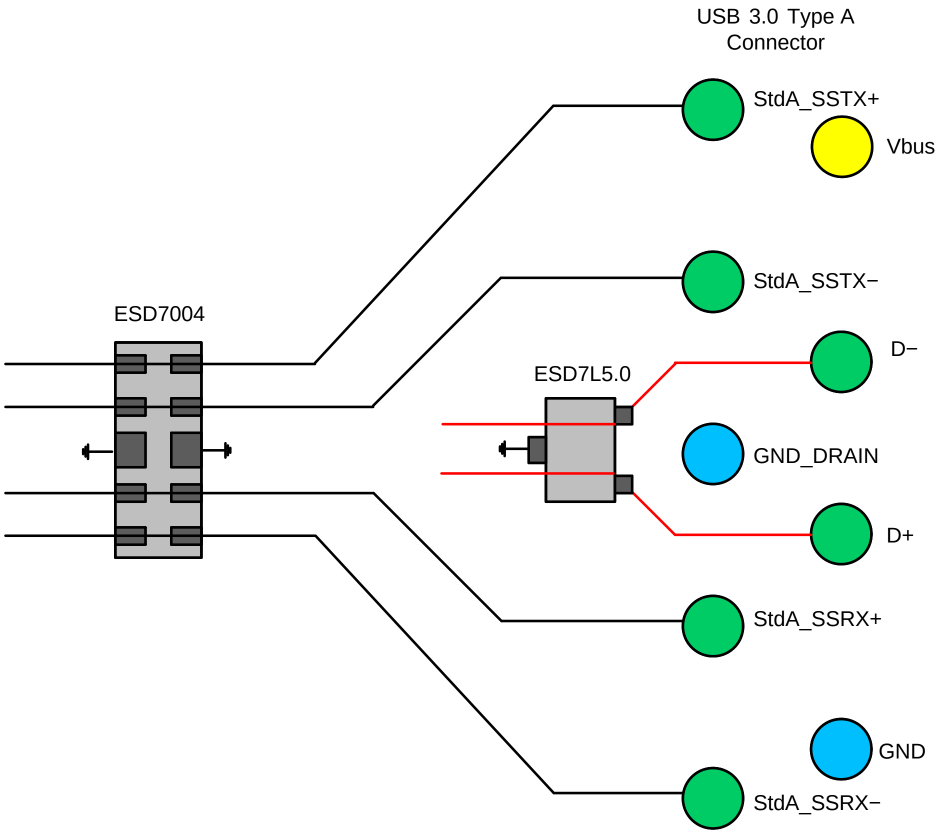


Figure 23. USB3.0 Standard A Connector Layout Diagram

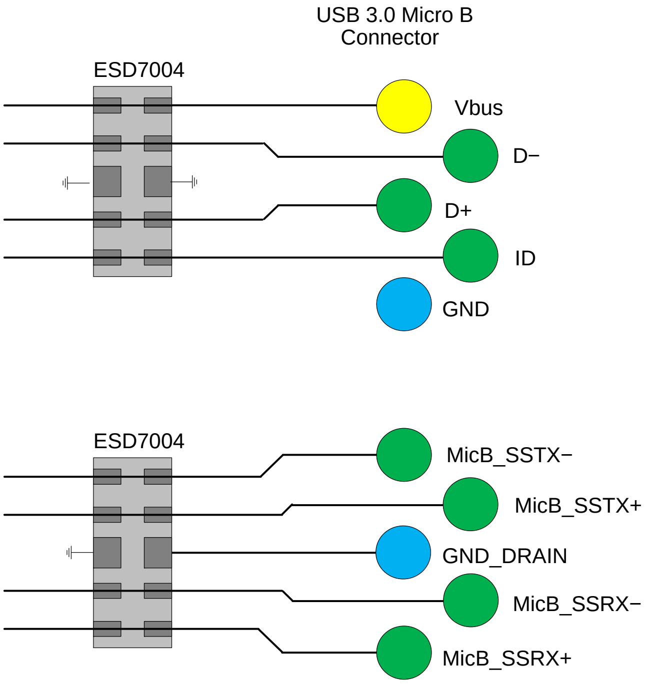


Figure 24. USB3.0 Micro B Connector Layout Diagram

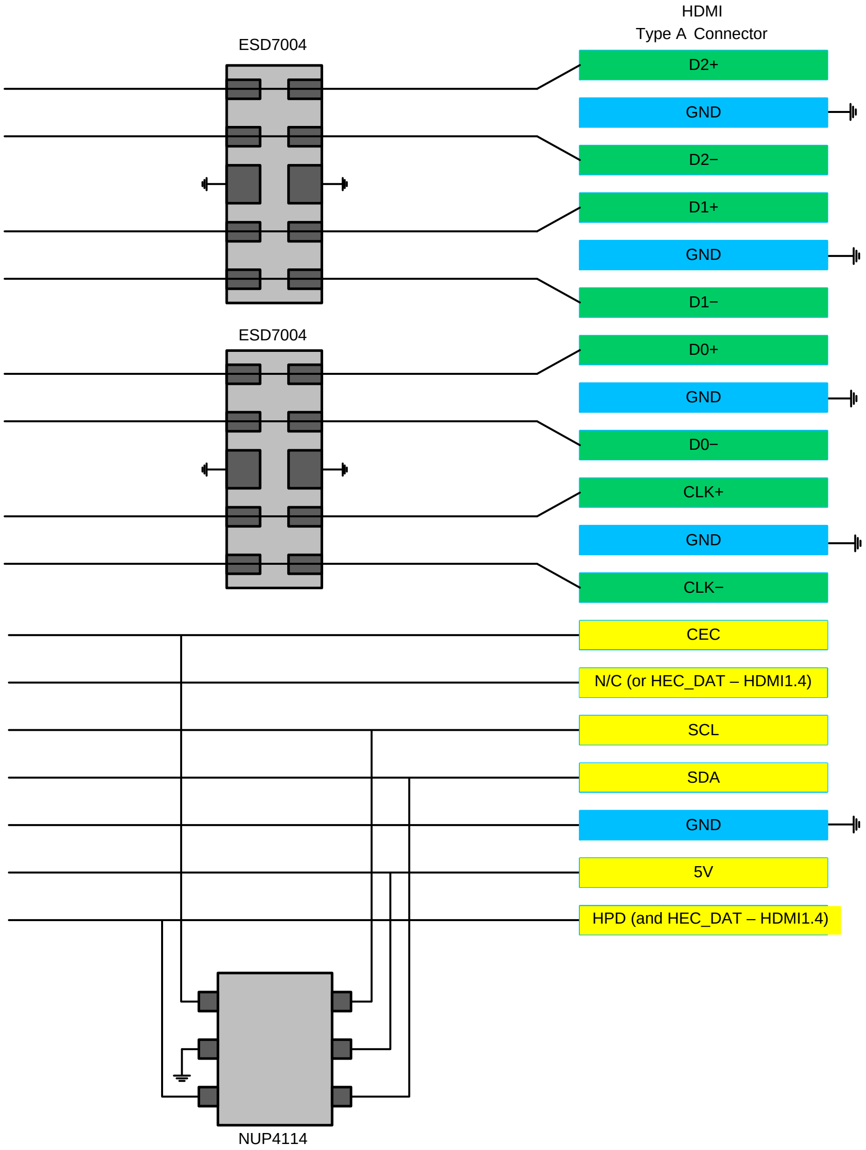


Figure 25. HDMI Layout Diagram

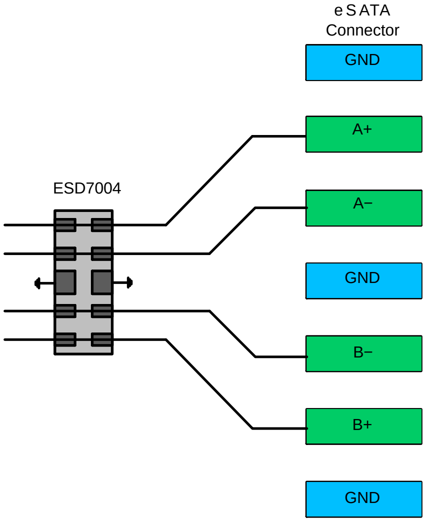


Figure 26. eSATA Layout Diagram

REVISION HISTORY

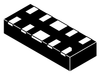
Revision	Description of Changes	Date
7	Electrical Characteristics table updated with latest data and new Typical Characteristics plot added to match latest **onsemi** datasheet layout.	5/22/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

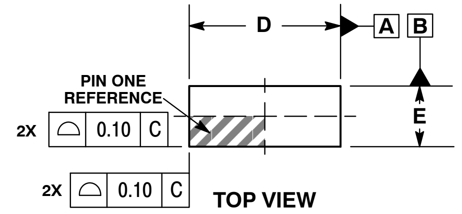
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

UDFN10 2.5x1, 0.5P
CASE 517BB
ISSUE O

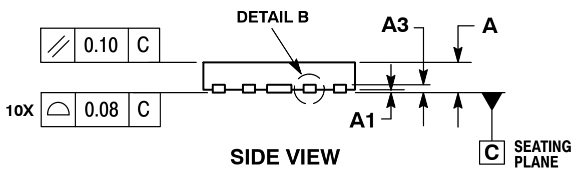
DATE 17 NOV 2009



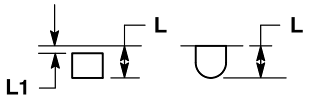
SCALE 4:1



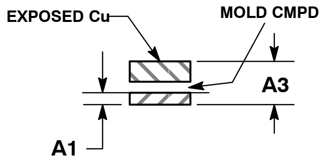
TOP VIEW



SIDE VIEW



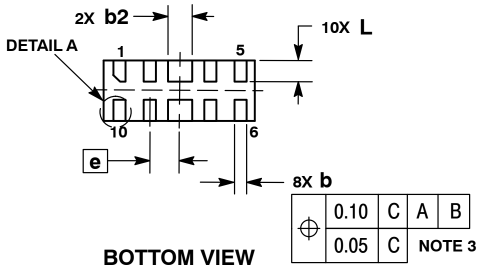
DETAIL A
OPTIONAL
CONSTRUCTIONS



DETAIL B
OPTIONAL
CONSTRUCTION

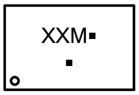
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
b2	0.35	0.45
D	2.50 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.05



BOTTOM VIEW

GENERIC MARKING DIAGRAM*

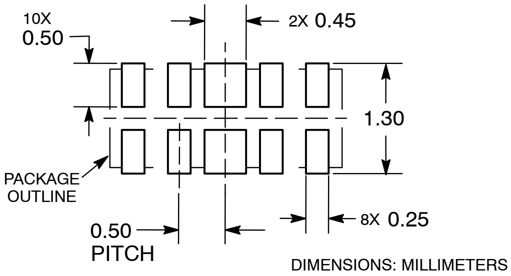


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**UDFN10 2.5X1, 0.5P**	**PAGE 1 OF 1**

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