ADT7462

Flexible Temperature, Voltage Monitor, and System Fan Controller

The ADT7462 is a flexible systems monitor IC, suitable for use in a wide variety of applications. It can monitor temperature in up to three remote locations, as well as its ambient temperature.

There are up to four PWM outputs. These can be used to control the speed of a cooling fan by varying the % duty cycle of the PWM drive signal applied to the fan. The ADT7462 supports high frequency PWM for 4-wire fans and low frequency PWM for 2-wire and 3-wire fans. Up to eight TACH inputs can be used to measure the speed of 3-wire and 4-wire fans. There are up to 13 voltage monitoring inputs, ranging from 12 V to 0.9 V.

The ADT7462 is fully compatible with SMBus 1.1 and SMBus 1.0. The ADT7462 also includes a $\overline{\text{THERM}}$ I/O and a $\overline{\text{RESET}}$ I/O.

The ADT7462 is available in a 32-lead LFCSP_VQ. Many of the pins are multi-functional. Five easy configuration options can be set up using the easy configuration register. Users choose the configuration closest to their requirements; individual pins can be reconfigured after the easy configuration option has been chosen.

Features

- One Local and Up to Three Remote Temperature Channels Series Resistance Cancellation On Remote Channels
- Thermal Protection Using $\overline{\text{THERM}}$ Pins
- Up to Four PWM Fan Drive Outputs Supports Both High and Low Frequency PWM Drives
- Up to Eight TACH Inputs Measures the Speed of 3-wire and 4-wire Fans
- Automatic Fan Speed Control Loop Includes Dynamic T_{MIN} Control
- Monitors Up to 13 V Inputs
- Monitors Up to 7 VID Inputs; Includes On-The-Fly (OTF) VID Support
- Bidirectional Reset
- Chassis Intrusion Detect
- SMBus 1.1 and SMBus 1.0 Compatible
- 3.3 V and 5.0 V Operation
- Extended Operating Range from −40°C to +125°C
- Space-saving 32-lead Chip Scale Package
- This is a Pb-Free Device*

Applications

- Servers and Personal Computers
- Telecommunications Equipment
- Test Equipment and Measurement Instruments

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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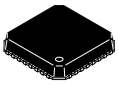
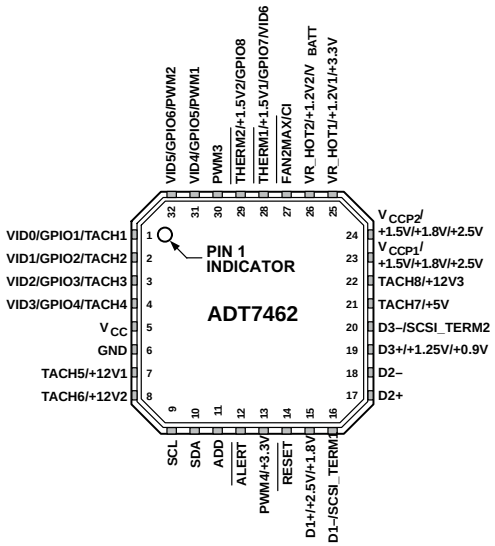


LFCSP−32
CASE 932

PIN ASSIGNMENT



MARKING DIAGRAM

ADT7462ACPZ	= Specific Device Code
#	= Pb-Free Package
YYWW	= Date Code
AL	= Assembly Lot
CC	= Country Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 81 of this data sheet.

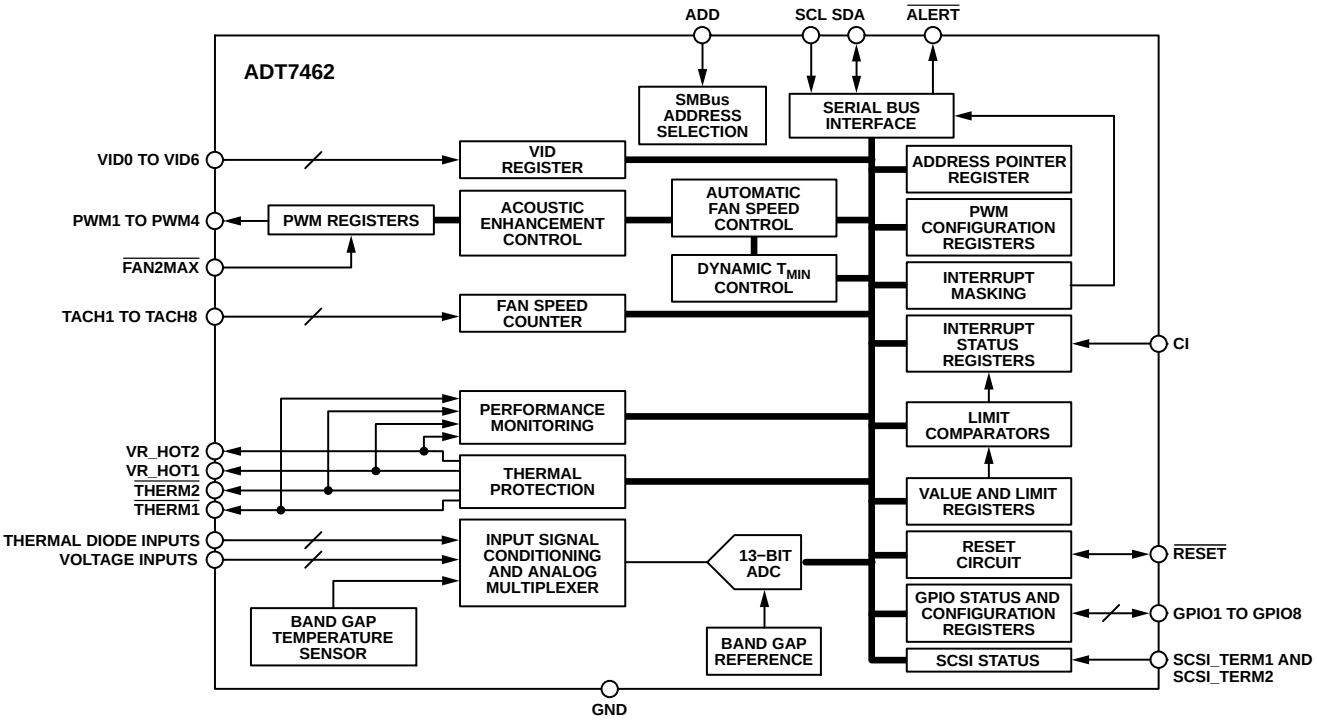


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Supply Voltage	6.5	V
Voltage on +12V Pin	20	V
Voltage on V_{BATT} Pin	4.0	V
Voltage on Any Other Input or Output Pin	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Operating Temperature Range	−40 to +125	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering Lead Temperature (Soldering, 10 sec) IR Reflow Peak Temperature	 300 260	°C
ESD Rating	1500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
32-lead LFCSP_VQ	32.5	32.71	°C/W

1. θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description	POR Default
1	VID0/GPIO1/TACH1	VID0: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO1: Open-Drain I/O. General-purpose input/output. TACH1: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1.	TACH1
2	VID1/GPIO2/TACH2	VID1: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO2: Open-Drain I/O. General-purpose input/output. TACH2: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2.	TACH2
3	VID2/GPIO3/TACH3	VID2: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO3: Open-Drain I/O. General-purpose input/output. TACH3: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.	TACH3
4	VID3/GPIO4/TACH4	VID3: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO4: Open-Drain I/O. General-purpose input/output. TACH4: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4.	TACH4
5	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. The ADT7462 can also be powered from a 5.0 V supply.	V_{CC}
6	GND	Ground Pin.	GND
7	TACH5/+12V1	TACH5: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 5. +12V1: Analog Input. Monitors 12 V Power Supply 1. Attenuators switched on by default.	TACH5
8	TACH6/+12V2	TACH6: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 6. +12V2: Analog Input. Monitors 12 V Power Supply 2. Attenuators switched on by default.	TACH6
9	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.	SCL
10	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus pullup.	SDA
11	ADD	The state of this pin on powerup determines the SMBus device address.	ADD
12	$\overline{\text{ALERT}}$	Active Low Open-Drain Digital Output. Requires 10 kΩ typical pullup. The $\overline{\text{ALERT}}$ pin is used to signal out-of-limit comparisons of temperature, voltage, and fan speed. This is compatible with SMBus $\overline{\text{ALERT}}$.	$\overline{\text{ALERT}}$
13	PWM4/+3.3V	PWM4: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 4. +3.3V: Analog Input. Monitors 3.3 V power supply.	PWM4
14	$\overline{\text{RESET}}$	Active Low Open-Drain Digital I/O. Power-on reset, 5 mA driver (weak 100 kΩ pullup), active low output (100 kΩ pullup) with a 180 ms typical pulse width. $\overline{\text{RESET}}$ is asserted whenever V_{CC} is below the reset threshold. It remains asserted for approximately 180 ms after V_{CC} rises above the reset threshold. Pin 14 also functions as an active low $\overline{\text{RESET}}$ input and resets all unlocked registers to their default values.	$\overline{\text{RESET}}$
15	D1+/+2.5V/+1.8V	D1+: Anode Connection to Thermal Diode 1. +2.5V: Monitors 2.5 V analog input. +1.8V: Monitors 1.8 V analog input.	D1+
16	D1−/SCSI_TERM1	D1−: Cathode Connection to Thermal Diode 1. SCSI_TERM1: Digital Input, SCSI Termination 1.	D1−
17	D2+	Anode Connection to Thermal Diode 2.	D2+
18	D2−	Cathode Connection to Thermal Diode 2.	D2−
19	D3+/+1.25V/+0.9V	D3+: Anode Connection to Thermal Diode 3. +1.25V: Monitors 1.25 V analog input. +0.9V: Monitors 0.9 V analog input.	D3+
20	D3−/SCSI_TERM2	D3−: Cathode connection to Thermal Diode 3. SCSI_TERM2: Digital Input, SCSI Termination 2.	D3−
21	TACH7/+5V	TACH7: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 7. +5V: Analog Input. Monitors 5.0 V power supply.	TACH7

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description	POR Default
22	TACH8/+12V3	TACH8: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 8. +12V3: Analog Input. Monitors 12 V Power Supply 3.	TACH8
23	V_{CCP1}/+1.5V/+1.8V/+2.5V	V_{CCP1}: Monitors 1.2 V analog input. +1.5V: Monitors 1.5 V analog input. +1.8V: Monitors 1.8 V analog input. +2.5V: Monitors 2.5 V analog input.	+1.8V
24	V_{CCP2}/+1.5V/+1.8V/+2.5V	V_{CCP2}: Monitors 1.2 V analog input. +1.5V: Monitors 1.5 V analog input. +1.8V: Monitors 1.8 V analog input. +2.5V: Monitors 2.5 V analog input.	+2.5V
25	VR_HOT1/+1.2V1/+3.3V	VR_HOT1: Digital Input Indicating Overtemperature Event on Voltage Regulator. +1.2V1: 0 V to 1.2 V Analog Input. For example, can be used to monitor G_{BIT}. +3.3V: Analog Input. Monitors 3.3 V power supply.	+3.3V
26	VR_HOT2/+1.2V2/V_{BATT}	VR_HOT2: Digital Input Indicating Overtemperature Event on Voltage Regulator. +1.2V2: 0 V to 1.2 V Analog Input. For example, can be used to monitor FSB_V_{TT}. V_{BATT}: Analog Input. Monitors battery voltage, nominally 3.0 V.	V_{BATT}
27	$\overline{\text{FAN2MAX}}$/CI	$\overline{\text{FAN2MAX}}$: Sets fan to maximum speed when a fan fault condition occurs. Bidirectional open drain, active low I/O. CI: An active high input that captures a chassis intrusion event in Bit 7 of the digital status register. This bit remains set until cleared, as long as battery voltage is applied to the V_{BATT} input, even when the ADT7462 is powered off.	CI
28	$\overline{\text{THERM1}}$/+1.5V1/GPIO7/VID6	$\overline{\text{THERM1}}$: Can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the Intel® Pentium® 4 processor to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes. +1.5V1: 0 V to 1.5 V Analog Input. Can be used to monitor ICH. GPIO7: Open-Drain I/O. General-purpose input/output. VID6: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97).	$\overline{\text{THERM1}}$
29	$\overline{\text{THERM2}}$/+1.5V2/GPIO8	$\overline{\text{THERM2}}$: Can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be connected to the $\overline{\text{PROCHOT}}$ output of the Intel® Pentium® 4 processor to time and monitor $\overline{\text{PROCHOT}}$ assertions. Can be used as an output to signal overtemperature conditions or for clock modulation purposes. +1.5V2: 0 V to 1.5 V Analog Input. Can be used to monitor 3GIO. GPIO8: Open-Drain I/O. General-purpose input/output.	$\overline{\text{THERM2}}$
30	PWM3	Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 3.	PWM3
31	VID4/GPIO5/PWM1	VID4: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO5: Open-Drain I/O. General-purpose input/output. PWM1: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 1.	PWM1
32	VID5/GPIO6/PWM2	VID5: Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read in to the VID value register (0x97). GPIO6: Open-Drain I/O. General-purpose input/output. PWM2: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse-width modulated output to control the speed of Fan 2.	PWM2

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments		Min	Typ	Max	Unit
Power Supply						
Supply Voltage			3.0	3.3	5.5	V
Supply Current, I_{CC}	ADC Active, Interface Inactive (Note 2)		−	1.5	4.0	mA
Temperature-to-Digital Converter	**T_A Conditions**	**V_{CC} Conditions**				
Internal Sensor, T_A, Accuracy	$0°C \le T_A \le 85°C$ $-40°C \le T_A \le +100°C$ $0°C \le T_A \le 85°C$ $-40°C \le T_A \le +100°C$	$3\ V \le V_{CC} \le 3.6\ V$ $3\ V \le V_{CC} \le 3.6\ V$ $4.5\ V \le V_{CC} \le 5.5\ V$ $4.5\ V \le V_{CC} \le 5.5\ V$	− − − −	±0.5 − − −	±2.25 ±3.25 ±3.0 ±4.0	°C
Resolution			−	−	0.25	°C
Remote Sensor, T_D, Accuracy ($-40°C \le T_D \le +125°C$)	$0°C \le T_A \le 85°C$ $-40°C \le T_A \le +100°C$ $0°C \le T_A \le 85°C$ $-40°C \le T_A \le +100°C$	$3\ V \le V_{CC} \le 3.6\ V$ $3\ V \le V_{CC} \le 3.6\ V$ $4.5\ V \le V_{CC} \le 5.5\ V$ $4.5\ V \le V_{CC} \le 5.5\ V$	− − − −	±0.5 − − −	±2.25 ±3.25 ±2.75 ±3.5	°C
Resolution			−	−	0.25	°C
Remote Sensor Source Current (Note 3)	High Level Mid Level Low Level		− − −	85 34 5.0	− − −	μA
Series Resistance Cancellation (Note 3)	The ADT7462 Cancels 2 kΩ in Series with the Remote Thermal Diode		−	2.0	−	kΩ
ANALOG−TO−DIGITAL CONVERTER						
Total Unadjusted Error, TUE (Note 4 and 5)			−	−	±3.5	%
Differential Non-linearity, DNL	8 Bits		−	−	±1.0	LSB
Conversion Time (Voltage Input) (Note 3)			−	8.53	9.86	ms
Conversion Time (Local Temperature) (Note 3)			−	9.01	10.38	ms
Conversion Time (Remote Temperature) (Note 3)			−	38.36	42.09	ms
INPUT RESISTANCE						
Pin 7, Pin 8, Pin 13, Pin 21, Pin 22, Pin 25, Pin 28, Pin 29	Attenuators Enabled		−	140	−	kΩ
Pin 15, Pin 19	Attenuators Enabled		−	225	−	kΩ
Pin 23, Pin 24	Attenuators Enabled		−	66	−	kΩ
Pin 26, V_{BATT} and +1.2V2 (When Measured)	Attenuators Cannot Be Disabled		100	120	140	kΩ
V_{BATT} Current Drain (When Measured)	CR2032 Battery Life > 10 Years		−	80	100	nA
V_{BATT} Current Drain (When Not Measured)	CR2032 Battery Life > 10 Years		−	16	−	nA
FAN RPM TO DIGITAL CONVERTER						
Accuracy			−	−	±8.0	%
Internal Clock Frequency			82.8	90	97.2	kHz
OPEN-DRAIN OUTPUTS (PWM, GPIO)						
High Level Output Leakage Current, I_{OH}	$V_{OUT} = V_{CC}$		−	0.1	±1.0	μA
Output Low Voltage, V_{OL}	$I_{OUT} = -3\ mA$, $V_{CC} = +3.3\ V$		−	−	0.4	V
DIGITAL OUTPUT ($\overline{RESET}$,$\overline{ALERT}$, $\overline{THERM}$)						
Output Low Voltage, V_{OL}	$I_{OUT} = -3\ mA$, $V_{CC} = +3.3\ V$		−	−	0.4	V
$\overline{RESET}$ Pulse Width (Note 3)			140	180	−	ms
$\overline{RESET}$ Threshold	Falling Voltage		3.0	3.05	3.1	V
$\overline{RESET}$ Hysteresis (Note 3)			−	70	−	mV

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPEN-DRAIN SERIAL BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −3 mA, V_{CC} = +3.3 V	−	−	0.4	V
High Level Output Leakage Current, I_{OH}	$V_{OUT} = V_{CC}$	−	0.1	±1.0	μA
SERIAL BUS DIGITAL INPUTS (SDA AND SCL)					
Input High Voltage, V_{IH}		2.1	−	−	V
Input Low Voltage, V_{IL}		−	−	0.8	V
Hysteresis		−	500	−	mV
DIGITAL INPUT LOGIC LEVELS (VID0 to VID6) AND $\overline{\text{THERM}}$, TACH, GPIO, VR_HOT, SCSI_TERM)					
Input High Voltage, V_{IH}	Bit 3 and Bit 4 of Configuration Register 3 = 0	1.7	−	−	V
Input Low Voltage, V_{IL}	Bit 3 and Bit 4 of Configuration Register 3 = 0	−	−	0.8	V
Input High Voltage, V_{IH} (VID0 to VID6)	Bit 3 of Configuration Register 3 = 1	0.65	−	−	V
Input High Voltage, V_{IH} ($\overline{\text{THERM}}$)	Bit 4 of Configuration Register 3 = 1	2/3 V_{CCP1}	−	−	V
Input Low Voltage, V_{IL}	Bit 3 and Bit 4 of Configuration Register 3 = 1	−	−	0.4	V
Hysteresis		−	500	−	mV
DIGITAL INPUT CURRENTS					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	−1.0	−	−	μA
Input Low Current, I_{IL}	V_{IN} = 0	−	−	+1.0	μA
Input Capacitance (Note 3)		−	5.0	−	pF
SERIAL BUS TIMING (Note 3)					
Clock Frequency	See Figure 2	−	−	400	kHz
Glitch Immunity, t_{SW}	See Figure 2	−	50	−	ns
Bus Free Time	See Figure 2	1.3	−	−	μs
Start Setup Time, $t_{SU;STA}$	See Figure 2	0.6	−	−	μs
Start Hold Time, $t_{HD;STA}$	See Figure 2	0.6	−	−	μs
SCL Low Time, t_{LOW}	See Figure 2	1.3	−	−	μs
SCL High Time, t_{HIGH}	See Figure 2	0.6	−	−	μs
SCL, SDA Rise Time, t_R	See Figure 2	−	−	1000	ns
SCL, SDA Fall Time, t_F	See Figure 2	−	−	300	ns
Data Setup Time, $t_{SU;DAT}$	See Figure 2	100	−	−	ns
Detect Clock Low Timeout	Can Be Optionally Enabled	−	25	−	ms

1. All voltages are measured with respect to GND, unless otherwise specified. Typical values are at T_A = 25°C and represent the most likely parametric norm. Logic inputs accept input high voltages up to 5.0 V, even when the device is operating at supply voltages below 5.0 V. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.0 V for a rising edge.
2. Unused digital inputs connected to GND.
3. Guaranteed by design, not production tested.
4. Note that this specification does not apply if Pin 26 (V_{BATT}, +1.2V) is being measured in single-channel mode. See Figure 16 in the Typical Performance Characteristics section for V_{BATT} accuracy.
5. For Pin 23 and Pin 24 configured as +1.8V or +2.5V only, restricted conditions of $V_{CC} \geq 3.3$ V and +25°C ≤ T_A ≤ +125°C apply.

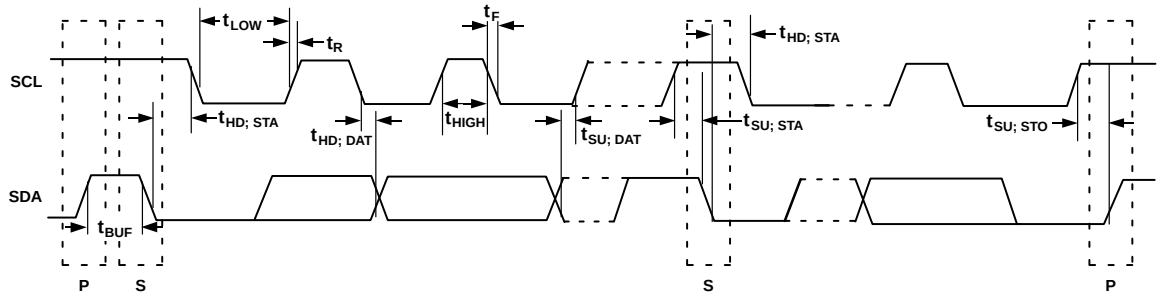


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

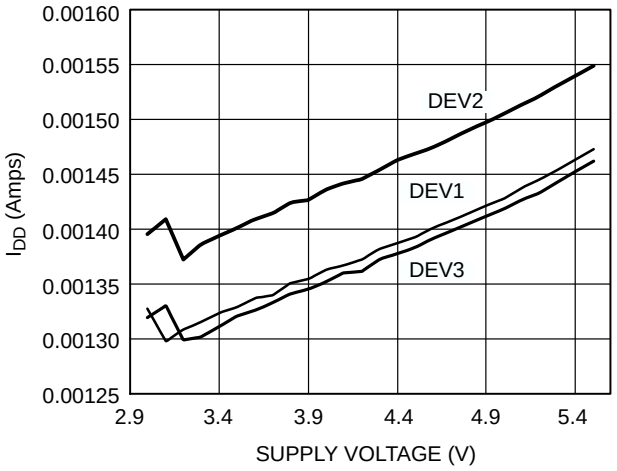


Figure 3. Supply Current vs. Supply Voltage

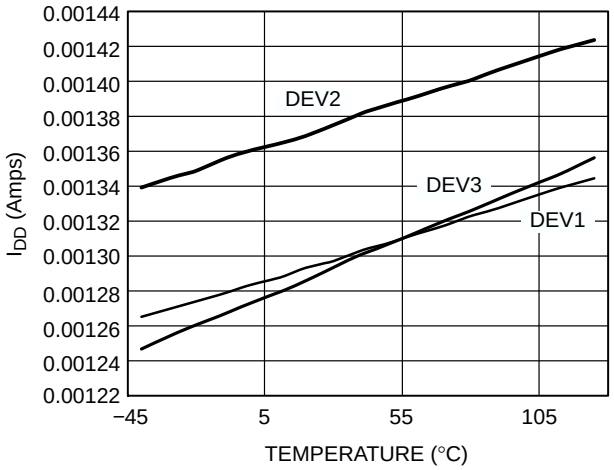


Figure 4. Supply Current vs. Temperature

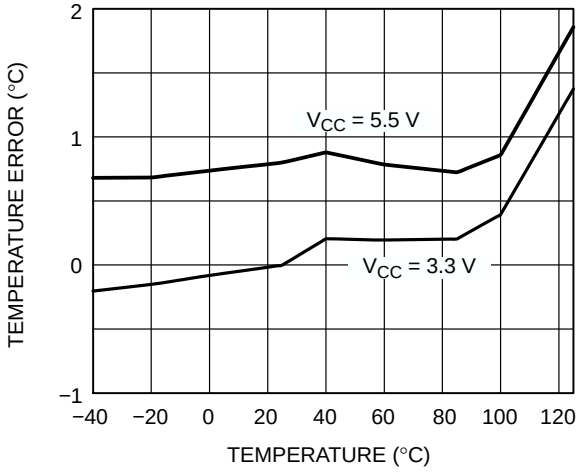


Figure 5. Local Sensor Temperature Error

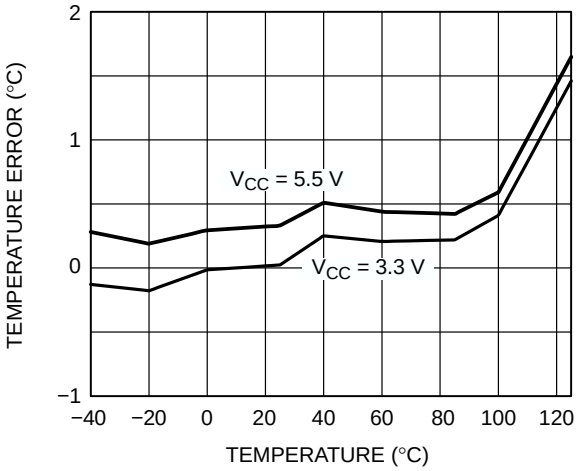


Figure 6. Remote Sensor Temperature Error

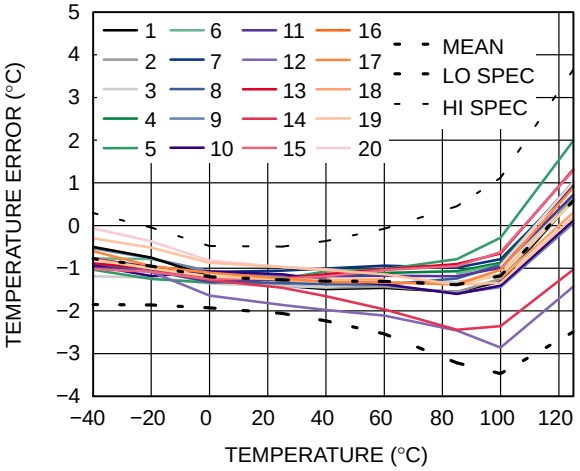


Figure 7. Temperature Error Measuring Intel Pentium® 4 Processor

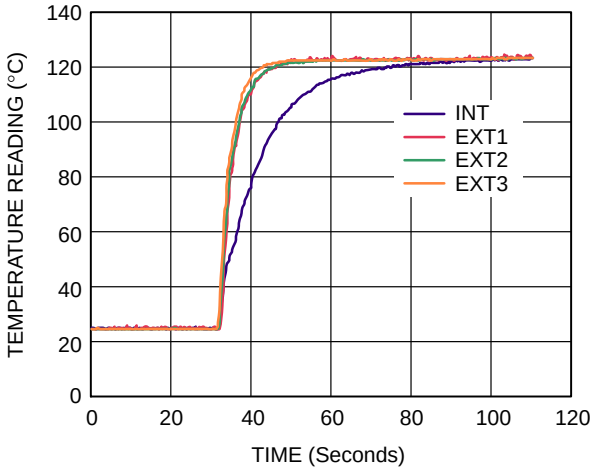


Figure 8. ADT7462 Response to Thermal Shock

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

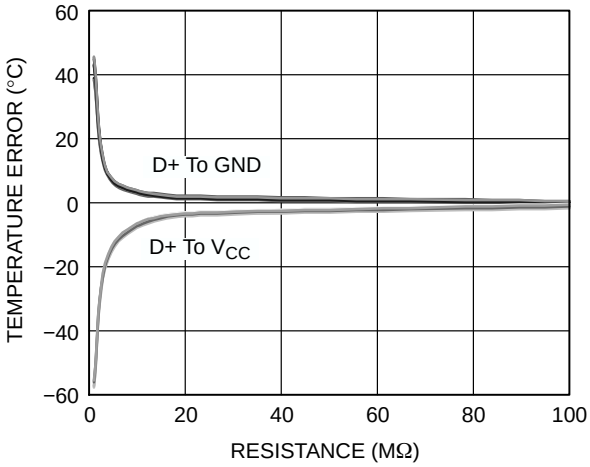


Figure 9. Remote Temperature Error vs. Resistance (SRC)

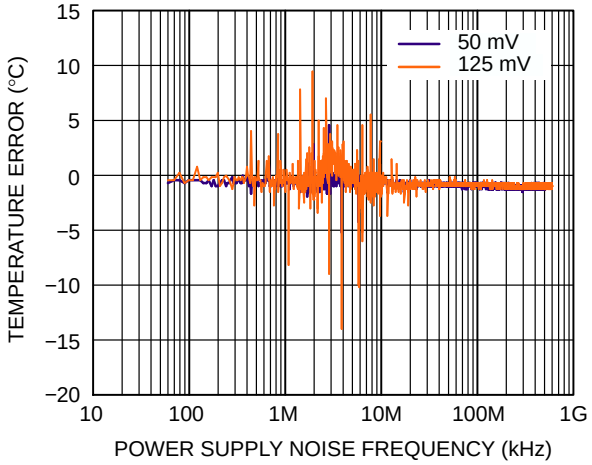


Figure 10. Local Temperature Error vs. Power Supply Noise Frequency

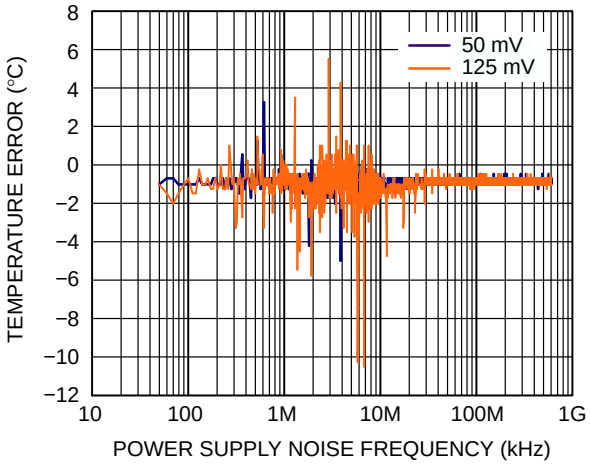


Figure 11. Remote Temperature Error vs. Power Supply Noise Frequency

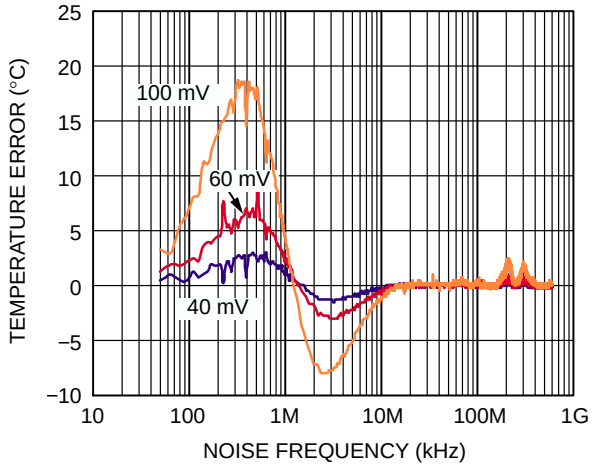


Figure 12. Remote Temperature Error vs. Common-Mode Noise Frequency

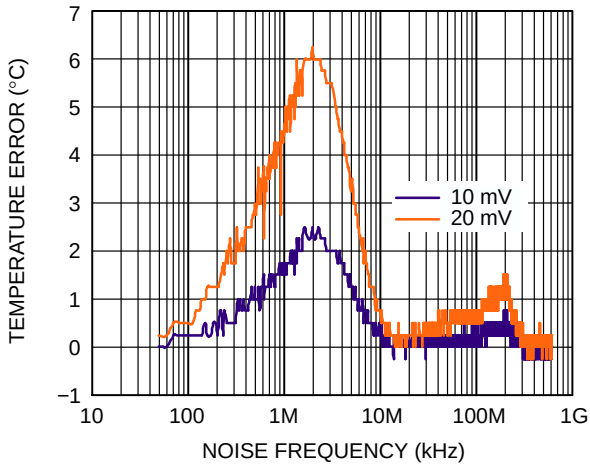


Figure 13. Remote Temperature Error vs. Differential-Mode Noise Frequency

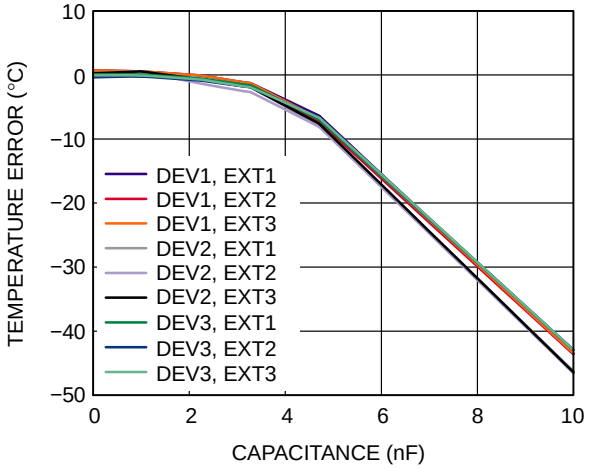


Figure 14. Remote Temperature Error vs. Capacitance Between D+ and D−

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

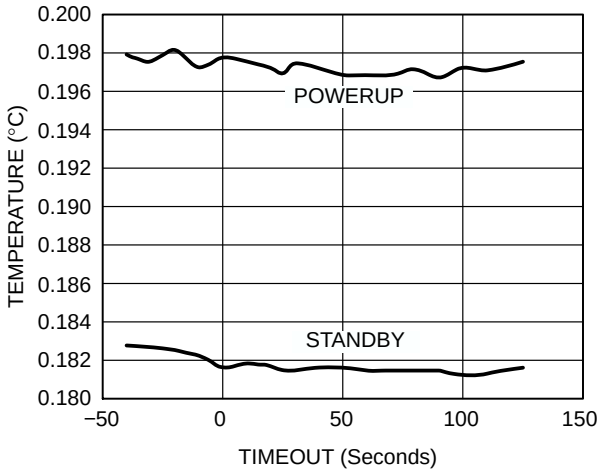


Figure 15. Local Temperature vs. Power-On Reset Timeout

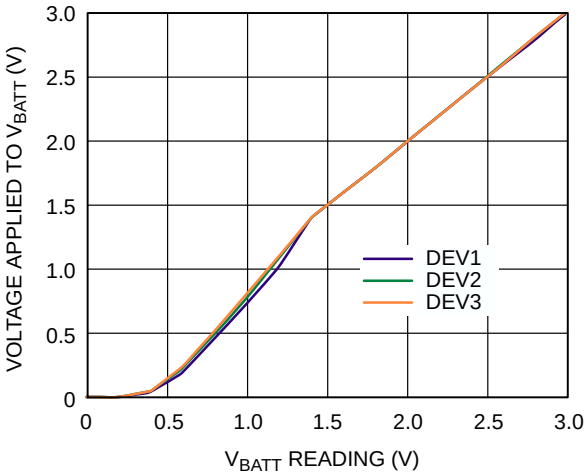


Figure 16. Applied Voltage vs. V_{BATT} Reading

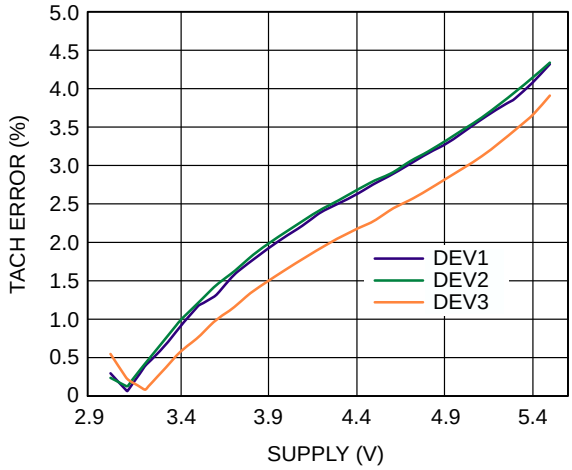


Figure 17. TACH Accuracy vs. Supply Voltage

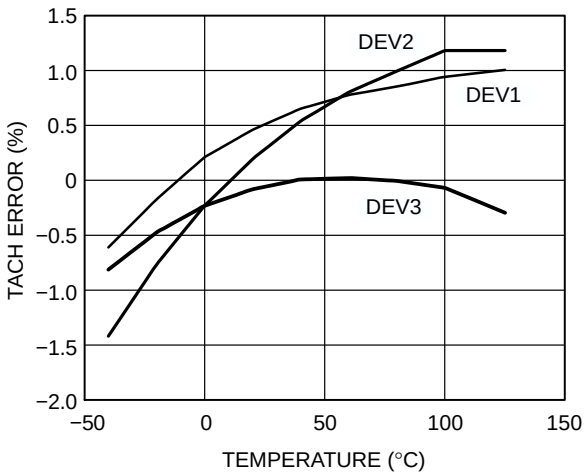


Figure 18. TACH Accuracy vs. Temperature

Function Description: Easy Configuration Options

There are a number of multifunctional pins on the ADT7462 that need to be configured on powerup to suit the desired application. Note that due to the large number of pins that need to be configured, it could take several SMBus transactions to achieve the required configuration. For this reason, the ADT7462 has five easy configuration options. The user sets a bit in the easy configuration option register (0x14) to set up the required configuration (see Table 5).

Table 5. EASY CONFIGURATION REGISTER SETTINGS

Easy Configuration Option	Register 0x14 Setting
Option 1	Bit 0 = 1
Option 2	Bit 1 = 1
Option 3	Bit 2 = 1
Option 4	Bit 3 = 1
Option 5	Bit 4 = 1

Once the most convenient easy configuration option has been set, the user can configure any of the pins individually. The setup complete bit (Bit 5 of Register 0x01) must then be set to 1 to indicate that the ADT7462 is configured correctly, and then monitoring of the selected channels begins.

The following is a detailed description of the five easy configuration options that are available.

Configuration Option 1

Configuration Option 1 is the default configuration. It is also the most suitable for thermal monitoring, voltage monitoring, and fan control for single and dual processor systems. Features of Configuration Option 1 include the following:

- One Local and Three Remote Temperature Channels
- Four PWM Drives and Eight TACH Inputs
- Two $\overline{\text{THERM}}$ I/Os
- Voltage Monitoring
- +3.3V
- +2.5V
- +1.8V
- V_{BATT}
- $\overline{\text{RESET}}$ I/O
- CI (Chassis Intrusion) or $\overline{\text{FAN2MAX}}$

Figure 19 shows the pin configuration when Configuration Option 1 is chosen.

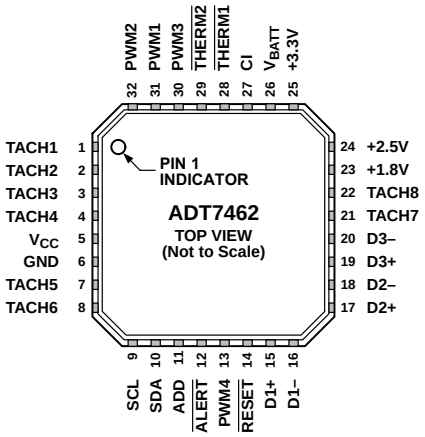


Figure 19. Configuration Option 1

Table 6. CONFIGURATION OPTION 1

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	TACH5	Pin Configuration Reg 1	Bit 0 = 1
8	TACH6	Pin Configuration Reg 2	Bit 7 = 1
13	PWM4	Pin Configuration Reg 2	Bit 6 = 1
15	D1+	Pin Configuration Reg 1	Bit 6 = 1
16	D1−	Pin Configuration Reg 1	Bit 6 = 1
19	D3+	Pin Configuration Reg 1	Bit 5 = 1
20	D3−	Pin Configuration Reg 1	Bit 5 = 1
21	TACH7	Pin Configuration Reg 2	Bit 3 = 1
22	TACH8	Pin Configuration Reg 2	Bit 2 = 1
23	+1.8V	Pin Configuration Reg 2	Bits [1:0] = 10
24	+2.5V	Pin Configuration Reg 3	Bits [7:6] = 01
25	+3.3V	Pin Configuration Reg 3	Bits [5:4] = 00
26	V_{BATT}	Pin Configuration Reg 3	Bits [3:2] = 00
27	CI	Pin Configuration Reg 3	Bit 1 = 1
28†	$\overline{\text{THERM1}}$	Pin Configuration Reg 4	Bits [7:6] = 1×
29	$\overline{\text{THERM2}}$	Pin Configuration Reg 4	Bits [5:4] = 1×
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

Configuration Option 2

Configuration Option 2 is used for thermal monitoring and fan control for Processor 1 and Processor 2 in a dual processor system. It can also monitor one set of VIDs, if required. Features of Configuration Option 2 include the following:

- One Local and Three Remote Thermal Channels
- Up to Four PWM Drives and Up to Eight TACH Inputs (VID Pins and TACHs/PWMs are Muxed Together)
- Two $\overline{\text{THERM}}$ I/Os
- Two VRD Inputs
- $\overline{\text{RESET}}$ I/O
- Two V_{CCP} Voltage Monitoring Channels

Figure 20 shows the pin configuration when Configuration Option 2 is chosen.

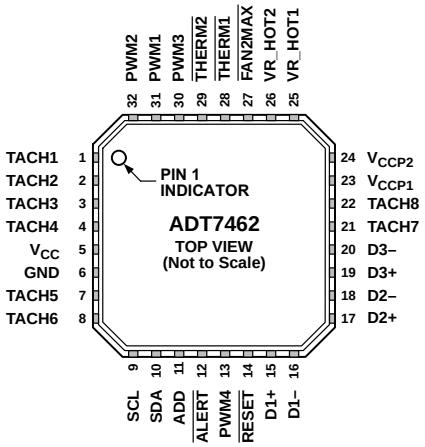


Figure 20. Configuration Option 2

Table 7. CONFIGURATION OPTION 2

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	TACH5	Pin Configuration Reg 1	Bit 0 = 1
8	TACH6	Pin Configuration Reg 2	Bit 7 = 1
13	PWM4	Pin Configuration Reg 2	Bit 6 = 1
15	D1+	Pin Configuration Reg 1	Bit 6 = 1
16	D1−	Pin Configuration Reg 1	Bit 6 = 1
19	D3+	Pin Configuration Reg 1	Bit 5 = 1
20	D3−	Pin Configuration Reg 1	Bit 5 = 1
21	TACH7	Pin Configuration Reg 2	Bit 3 = 1
22	TACH8	Pin Configuration Reg 2	Bit 2 = 1
23	V_{CCP1}	Pin Configuration Reg 2	Bits [1:0] = 00
24	V_{CCP2}	Pin Configuration Reg 3	Bits [7:6] = 00
25	VR_HOT1	Pin Configuration Reg 3	Bits [5:4] = 1×
26	VR_HOT2	Pin Configuration Reg 3	Bits [3:2] = 1×
27	$\overline{\text{FAN2MAX}}$	Pin Configuration Reg 3	Bit 1 = 0
28†	$\overline{\text{THERM1}}$	Pin Configuration Reg 4	Bits [7:6] = 1×
29	$\overline{\text{THERM2}}$	Pin Configuration Reg 4	Bits [5:4] = 1×
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

Configuration Option 3

Configuration Option 3 is used to monitor all the voltages in the system for Processor 1 and Processor 2. Additional pins can be configured for fan control, VIDs, or GPIOs, as required. Features of Configuration Option 3 include the following:

- Up to 13 Different Voltages Monitored
- Three +12V
- +5V
- +3.3V
- +2.5V
- +1.8V
- Two +1.5V
- Two +1.2V (V_{CCP1}, V_{CCP2})
- 0.9V
- V_{BATT}
- One Local and One Remote Temperature Channels
- Up to Three PWM Drives and Up to Four TACH Inputs
- $\overline{\text{RESET}}$ I/O

Figure 21 shows the pin configuration when Configuration Option 3 is chosen.

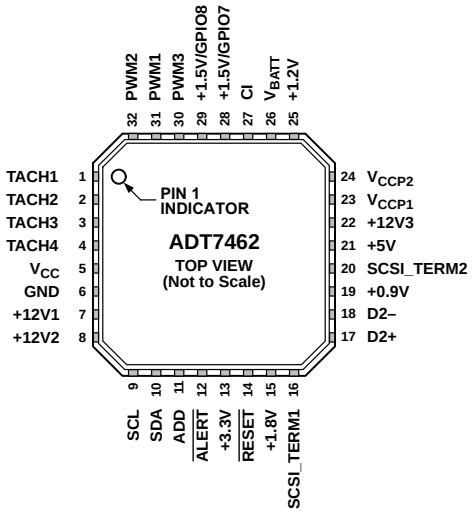


Figure 21. Configuration Option 3

Table 8. CONFIGURATION OPTION 3

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	+12V1	Pin Configuration Reg 1	Bit 0 = 0
8	+12V2	Pin Configuration Reg 2	Bit 7 = 0
13	+3.3V	Pin Configuration Reg 2	Bit 6 = 0
15	+1.8V	Pin Configuration Reg 1	Bit 6 = 0
16	SCSI_ TERM1	Pin Configuration Reg 1	Bit 6 = 0
19	+0.9V	Pin Configuration Reg 1	Bit 5 = 0
20	SCSI_ TERM2	Pin Configuration Reg 1	Bit 5 = 0
21	+5V	Pin Configuration Reg 2	Bit 3 = 0
22	+12V3	Pin Configuration Reg 2	Bit 2 = 0
23	V_{CCP1}	Pin Configuration Reg 2	Bits [1:0] = 00
24	V_{CCP2}	Pin Configuration Reg 3	Bits [7:6] = 00
25	+1.2V	Pin Configuration Reg 3	Bits [5:4] = 01
26	V_{BATT}	Pin Configuration Reg 3	Bits [3:2] = 00
27	CI	Pin Configuration Reg 3	Bit 1 = 1
28†	+1.5V/ GPIO7	Pin Configuration Reg 4	Bits [7:6] = 01
29	+1.5V/ GPIO8	Pin Configuration Reg 4	Bits [5:4] = 01
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

Configuration Option 4

Configuration Option 4 is used to monitor temperature, voltages, and fans for Processor 1 in a dual processor system. Features of Configuration Option 4 include the following:

- One Local and Two Remote Temperature Channels
- Up to Four PWM Drives and Six TACH Inputs
- Up to Eight Voltages Monitored
- +12V
- +5V
- +3.3V
- Two +1.5V
- +1.2V (V_{CCP1})
- +0.984V (Mem_V_{TT})
- V_{BATT}
- $\overline{\text{THERM}}$ I/O
- VRD Input
- $\overline{\text{RESET}}$ I/O

Figure 22 shows the pin configuration when Configuration Option 4 is chosen.

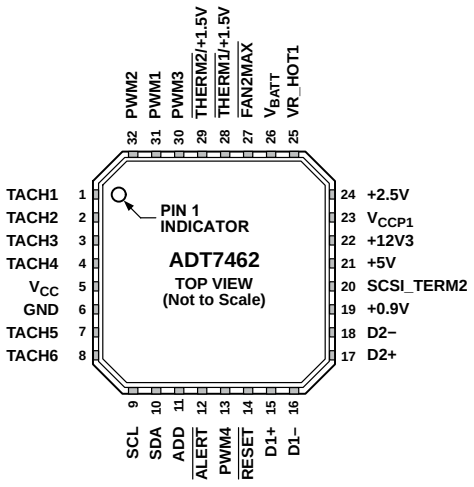


Figure 22. Configuration Option 4

Table 9. CONFIGURATION OPTION 4

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	TACH5	Pin Configuration Reg 1	Bit 0 = 1
8	TACH6	Pin Configuration Reg 2	Bit 7 = 1
13	PWM4	Pin Configuration Reg 2	Bit 6 = 1
15	D1+	Pin Configuration Reg 1	Bit 6 = 1
16	D1−	Pin Configuration Reg 1	Bit 6 = 1
19	+0.9V	Pin Configuration Reg 1	Bit 5 = 0
20	SCSI_ TERM2	Pin Configuration Reg 1	Bit 5 = 0
21	+5V	Pin Configuration Reg 2	Bit 3 = 0
22	+12V3	Pin Configuration Reg 2	Bit 2 = 0
23	V_{CCP1}	Pin Configuration Reg 2	Bits [1:0] = 00
24	+2.5V	Pin Configuration Reg 3	Bits [7:6] = 01
25	VR_HOT1	Pin Configuration Reg 3	Bits [5:4] = 1×
26	V_{BATT}	Pin Configuration Reg 3	Bits [3:2] = 00
27	$\overline{\text{FAN2MAX}}$	Pin Configuration Reg 3	Bit 1 = 0
28 †*	$\overline{\text{THERM1}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
29*	$\overline{\text{THERM2}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

*It is not possible to configure +1.5V monitoring on Pin 29 and $\overline{\text{THERM1}}$ on Pin 28. Pin 28 must both be configured as either +1.5V monitoring or as $\overline{\text{THERM}}$ I/O (see Table 51).

Configuration Option 5

Configuration Option 5 is used to monitor temperature, voltages, and fans for Processor 2 in a dual processor system. Features of Configuration Option 5 include the following:

- One Local and Two Remote Temperature Channels
- Up to Three PWM Drives and Up to Six TACH Inputs
- Voltage Monitoring
- Two +12V
- +3.3V
- Mem_Core (+1.969V)
- +1.8 V
- Two +1.5V
- +1.2V (V_{CCP2})
- $\overline{\text{RESET}}$ I/O

Figure 23 shows the pin configuration when Configuration Option 5 is chosen.

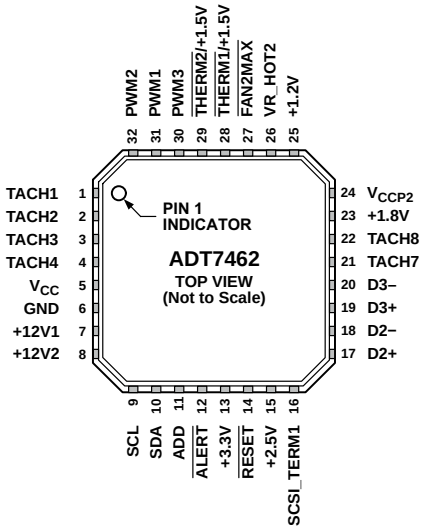


Figure 23. Configuration Option 5

Table 10. CONFIGURATION OPTION 5

Pin	Function	Configuration Register	Bit Value
1†	TACH1	Pin Configuration Reg 1	Bit 4 = 1
2†	TACH2	Pin Configuration Reg 1	Bit 3 = 1
3†	TACH3	Pin Configuration Reg 1	Bit 2 = 1
4†	TACH4	Pin Configuration Reg 1	Bit 1 = 1
7	+12V1	Pin Configuration Reg 1	Bit 0 = 0
8	+12V2	Pin Configuration Reg 2	Bit 7 = 0
13	+3.3V	Pin Configuration Reg 2	Bit 6 = 0
15	+2.5V	Pin Configuration Reg 1	Bit 6 = 0
16	SCSI_ TERM1	Pin Configuration Reg 1	Bit 6 = 0
19	D3+	Pin Configuration Reg 1	Bit 5 = 1
20	D3−	Pin Configuration Reg 1	Bit 5 = 1
21	TACH7	Pin Configuration Reg 2	Bit 3 = 1
22	TACH8	Pin Configuration Reg 2	Bit 2 = 1
23	+1.8V	Pin Configuration Reg 2	Bits [1:0] = 10
24	V_{CCP2}	Pin Configuration Reg 3	Bits [7:6] = 00
25	+1.2V	Pin Configuration Reg 3	Bits [5:4] = 01
26	VR_HOT2	Pin Configuration Reg 3	Bits [3:2] = 1×
27	$\overline{\text{FAN2MAX}}$	Pin Configuration Reg 3	Bit 1 = 0
28 †*	$\overline{\text{THERM1}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
29*	$\overline{\text{THERM2}}$/ $\overline{+1.5\text{V}}$	Pin Configuration Reg 4	See Table 51
31†	PWM1	Pin Configuration Reg 4	Bit 3 = 1
32†	PWM2	Pin Configuration Reg 4	Bit 2 = 1

†If VIDs are selected, these pins are configured as VIDs. To enable VIDs, set Bit 7 of Pin Configuration Register 1 (0x10) = 1.

*It is not possible to configure +1.5V monitoring on Pin 29 and $\overline{\text{THERM1}}$ on Pin 28. Pin 28 must both be configured as either +1.5V monitoring or as $\overline{\text{THERM}}$ I/O (see Table 51).

Serial Bus Interface

The ADT7462 is controlled through use of the serial system management bus (SMBus). The ADT7462 is connected to this bus as a slave device, under the control of a master controller. The SMBus interface in the ADT7462 is fully SMBus 1.1 and SMBus 1.0 compliant. The SMBus address is determined by the state of the ADD input on powerup.

ADD Input

The ADD pin is a three-state input to the ADT7462. It is used to determine the SMBus address used. This pin is sampled on powerup only. Any changes subsequent to powerup are not reflected until the ADT7462 is powered down and back up again. The corresponding 7-bit SMBus address for the state of the ADD pin is shown in Table 11.

Table 11. CORRESPONDING SMBUS ADDRESSES FOR ADD INPUT

ADD Pin	SMBus Version	SMBus Address
High	N/A	N/A
Float	SMBus 1.1	0x5C
Low	SMBus 1.1	0x58

SMBus Fixed Address

The ADT7462 supports SMBus fixed address mode and is fully backward compatible with SMBus 1.1 and SMBus 1.0. The ADT7462 powers up with a fixed SMBus address that cannot be changed by the assign address call. The fixed address is set by the state of the ADD input pin on powerup. The ADT7462 also responds to the SMBus device default address of 0x61.

SMBus Operation

The SMBus specification defines specific conditions for different types of read and write operations. The general SMBus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, that is, whether data is written to or read from the slave device.
2. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the 9th clock pulse, known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from it or written to it. If the R/$\overline{W}$ bit = 0, the master writes to the slave device. If the R/$\overline{W}$ bit = 1, the master reads from the slave device.
3. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
4. When all data bytes have been read or written, stop conditions are established. In write mode, the master releases the data line during the 10th clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the 9th clock pulse. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse and then takes it high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

For the ADT7462, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or to read data from it, the address pointer register must be set so that the correct data register is addressed. Then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 24. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities.

- If the ADT7462 address pointer register value is unknown or not the desired value, it must be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7462 as before, but only the data byte containing the register address is sent because no data is written to the register (see Figure 25).
  A read operation is then performed, consisting of the serial bus address and the R/$\overline{W}$ bit set to 1, followed by

the data byte read from the data register (see Figure 26).

- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register (see Figure 26).

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value.

However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7462 also supports the read byte protocol (see System Management Bus Specifications Rev. 2.0 for more information).

If several read or write operations must be performed in succession, then the master can send a repeat start condition, instead of a stop condition, to begin a new operation.

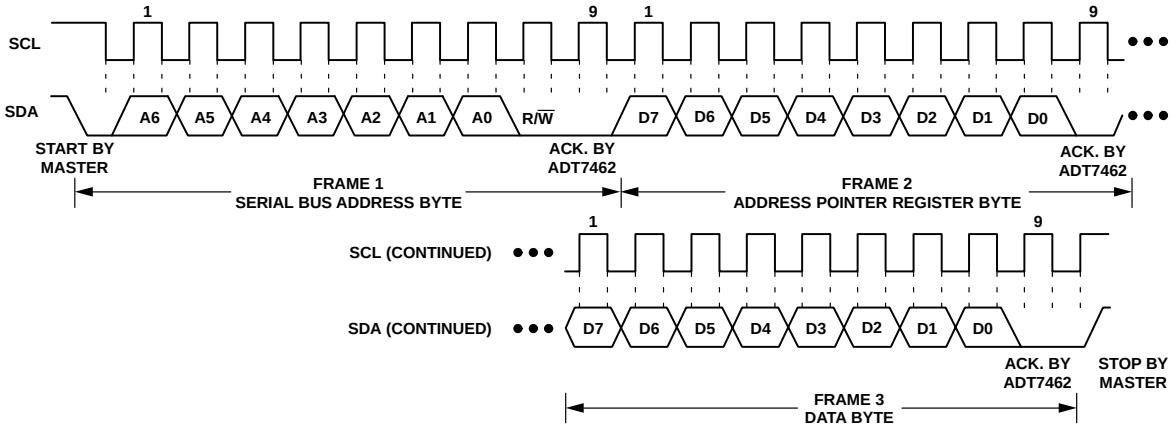


Figure 24. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

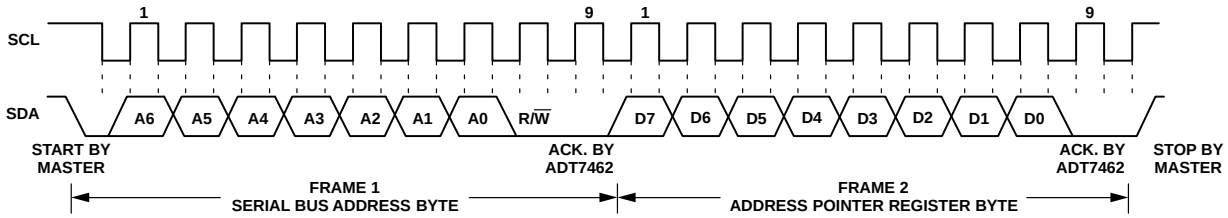


Figure 25. Writing to the Address Pointer Register Only

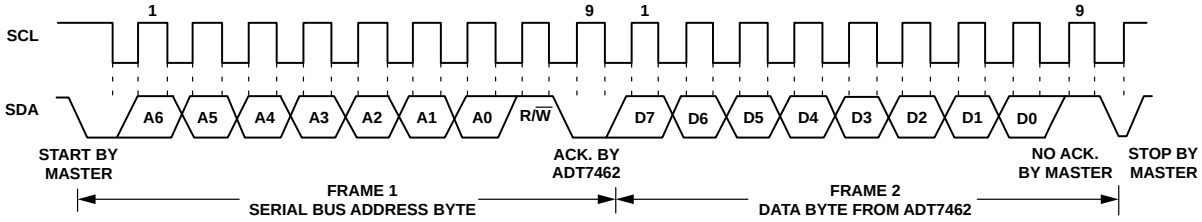


Figure 26. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7462 are discussed below. The following abbreviations are used in the diagrams:

- S − Start
- P − Stop
- R − Read
- W − Write
- A − Acknowledge
- $\overline{A}$ − No Acknowledge

The ADT7462 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code.
5. The slave asserts an ACK on SDA.
6. The master asserts a stop condition on SDA to end the transaction.

For the ADT7462, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This operation is shown in Figure 27.

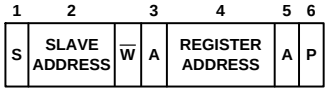


Figure 27. Setting a Register Address for Subsequent Read

If it is required to read data from the register immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code.
5. The slave asserts an ACK on SDA.
6. The master sends a data byte.
7. The slave asserts an ACK on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

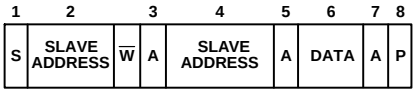


Figure 28. Single-byte Write to a Register

Block Write

In this operation, the master device writes a block of data to a slave device. The start address for a block write must be set previously. In the case of the ADT7462, this is done by a send byte operation to set a RAM address. The user writes the number of registers to be written to in the block read command to the #Bytes bits of the Configuration 0 register.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block write. The ADT7462 command code for a block write is 0xA0 (1010 0000).
5. The slave asserts an ACK on SDA.
6. The master sends the data bytes (the number of data bytes sent is written to the #Bytes bits of the Configuration 0 register).
7. The slave asserts an ACK on SDA after each data byte.
8. The master sends a packet error checking (PEC) byte.
9. The ADT7462 checks the PEC byte and issues an ACK, if correct. If incorrect (NO ACK), the master resends the data bytes.
10. The master asserts a stop condition on SDA to end the transaction.

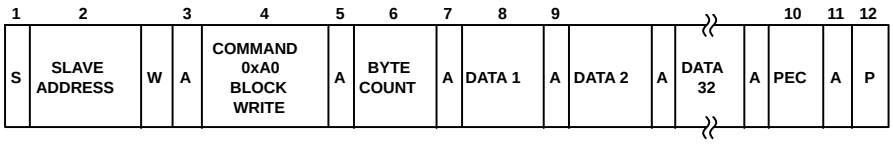


Figure 29. Block Write to ADT7462

Read Operations

The ADT7462 uses the following SMBus read protocols.

Receive Byte

The receive byte is useful when repeatedly reading a single register. The register address must be set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an ACK on SDA.
4. The master receives a data byte.
5. The master asserts a NO ACK on SDA.
6. The master asserts a stop condition on SDA to end the transaction.

For the ADT7462, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write a byte operation.

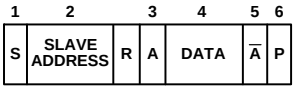


Figure 30. Single-byte Read from a Register

Block Read

In this operation, the master device reads a block of data from a slave device. The start address for a block read must be set previously, as well as the number of bytes to be read (maximum = 32). In the case of the ADT7462, the start address is activated by a send byte operation to set a RAM address. The number of bytes to be read should be written to the #Bytes bits in the Configuration 0 register. The block read operation consists of a send byte operation that sends a block read command to the slave, immediately followed by a repeated start and a read operation that reads out multiple data bytes, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block read. The ADT7462 command code for a block read is 0xA1 (1010 0001).
5. The slave asserts an ACK on SDA.
6. The master asserts a repeat start condition on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts an ACK on SDA.
9. The ADT7462 sends a byte count telling the master how many data bytes to expect. The maximum number of bytes is 32.
10. The master asserts an ACK on SDA.
11. The master receives the expected number of data bytes.
12. The master asserts an ACK on SDA after each data byte.
13. The ADT7462 issues a PEC byte to the master. The master should check the PEC byte and issue another block read if the PEC byte is incorrect.
14. A NO ACK is generated after the PEC byte to signal the end of the read.
15. The master asserts a stop condition on SDA to end the transaction.

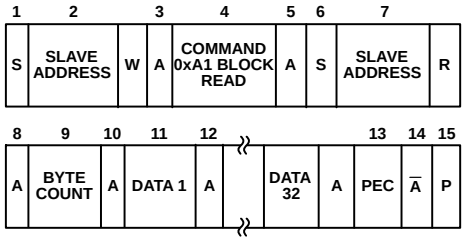


Figure 31. Block Read from RAM

Note that although the ADT7462 supports packet error checking (PEC), its use is optional. The PEC byte is calculated using CRC−8. The frame check sequence (FCS) conforms to CRC−8 by the polynomial.

$$C(x) = x^8 + x^2 + x + 1$$

Consult the SMBus 1.1 specifications for more information.

Alert Response Address

Alert Response Address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the ARA, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7462 has responded to the ARA, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBus Timeout

The ADT7462 includes an SMBus timeout feature. If there is no SMBus activity for 25 ms, the ADT7462 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus while the device is expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 3 (0x03)

Bit 1 SCL_Timeout = 1; SCL Timeout Enabled

Bit 1 SCL_Timeout = 0; SCL Timeout Disabled (Default)

Bit 2 SDA_Timeout = 1; SDA Timeout Enabled

Bit 2 SDA_Timeout = 0; SDA Timeout Disabled (Default)

Temperature and Voltage Measurement

Temperature Measurement

The ADT7462 can measure its own ambient temperature and the temperature of up to three remote thermal diodes. These diodes can be discrete diode-connected 2N3904/2N3906s or they can be located on a processor die. Figure 32 shows how to connect a remote NPN or PNP transistor.

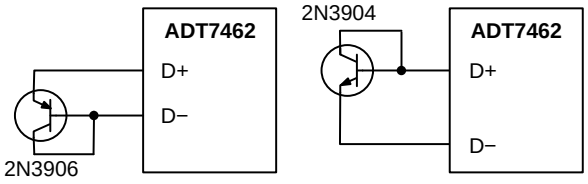


Figure 32. How to Measure Temperature Using Discrete Transistors

Remote Thermal Diode 1 connects to Pin 15 and Pin 16.

Remote Thermal Diode 2 connects to Pin 17 and Pin 18.

Remote Thermal Diode 3 connects to Pin 19 and Pin 20.

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor, operated at constant current. Unfortunately, this technique requires calibration to cancel the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the ADT7462 is to measure the change in V_{BE} when the device is operated at three different currents. Previous devices have used only two operating currents; use of a third current allows automatic cancellation of any resistances in series with the external temperature sensor.

Figure 33 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded and should be linked to the base. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input. C1 can optionally be added as a noise filter (recommended maximum value 1000 pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section.

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. As shown in Figure 33, N1 × I and N2 × I are different multiples of the Current I. The currents through the temperature diode are switched between I and N1 × I, giving ΔV_{BE1}, and then between I and N2 × I, giving ΔV_{BE2}. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also be shown to cancel the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then to a chopper-stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles for low conversion rates.

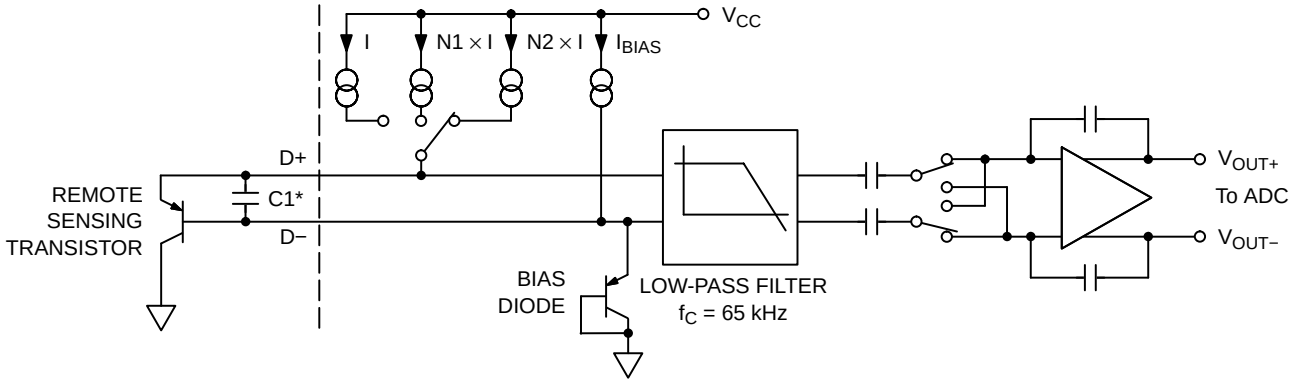
Signal conditioning and measurement of the internal temperature sensor are performed in the same manner (see Figure 33).

Temperature Measurement Results

The results of the local and remote temperature measurements are stored in the local and remote temperature value registers and are compared with limits programmed into the local and remote high and low limit registers.

Table 12. TEMPERATURE MEASUREMENT REGISTERS

Temperature Value	Register Address
Local Temperature, LSB	Register 0x88, Bits [7:6]
Local Temperature, MSB	Register 0x89
Remote 1 Temperature, LSB	Register 0x8A, Bits [7:6]
Remote 1 Temperature, MSB	Register 0x8B
Remote 2 Temperature, LSB	Register 0x8C, Bits [7:6]
Remote 2 Temperature, MSB	Register 0x8D
Remote 3 Temperature, LSB	Register 0x8E, Bits [7:6]
Remote 3 Temperature, MSB	Register 0x8F



*CAPACITOR C1 IS OPTIONAL. IT SHOULD ONLY BE USED IN NOISY ENVIRONMENTS.

Figure 33. Input Signal Conditioning

The temperature value is stored in two registers. The MSB has a resolution of 1°C. Only two bits in the temperature LSB register are used, Bit 7 and Bit 6, giving a temperature measurement resolution of 0.25°C. The temperature measurement range for both local and remote measurements is from −64°C to +191°C. However, the ADT7462 itself should never be operated outside its operating temperature range, which is from −40°C to +125°C. For the remote diode, the user should refer to the data sheet of the diode.

Table 13. TEMPERATURE DATA FORMAT

Temperature Value	MSB	LSB
−64°C	0000 0000	0000 0000
−50.25°C	0000 1110	0100 0000
−25°C	0010 0111	0000 0000
0°C	0100 0000	0000 0000
+25°C	0101 1001	0000 0000
+50.25°C	0111 0010	0100 0000
+100°C	1010 0100	0000 0000

When reading the full temperature value, the LSB should be read first and then the MSB. Reading the LSBs causes the current MSBs to be frozen until they are read. Reading the MSBs only does not cause any register to be locked. This is useful when a temperature reading with 1°C resolution is required.

Series Resistance Cancellation

Parasitic resistance in series with the remote diode D+ and D− inputs can be caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.8°C offset per ohm of parasitic resistance in series with the remote diode.

The ADT7462 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The ADT7462 is designed to automatically cancel typically up to 2 kΩ of resistance. By using an advanced temperature measurement method, the process is transparent to the user. This feature also allows an RCR filter to be added to the sensor path, allowing the part to be used accurately in noisy environments.

Temperature Limits

Each temperature measurement channel has a high and low temperature limit associated with it. The temperature measurements are compared with these limits, and the results of these comparisons are stored in status registers. A Logic 0 indicates an in-limit comparison, and a Logic 1 indicates an out-of-limit comparison. The ADT7462 can generate an $\overline{\text{ALERT}}$, if configured to do so, after a status bit is set. For more information on the status registers and $\overline{\text{ALERT}}$, see the Status and Mask Registers $\overline{\text{ALERT}}$ section.

Each temperature channel also has a $\overline{\text{THERM1}}$ and a $\overline{\text{THERM2}}$ temperature limit associated with it. When these temperature limits are exceeded, the corresponding $\overline{\text{THERM}}$ pin is asserted low (if $\overline{\text{THERM}}$ is configured as an output), and the fans are boosted to full speed (if the boost bit is set). Table 14 shows a complete list of all the temperature limits and their default values.

Table 14. TEMPERATURE LIMIT REGISTERS

Temperature Value	Register Address	Default
Local Low Temperature Limit	0x44	0x40
Remote 1 Low Temperature Limit	0x45	0x40
Remote 2 Low Temperature Limit	0x46	0x40
Remote 3 Low Temperature Limit	0x47	0x40
Local High Temperature Limit	0x48	0x95
Remote 1 High Temperature Limit	0x49	0x95
Remote 2 High Temperature Limit	0x4A	0x95
Remote 3 High Temperature Limit	0x4B	0x95
Local $\overline{\text{THERM1}}$ Temperature Limit	0x4C	0xA4
Remote 1 $\overline{\text{THERM1}}$ Temperature Limit	0x4D	0xA4
Remote 2 $\overline{\text{THERM1}}$ Temperature Limit	0x4E	0xA4
Remote 3 $\overline{\text{THERM1}}$ Temperature Limit	0x4F	0xA4
Local $\overline{\text{THERM2}}$ Temperature Limit	0x50	0xA4
Remote 1 $\overline{\text{THERM2}}$ Temperature Limit	0x51	0xA4
Remote 2 $\overline{\text{THERM2}}$ Temperature Limit	0x52	0xA4
Remote 3 $\overline{\text{THERM2}}$ Temperature Limit	0x53	0xA4

Offset Registers

The ADT7462 has temperature offset registers at Register 0x56 to Register 0x59 for the local, Remote 1, Remote 2, and Remote 3 temperature channels. By doing a one-time calibration of the system, the user can determine the offset caused by system board noise and cancel it using the offset registers. The offset registers automatically add a twos complement, 8-bit reading to every temperature measurement. The LSBs add 0.5°C offset to the temperature reading so the 8-bit register effectively allows temperature offsets of up to ±64°C with a resolution of 0.5°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Temperature Offset Registers

Register 0x56 Local Temperature Offset = 0x00 (0°C Default)

Register 0x57 Remote 1 Temperature Offset = 0x00 (0°C Default)

Register 0x58 Remote 2 Temperature Offset = 0x00 (0°C Default)

Register 0x59 Remote 3 Temperature Offset = 0x00 (0°C Default)

Layout Considerations

Digital boards can be electrically noisy environments. The ADT7462 measures very small voltages from the remote sensor, so care must be taken to minimize noise induced at the sensor inputs. The following precautions should be taken:

- Place the ADT7462 as close as possible to the remote sensing diode. Provided that the worst noise sources, such as clock generators, data/address buses, and CRTs, are avoided, this distance can be 4 inches to 8 inches.
- Route the D+ and D− tracks close together, in parallel, with grounded guard tracks on each side. To minimize inductance and reduce noise pickup, a 5 mil track width and spacing is recommended. If possible, provide a ground plane under the tracks.

Figure 34. Typical Arrangement of Signal Tracks

- Minimize the number of copper/solder joints that can cause thermo-couple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D− path and at the same temperature.
- Thermocouple effects should not be a major problem because 1°C corresponds to about 200 mV, and thermocouple voltages are about 3 mV/°C of temperature difference. Unless there are two thermocouples with a large temperature differential between them, thermocouple voltages should be much less than 200 mV.
- Place a 0.1 μF bypass capacitor close to the V_{CC} pin. In extremely noisy environments, an input filter capacitor can be placed across D+ and D− close to the ADT7462. This capacitance can affect the temperature measurement, so care must be taken to ensure that any capacitance seen at D+ and D− is a maximum of 1000 pF. This maximum value includes the filter capacitance, plus any cable or stray capacitance between the pins and the sensor diode.
- If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This works from about 6 feet up to 12 feet.
- For really long distances (up to 100 feet), use shielded twisted pair, such as Belden No. 8451 microphone cable. Connect the twisted pair to D+ and D− and the shield to GND close to the ADT7462. Leave the remote end of the shield unconnected to avoid ground loops.
- Because the measurement technique uses switched current sources, excessive cable or filter capacitance can affect the measurement. When using long cables, the filter capacitance can be reduced or removed.

Noise Filtering

For temperature sensors operating in noisy environments, the industry-standard practice is to place a capacitor across the D+ and D− pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. While this capacitor does reduce noise, it does not eliminate it, making it difficult to use the sensor in a very noisy environment.

The ADT7462 has a major advantage over other devices in eliminating the effects of noise on the external sensor. The series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the device. The effect of any filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7462 and the remote temperature sensor to operate in noisy environments. Figure 35 shows a low-pass RCR filter, with the following values:

R = 100 Ω

C = 1 nF

This filtering reduces both common-mode noise and differential noise.

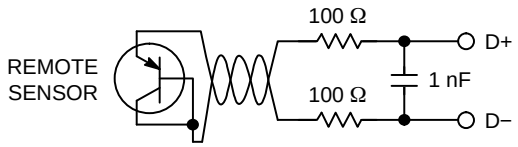


Figure 35. Filter Between Remote Sensor and ADT7462

Voltage Measurement

The ADT7462 is capable of measuring up to 13 different voltage inputs at one time. Table 15 is a list of the voltage measurement inputs and the corresponding input pins. Each pin can be configured to measure the desired voltage option using the Pin Configuration 1 (0x10) to Pin Configuration 4 (0x13) registers or the easy configuration options.

Input Circuit

The internal structure for the voltage inputs is shown in Figure 36. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order, low-pass filter that gives the input immunity to high frequency noise.

Voltages with full-scale values greater than the reference are divided so that the full-scale value equals the reference (2.25 V). All analog inputs are multiplexed into the on-chip, successive approximation ADC. This ADC has a resolution of ten bits. The basic input range is from 0 V to 2.25 V, but the inputs have built-in attenuators to allow measurement of larger and smaller voltages. To allow a tolerance for these voltages, the ADC produces an output of 3/4 full scale (decimal 768 or 0x300) for the nominal input voltage and so has enough headroom to cope with overvoltages.

A list of corresponding LSB and full-scale values for each input voltage is shown in Table 16.

Table 15. VOLTAGE INPUTS

Pin	Voltage Measured
7	+12V1
8	+12V2
13	+3.3V
15	+2.5V / +1.8V
19	+1.25V / +0.9V
21	+5V
22	+12V3
23	V_{CCP1} / +1.5V / +1.8V / +2.5V
24	V_{CCP2} / +1.5V / +1.8V / +2.5V
25	+1.2V1 (G_{BIT}) / +3.3V
26	+1.2V2 (FSB_V_{TT}) / V_{BATT}
28	+1.5V1 (ICH)
29	+1.5V2 (3GIO)

Table 16. INPUT RANGE CODE CONVERSION

Nominal Input Voltage (3/4 Scale)	Pin No.	1 LSB Value	Full Scale
+12V	7, 8, 22	0.0625	16 V
+5V	21	0.026	6.67 V
V_{CCP1}, V_{CCP2}	23, 24	0.00625	1.6 V
V_{CCP1}, when VIDs are Enabled	23	0.0125	3.2 V
+3.3V	13, 25	0.0172	4.4 V
V_{BATT}	26	0.0156	4.0 V
+2.5V	15, 23, 24	0.013	3.33 V
+1.8V	15, 23, 24	0.0094	2.4 V
+1.5V	23, 24, 28, 29	0.0078	2.0 V
+1.25V	19	0.0065	1.667 V
+1.2V	25, 26	0.00625	1.6 V
+0.9V	19	0.00469	1.2 V

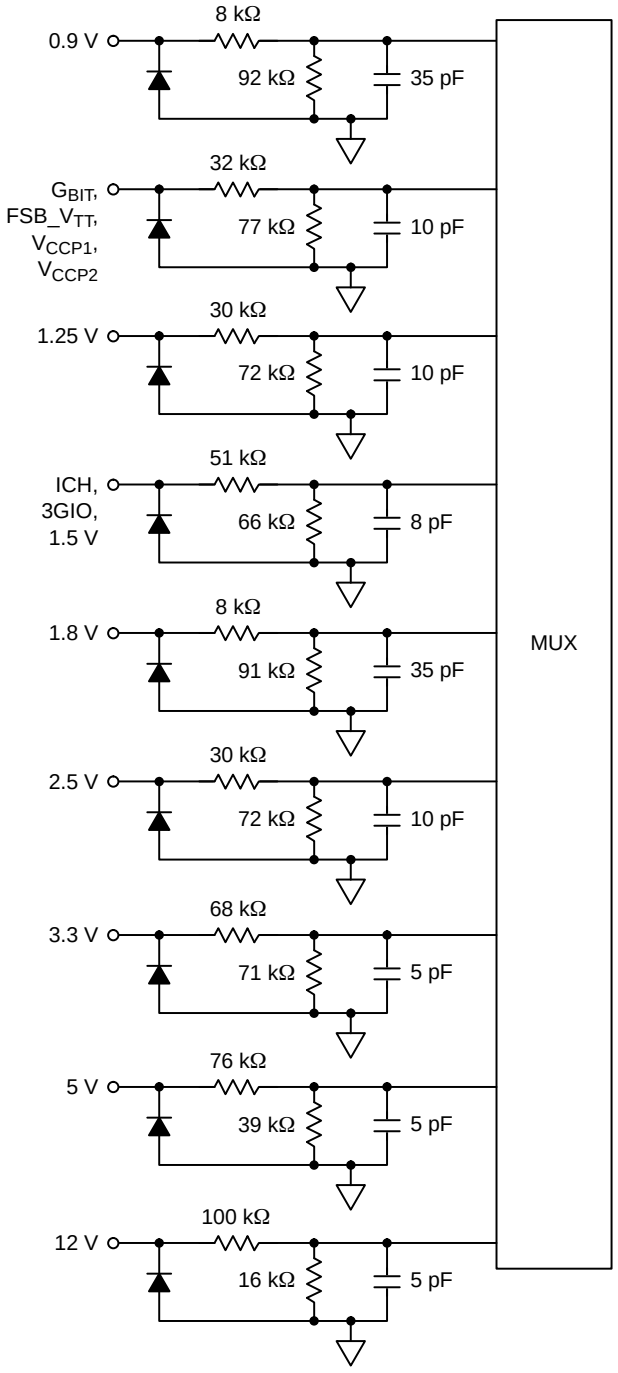


Figure 36. Voltage Input Structures

Example Calculations

Given the LSB value for each channel, the corresponding code for each voltage (or vice versa) can be calculated.

$$\text{Code} = \frac{\text{Voltage}}{1\ \text{LSB}}$$

Example:

The code for 1.8 V in a 1.8 V channel is:

$$\text{Code} = \frac{1.8}{0.0094} = 192\ (\text{that is, } 3/4\ \text{scale})$$

Similarly, the voltage, given the code in a particular channel, is calculated as follows:

$$\text{Voltage} = \text{Code} \times 1\ \text{LSB}$$

where:

10 V is connected to the 12 V channel.

1 LSB = 0.0625.

Code = 160 decimal.

Voltage Measurement and Limit Registers

The corresponding register locations for voltage measurements are listed in Table 17. Each voltage measurement channel has a high and low voltage limit associated with it. The voltage measurements are compared with these limits. The results of these comparisons are stored in status registers. A Logic 0 indicates an in-limit condition, and a Logic 1 indicates an out-of-limit condition. The ADT7462 can generate an $\overline{\text{ALERT}}$, if configured to do so, when a status bit is set. For more information on the status registers and $\overline{\text{ALERT}}$, see the Status and Mask Registers $\overline{\text{ALERT}}$ section. A complete list of all the high and low voltage limits in the ADT7462 and their default values is contained in Table 17.

Table 17. VOLTAGE VALUE AND LIMIT REGISTERS

Voltage Value	Pin No.	Value Register Address	Low Limit		High Limit	
			Register	Default	Register	Default
+12V1	7	0xA3	0x6D	0x00	0x7C	0xFF
+12V2	8	0xA5	0x6E	0x00	0x7D	0xFF
+3.3V	13	0x96	0x70	0x00	0x68	0xFF
+1.8V or +2.5V	15	0x8B	0x45	0x40	0x49	0x95
+1.25V or +0.9V	19	0x8F	0x47	0x40	0x4B	0x95
+5V	21	0xA7	0x71	0x00	0x7E	0xFF
+12V3	22	0xA9	0x6F	0x00	0x7F	0xFF
V_{CCP1}, +1.5V, +1.8V, +2.5V	23	0x90	0x72	0x20	0x69	0xFF
V_{CCP2}, +1.5V, +1.8V, +2.5V	24	0x91	0x73	0x00	0x6A	0xFF
+1.2V1 (G_{BIT}) or +3.3V	25	0x92	0x74	0x00	0x6B	0xFF
+1.2V2 (FSB_V_{TT}) or V_{BATT}	26	0x93	0x75	0x80	0x6C	0xFF
+1.5V1 (ICH)	28	0x94	0x77	0x00	0x50	0xA4
+1.5V2 (3GIO)	29	0x95	0x76	0x00	0x4C	0xA4

Battery Measurement Input (V_{BATT})

The V_{BATT} input allows the condition of a CMOS backup battery to be monitored. This is typically a lithium coin cell, such as a CR2032. The V_{BATT} input is accurate only for voltages greater than 1.2 V. Note that when Pin 26 is configured as a +1.2V input, voltages lower than 1.2 V are not accurately measured. Input voltage and corresponding voltage measured are shown in Figure 16.

Typically, the battery in a system is required to keep some devices powered on when the system is in a powered-off state. The V_{BATT} measurement input is designed to minimize battery drain. To reduce current drain from the battery, the lower resistor of the V_{BATT} attenuator is not connected, except when a V_{BATT} measurement is being made. The total current drain on the V_{BATT} pin is 80 nA typical (for a maximum V_{BATT} voltage = 4.0 V), so a CR2032 CMOS battery functions in a system in excess of the expected 10 years. Note that when a V_{BATT} measurement is not being made, the current drain is reduced to 16 nA typical. Under normal voltage measurement operating conditions, all measurements are made in a round-robin format, and each reading is actually the result of 16 digitally averaged measurements. However, averaging is not carried out on the V_{BATT} measurement to reduce measurement time and, therefore, reduce the current drain from the battery.

The V_{BATT} current drain when a measurement is being made is calculated by:

$$I = \frac{V_{BATT}}{100\ k\Omega} \times \frac{t_{pulse}}{t_{period}}$$

where:

t_{PULSE} is the V_{BATT} measurement time (~711 μs typical).
t_{PERIOD} is the time required to measure all analog inputs.

Monitoring cycle time depends on the ADT7462 configuration. Calculating the monitoring cycle time is described in more detail in the ADC Information section.

V_{BATT} Input Battery Protection

In addition to minimizing battery current drain, the V_{BATT} measurement circuitry is specifically designed with battery protection in mind. Internal circuitry prevents the battery from being back-biased by the ADT7462 supply or through any other path under normal operating conditions. In the unlikely event of a catastrophic ADT7462 failure, the ADT7462 includes a second level of battery protection, including a series 3 kΩ resistor to limit current to the battery, as recommended by UL (see Figure 37). Thus, it is not necessary to add a series resistor between the battery and the V_{BATT} input; the battery can be connected directly to the V_{BATT} input to improve voltage measurement accuracy.

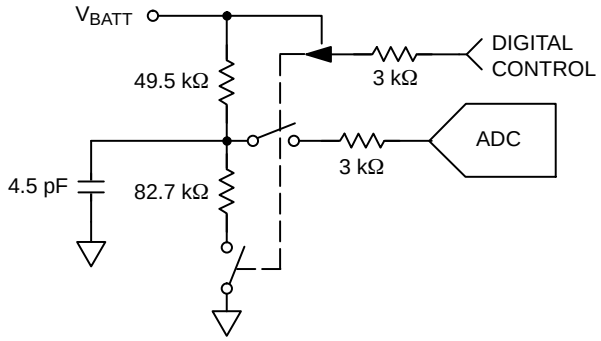


Figure 37. Equivalent V_{BATT} Input Protection Circuit

ADC Information

Round Robin

Both temperature and voltage measurements are analog inputs that are digitized using the on-board ADC. An internal multiplexer switches between the different analog inputs and digitizes them, in turn, in a round-robin manner. The total conversion time depends upon how the ADT7462 is configured. The conversion times for each measurement channel are shown in Table 18. The complete conversion time is the sum of the time for the voltage and temperature measurements.

For example, if the ADT7462 is configured as Easy Configuration Option 1, the round-robin conversion time is calculated as follows:

Total Conversion Time =
1 × (Local Conversion Time) +
3 × (Remote Conversion Time) +
4 × (Voltage Measurement Time)

The TACH is not measured using the ADC and so is not part of the round-robin monitoring cycle.

Table 18. MEASUREMENT CHANNEL CONVERSION TIMES

Channel	Conversion Time (ms)
Local Temperature	9.01
Remote Temperature	38.36
Voltage	8.53

For each ADC temperature and voltage measurement read from their value registers, 16 readings have actually been made internally and the results averaged before being placed in the value register.

Bypass Voltage Attenuators

There are up to 13 voltage measurement channels on the ADT7462. Each of these voltage measurement channels has an input structure (see Figure 36 for input structures for each of the voltage channels). Because the ADC has a voltage input range from 0 V to 2.25 V, these input circuits attenuate the voltage input using a resistor divider network to match the input range of the ADC. However, the user may occasionally want to remove the attenuators and directly apply a voltage of between 0 V and 2.25 V to the ADC. These attenuators can be disabled by setting relevant bits in the voltage attenuator configuration registers (see Table 19). This feature also allows the user to rescale the voltage inputs using an external attenuator circuit. However, when the attenuators are disabled, the user should ensure that the voltage on the pin never exceeds 2.25 V.

Table 19. VOLTAGE ATTENUATOR CONFIGURATION REGISTERS

Register Name	Register Address
Voltage Attenuator Configuration Register 1	0x18
Voltage Attenuator Configuration Register 2	0x19

Single-channel ADC Conversions

Setting Bit 2 of the EDO Enable register (0x16) places the ADT7462 into single-channel mode. In this mode, the ADT7462 can be made to convert on a single voltage or temperature channel only. The channel to be converted on is selected by writing to Bits [7:3] of the EDO (single-channel) Enable register (0x16). When the device is in single-channel mode, the pin configuration option should not be changed.

Note that when the Pin 26 voltage, which includes the V_{BATT} option, is selected in single-channel mode, this means that voltage measurements are continuously made in this mode. If a battery is connected to this input, this results in an excessive current drain on the battery. The specification of >10 years of battery life is valid only when the battery voltage is measured as part of the round robin and not in single-channel mode.

Table 20. SINGLE-CHANNEL MODE OPTIONS

Bits [7:3]	ADC Channel Selected
0000 0	+1.2V2 Voltage, Pin 26
0000 1	Remote 1 Temperature
0001 0	Remote 2 Temperature
0001 1	Remote 3 Temperature
0010 0	Local Temperature
0010 1	+12V1 Voltage, Pin 7
0011 0	+12V2 Voltage, Pin 8
0011 1	+12V3 Voltage, Pin 22
0100 0	+3.3V Voltage, Pin 13
0100 1	+2.5V/+1.8V Voltage, Pin 15
0101 0	+1.25V/+0.9V Voltage, Pin 19
0101 1	+5V Voltage, Pin 21
0110 0	+1.5V/+1.8V/+2.5V Voltage, Pin 23
0110 1	+1.5V/+1.8V/+2.5V Voltage, Pin 24
0111 0	+1.2V1/+3.3V Voltage, Pin 25
1000 0	+1.5V1 Voltage, Pin 28
1000 1	+1.5V2 Voltage, Pin 29

Dynamic VID Functionality

VID Code

The ADT7462 can be configured to monitor up to seven VID inputs. The VID code is output on seven lines from the CPU to tell the power controller what input voltage it requires. The ADT7462 can monitor the VID code and the voltage applied to the CPU to ensure that they match within an acceptable range. This acceptable range is programmable in the ADT7462.

The VID lines are monitored by the ADT7462, and the VID code is stored in the VID Value register (0x97), which can be read back over the SMBus.

VID monitoring is enabled by setting Bit 7 (VIDs) of Pin Configuration Register 1 (0x10) to 1. See Table 21 and Table 22 for information on which pin should be connected to each VID line. When VID monitoring is enabled, all seven pins are automatically configured as VID inputs. It is not possible to select six pins as VID inputs and use the remaining pin as an alternate function.

VID Value Register (0x97)

Bit 0 = VID0 (reflects the logic state of Pin 1)

Bit 1 = VID1 (reflects the logic state of Pin 2)

Bit 2 = VID2 (reflects the logic state of Pin 3)

Bit 3 = VID3 (reflects the logic state of Pin 4)

Bit 4 = VID4 (reflects the logic state of Pin 31)

Bit 5 = VID5 (reflects the logic state of Pin 32)

Bit 6 = VID6 (reflects the logic state of Pin 28)

The ADT7462 supports both the VR10 and the VR11 specifications. The default option supports the VR10 specification. To switch to the VR11 specification, set Bit 6 of Configuration Register 0 (0x00) to 1. VR11 is defined as eight bits; the ADT7462 monitors only seven VID lines (see Table 21).

Table 21. VR11 VID CODES

VID Number	Pin No.	Voltage
VID6	28	400 mV
VID5	32	200 mV
VID4	31	100 mV
VID3	4	50 mV
VID2	3	25 mV
VID1	2	12.5 mV
VID0	1	6.25 mV

VR10 requires only six VID lines (see Table 22). Pin 28 should be connected to ground when monitoring VR10 VID codes. VID6 reports a 0.

Table 22. VR10 VID CODES

VID Number	Pin No.	Voltage
VID6	28	Unused, Connect to GND
VID5	32	12.5 mV
VID4	31	400 mV
VID3	4	200 mV
VID2	3	100 mV
VID1	2	60 mV
VID0	1	25 mV

Dynamic VID Monitoring

The ADT7462 supports dynamic VID monitoring. The purpose of the VID code is to tell the voltage controller what V_{CCP} voltage should be applied to the CPU. The V_{CCP} voltage applied to the processor changes as the power requirements of the processor change. The VID is compared with V_{CCP1} only. Note that when the VIDs are enabled, the LSB value for V_{CCP1} becomes 0.0125 V (see Table 16).

The VID values can represent voltages from 0.8375 V to 1.6 V. The VID code is sampled by the ADT7462 every 11 μs and is stored in Register 0x97. Once the VID code has been stable (that is, does not change) for 55 μs, the measured V_{CCP} is then compared with the VID code. The comparison table used is for either the VR10 or the VR11 specification (set by Bit 6 of Register 0x00). If the VID code and the measured V_{CCP} do not match within a certain limit, an $\overline{\text{ALERT}}$ is generated.

The VID value decoded and the V_{CCP} measurement must be within a window controlled by the VID high and low limits. The VID is compared with V_{CCP1} only. Register 0x78 holds the 4-bit VID high and low limits. The high limit has a range of 0 mV to 375 mV with a resolution of 25 mV (four bits). The low limit has a range of 0 mV to −187.5 mV with a resolution of 12.5 mV (four bits). The high limit is used in a greater-than comparison, and the low limit is used in a less-than-or-equal-to comparison. Note that if both limits are set to 0x00, because the low limit is less than or equal to the comparison, an $\overline{\text{ALERT}}$ always results. Therefore, the minimum value for low limit is 0x01.

If the V_{CCP} voltage measured and the VID code do not match to within the programmed limit, Status Bit 6 of the digital status register is set (Register 0xBE). This, in turn, can generate an $\overline{\text{ALERT}}$ if it is not masked.

Example

VID high limit: 100 mV (Register 0x78), four MSBs set to 0100.

VID low limit: 50 mV (Register 0x78), four LSBs set to 0100.

VID value equates to 1.1 V. This is the read VID decoded, using either VR10 or VR11 tables.

V_{CCP1} must be in the window of 1.05 V to 1.2 V. If the V_{CCP1} value is outside this window, the status bit is set and an $\overline{\text{ALERT}}$ is generated.

To clear an $\overline{\text{ALERT}}$ generated in this way, read the digital status register. If the VID code and V_{CCP} are now matching within the programmed window (that is, the error condition that caused the $\overline{\text{ALERT}}$ has gone away), then the status bit is reset and so is the $\overline{\text{ALERT}}$.

The VID to V_{CCP} voltage tables for both VR10 and VR11 can be found on the Intel website. See the Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.0 Design Guidelines, Page 18 and Page 19, for additional information.

Status and Mask Registers and $\overline{\text{ALERT}}$

Status Registers

Each measured temperature and voltage has an associated high and low limit. The measured values are compared with these programmable limits. The results of these comparisons are stored in the status registers. A Logic 0 in the status register represents an in-limit comparison, while a Logic 1 represents an out-of-limit comparison.

Once a status bit is set, it remains set until the status register is read by the SMBus master. Once read, the status bit is cleared if the error condition has gone away. The status registers are duplicated to accommodate situations where there are two SMBus masters. If one master reads the host status registers and consequently clears them, the second master has no way of knowing what bits were set and what bits were cleared. The second SMBus master can read from the duplicate BMC status registers to determine which status bits were set.

Table 23 is a list of the status registers and corresponding addresses.

Table 23. STATUS REGISTERS

Register Name	Host Address	BMC Address
Thermal Status Register 1	0xB8	0xC0
Thermal Status Register 2	0xB9	0xC1
Thermal Status Register 3	0xBA	–
Voltage Status Register 1	0xBB	0xC3
Voltage Status Register 2	0xBC	0xC4
Fan Status Register 1	0xBD	0xC5
Digital Status Register 1	0xBE	0xC6
GPIO Status Register	0xBF	–

$\overline{\text{ALERT}}$ Output

The ADT7462 has an SMBus $\overline{\text{ALERT}}$ output that is asserted when one of the status bits is set. This is to alert the master that an out-of-limit measurement has taken place or that there is a fault on one of the fan channels.

An $\overline{\text{ALERT}}$ is generated as a result of a status bit being set in any of the registers.

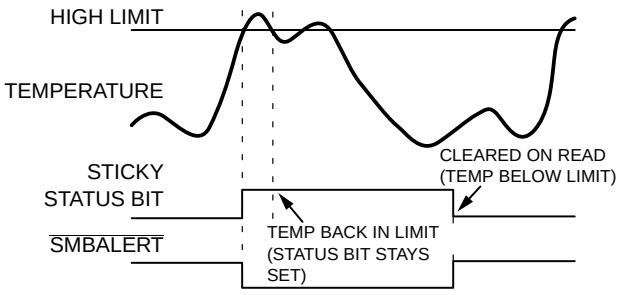


Figure 38. $\overline{\text{ALERT}}$ and Status Bit Behavior

Figure 38 shows how the $\overline{\text{ALERT}}$ output and “sticky” status bits behave. When a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition goes away and the status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out-of-limit event cannot be missed, if software is polling the device periodically. Note that the $\overline{\text{ALERT}}$ output remains low for the entire duration that a reading is out of limit and until the status register has been read.

Mask Registers

The user has the option of masking any of the individual status bits that generate an $\overline{\text{ALERT}}$. This is achieved by setting the appropriate bit in the mask registers. The $\overline{\text{ALERT}}$ output is not asserted on the setting of a status bit if it has been masked. The status bit itself is not affected and continues to be set when an out-of-limit condition exists.

Table 24 is a list of the mask registers and corresponding addresses.

Table 24. MASK REGISTERS

Register Name	Register Address
Thermal Mask Register 1	0x30
Thermal Mask Register 2	0x31
Voltage Mask Register 1	0x32
Voltage Mask Register 2	0x33
Fan Mask Register	0x34
Digital Mask Register	0x35
GPIO Mask Register	0x36

Fan Control

Fan Drive Using PWM Control

The ADT7462 uses pulse-width modulation (PWM) to control fan speed. Control relies on varying the duty cycle

(or on/off ratio) of a square wave applied to the fan to vary the fan speed. The advantage of using PWM control is that it uses a very simple external circuit. The specific circuit used depends upon the type of fan.

There are three main fan types in use: 2-wire fans, 3-wire fans, and 4-wire fans. The 2-wire fan has only power and ground connections. The 3-wire fan has power and ground connections and a TACH output to indicate the speed of the fan. The 4-wire fan has power and ground connections, a TACH output, and a PWM input. The PWM input is connected directly to the PWM drive of the ADT7462 and is used to control the speed of the fans.

For 2-wire and 3-wire fans, the low frequency PWM drive signal should be selected. For 4-wire fans, the high frequency PWM drive signal should be selected.

Using the ADT7462 with 2-wire Fans

Figure 39 shows the most typical circuit used with a 2-wire fan and illustrates how a 2-wire fan can be connected to the ADT7462. The low frequency PWM mode must be selected when using a 2-wire fan.

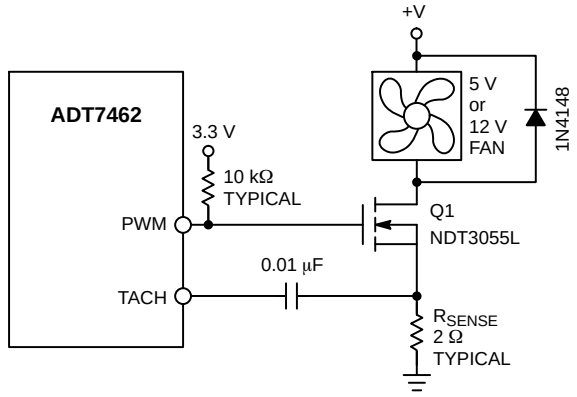


Figure 39. Driving a 2-wire Fan

Using the ADT7462 with 3-wire Fans

Figure 40 shows the most typical circuit used with a 3-wire fan.

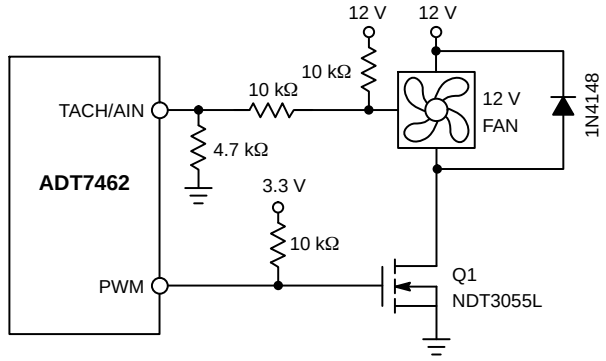


Figure 40. Driving a 3-wire Fan

The external circuitry required is very simple. A MOSFET, such as the NDT3055L, is used as the pass device. The specifications of the MOSFET depend on the maximum current required by the fan being driven. A typical PC fan can draw a nominal current ranging from a few hundred milliamps to over an amp of current. Depending on the current rating of the fan, a SOT device can be used where board space is a concern. If several fans in parallel are driven from a single PWM output or if larger server fans are driven, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3 V, for direct interfacing to the PWM pins. V_{GS} can be greater than 3.3 V as long as the pullup on the gate is tied to 5.0 V. The MOSFET should also have a low on resistance to ensure that there is not a significant voltage drop across the FET, which would reduce the voltage applied across the fan and reduce the full speed of the fan.

Figure 40 uses a 10 kΩ pullup resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 5.0 V maximum to prevent damaging the ADT7462. If in doubt as to whether the fan used has an open-collector or totem-pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section.

Driving a 3-wire fan with a PWM signal makes the fan speed measurement more difficult because the TACH signal is chopped by the PWM drive signal. Pulse stretching is required in this case to make accurate fan speed measurements. For more information, see the Fan Speed Measurement section.

Using the ADT7462 with 4-wire Fans

Figure 41 shows the most typical circuit used with 4-wire fans.

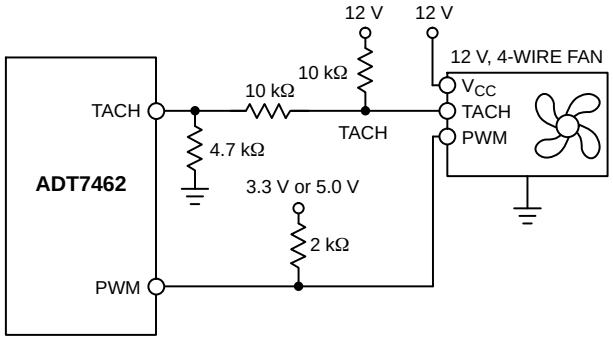


Figure 41. Driving a 4-wire Fan

Because the electronics in a 4-wire fan are powered continuously, unlike previous PWM driven/powered fans, 4-wire fans tend to perform better than 3-wire fans, especially for high frequency applications. 4-wire frames also eliminate the requirement for pulse stretching, because the TACH signal is always available.

Driving Two Fans from Each PWM

Note that the ADT7462 has up to eight TACH inputs available for fan speed measurement, but only four PWM

drive outputs. If all eight fans are being used in the system, two fans should be driven in parallel from each PWM output. Figure 42 shows how to drive two fans in parallel using the NDT3055L MOSFET. This information is relevant for low frequency mode only (2-wire and 3-wire fans), because the PWM and TACHs need to be synchronized to obtain accurate fan speed measurements using pulse stretching (see the Fan Speed Measurement with Pulse Stretching section). In high frequency mode and when using 4-wire fans, the TACH signal is always valid because the fan is always powered on.

Note that because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM pins are not required to source current and that they sink less than the 8 mA maximum current specified on the MOSFET data sheet.

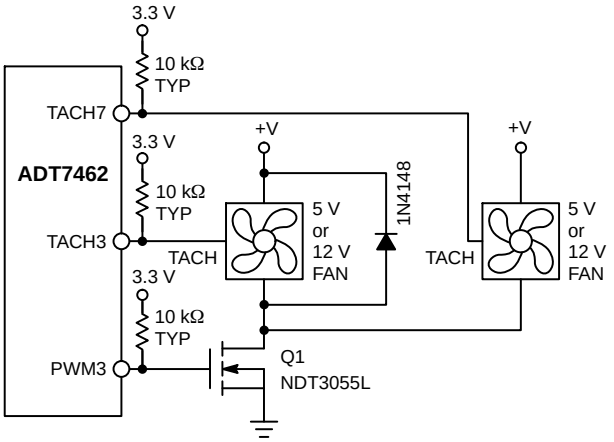


Figure 42. Interfacing Two Fans in Parallel to a PWM Output Using a Single N-channel MOSFET

Fan Speed Measurement and Control

TACH Inputs

Pin 1, Pin 2, Pin 3, Pin 4, Pin 7, Pin 8, Pin 21, and Pin 22 are TACH inputs intended for fan speed measurement.

Signal conditioning in the ADT7462 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5.0 V, even when V_{CC} is less than 5.0 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5.0 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 43 to Figure 46 show circuits for most common fan TACH circuits.

If the fan TACH output has a resistive pullup to V_{CC}, it can be connected directly to the fan input, as shown in Figure 43.

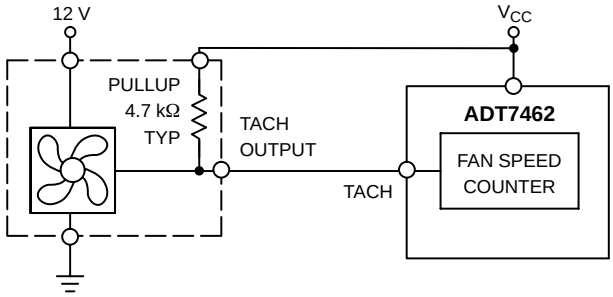


Figure 43. Fan with TACH Pullup to V_{CC}

If the fan output has a resistive pullup to 12 V (or other voltage greater than 5.0 V), the fan output can be clamped with a Zener diode, as shown in Figure 44. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 5.0 V, allowing for the voltage tolerance of the Zener diode. A value of between 3.0 V and 5.0 V is suitable.

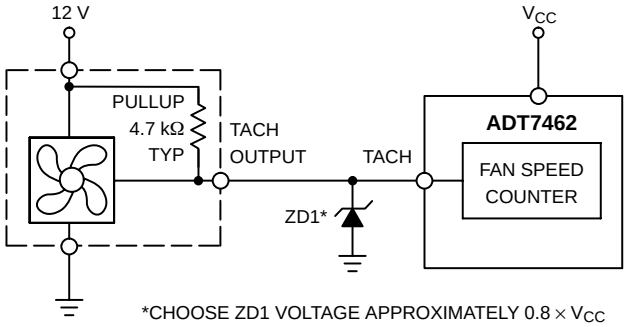


Figure 44. Fan with TACH Pullup to Voltage > 5.0 V, (Example 12 V) Clamped with Zener Diode

If the fan has a strong pullup (less than 1 kΩ) to 12 V or a totem-pole output, a series resistor can be added to limit the Zener current, as shown in Figure 45. Alternatively, a resistive attenuator can be used, as shown in Figure 46. R1 and R2 should be chosen such that:

$$2\ V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5\ V$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, so this should be taken into account when calculating resistor values.

With a pullup voltage of 12 V and a pullup resistor of less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ and 47 kΩ. This gives a high input voltage of 3.83 V.

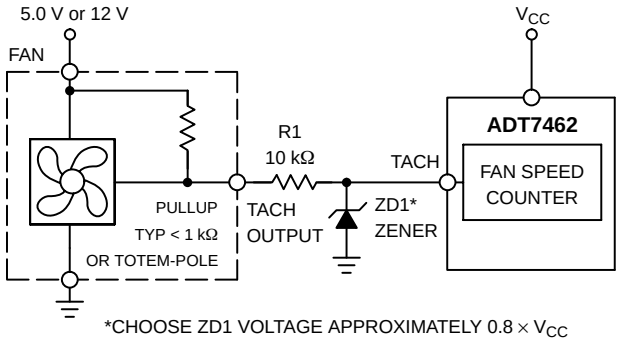


Figure 45. Fan with Strong TACH. Pullup to > V_{CC} or Totem-Pole Output, Clamped with Zener Diode and Resistor

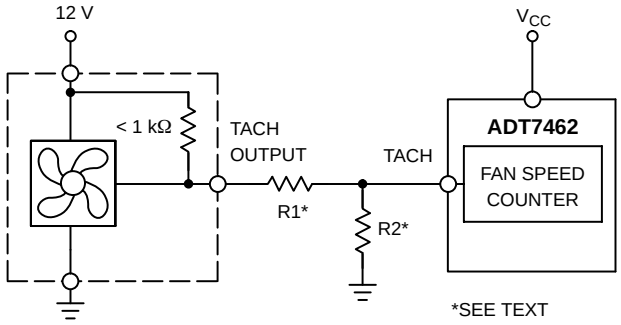


Figure 46. Fan with Strong TACH. Pullup to > V_{CC} or Totem-Pole Output, Attenuated with R1/R2

Fan Speed Measurement

The method of fan speed measurement when using 3-wire fans differs from that used with 4-wire fans. When 3-wire fans are in use, power is continuously applied and removed from the fan, thereby chopping the TACH information. As a result, every time a fan speed measurement is to be made, the fan must be switched on for a long enough period of time that a measurement can be made. This is called pulse stretching. With 4-wire fans, power is always applied to the fan, so fan speed measurements can be made continuously, and there is no need for pulse stretching. Pulse stretching is also not necessary when driving a 3-wire fan with a dc input. The Fan Speed Measurement with Pulse Stretching section, which describes how fan speed is measured both when pulse stretching is required and when it is not.

Fan Speed Measurement Without Pulse Stretching

Fan speed is measured by the ADT7462, and the result is stored in the fan TACH value registers. The fan counter does not count the fan TACH output pulses directly because the fan speed can be less than 1000 rpm, and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90 kHz oscillator into the input of a 16-bit counter for N periods of the fan TACH output (see Figure 47), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

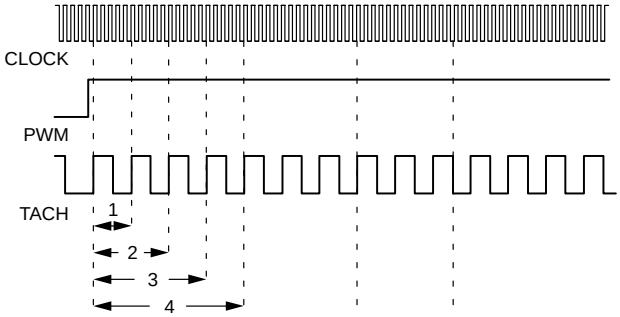


Figure 47. Fan Speed Measurement

To enable continuous measurement for 3-wire fans, set the corresponding dc bit for the TACH input in the TACH configuration register. This bit is set automatically when the HF PWM is in use with 4-wire fans.

Fan Speed Measurement with Pulse Stretching

The method for measuring fan speed for 3-wire fans requiring pulse stretching is similar to the method described in the Fan Speed Measurement without Pulse Stretching section for continuous measurements. The main difference is that the PWM drive must be synchronized to the TACH input so that the ADT7462 knows that pulse stretching is taking place while the TACH is being measured.

PWM1 is synchronized with TACH1 and TACH2.

PWM2 is synchronized with TACH3 and TACH4.

PWM3 is synchronized with TACH5 and TACH6.

PWM4 is synchronized with TACH7 and TACH8.

Driving and Measuring the Speed of Two Fans from One PWM Output

When pulse stretching is enabled, the ADT7462 measures fan speed once a second. The counter then counts up from the first to the third TACH pulse; this value is stored in the TACH value register. The PWM drive returns to its previous programmed value. Each TACH input is synchronized to a particular PWM output. The PWM and TACH pins must be connected as shown in Figure 48 to ensure that pulse stretching is synchronized between the PWM output and the TACH inputs, and an accurate fan speed measurement is made on each fan.

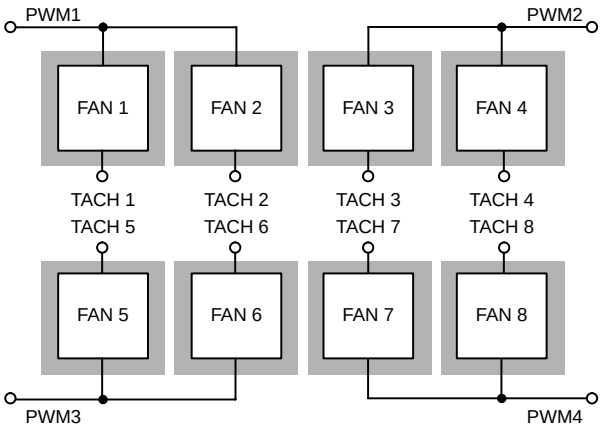


Figure 48. Synchronizing Fan PWM Output and TACH Inputs

Driving and Measuring the Speed of One Fan from One PWM Output

If four single fans are being controlled and measured by the ADT7462, the following configuration should be used. This applies only to 3-wire fans controlled using low frequency PWM with pulse stretching enabled.

Fan 1 is driven by PWM1 and measured using TACH1.

Fan 2 is driven by PWM2 and measured using TACH3.

Fan 3 is driven by PWM3 and measured using TACH5.

Fan 4 is driven by PWM4 and measured using TACH7.

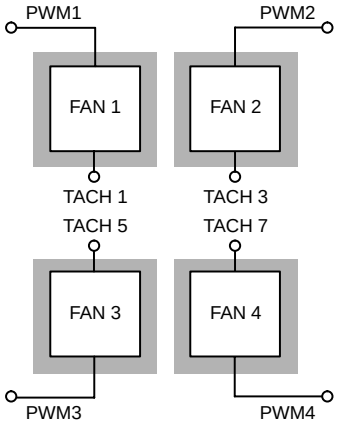


Figure 49. Driving and Measuring the Speed on a Single Fan

The PWM output is pulse stretched until a valid TACH is read on both TACH inputs synchronized to the particular PWM output. If one fan is connected to one PWM output, the PWM output is pulse stretched until the counter has timed out on the disconnected TACH input. In this case, the pulse is stretching longer than necessary in an effort to sense a disconnected fan. The speed of the connected fan may be increased and an audible change in fan speed may be observed. There are two options to prevent the PWM output from being stretched longer than necessary in this case.

- Connect the two synchronized TACH inputs together; for example, if PWM1 is driving a single fan being sensed on TACH1 only, connect TACH1 and TACH2 together.
- Turn off pulse stretching on the unused TACH input; that is, if PWM1 is driving a single fan being sensed on TACH1 only, turn off pulse stretching on TACH2 in Register 0x08. In this register:

  Bit 0 controls pulse stretching on TACH1 and TACH5.

  Bit 1 controls pulse stretching on TACH2 and TACH6.

  Bit 2 controls pulse stretching on TACH3 and TACH7.

  Bit 3 controls pulse stretching on TACH4 and TACH8.

Note that the TACH assignments in this register differ from the TACHs synchronized to each PWM output. Therefore, if the intention is to drive and sense four fans, connecting the TACHs together as described in Option 1 allows pulse stretching on all channels.

To enable fan speed measurements four times a second, set the FAST bit (Bit 0) of Configuration Register 2 (0x02). When the FAST bit is set, fan TACH readings are updated every 250 ms.

Fan Speed Measurement Registers

Fan speed measurement involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (because two pulses per revolution are being counted). Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates either that the fan has stalled or is running very slowly (< 100 rpm).

The actual fan TACH period is being measured; therefore, an $\overline{\text{ALERT}}$ is generated if the reading falls below a fan TACH limit. This $\overline{\text{ALERT}}$ sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$. The TACH limit is an 8-bit value that is compared with the TACH high byte of the TACH reading.

Table 25. TACHOMETER VALUE & LIMIT REGISTERS

TACH	Low Byte Value Register	High Byte Value Register	8-bit Limit Register
TACH1	0x98	0x99	0x78
TACH2	0x9A	0x9B	0x79
TACH3	0x9C	0x9D	0x7A
TACH4	0x9E	0x9F	0x7B
TACH5	0xA2	0xA3	0x7C
TACH6	0xA4	0xA5	0x7D
TACH7	0xA6	0xA7	0x7E
TACH8	0xA8	0xA9	0x7F

Calculating Fan Speed

Assuming a fan with two pulses per revolution (and two pulses per revolution being measured), fan speed is calculated by:

$$\text{Fan Speed(RPM)} = (\text{freq} \times 60)/\text{Fan Tachometer Reading} \quad \text{(eq. 1)}$$

where:

Fan Tachometer Reading is the 16-bit fan tachometer reading. freq is the oscillator frequency, 90 kHz.

Example:

TACH1 high byte (Register 0x99) = 0x17

TACH1 low byte (Register 0x98) = 0xFF

What is the speed of Fan 1 in rpm?

$$\text{Fan 1 Tachometer Reading} = 0 \times 17\text{FF} = 6143 \text{ Decimal} \quad \text{(eq. 2)}$$

$$\text{RPM} = (\text{freq} \times 60)/\text{Fan 1 Tachometer Reading} \quad \text{(eq. 3)}$$

$$\text{RPM} = (90000 \times 60)/6143 \quad \text{(eq. 4)}$$

$$\text{Fan Speed} = 879 \text{ RPM} \quad \text{(eq. 5)}$$

If the fan is a 6-pole fan, the count value is representative of 2/3 of a revolution. Therefore, the result of Equation 5 should be divided by 1.5. Similarly, if the fan used is an 8-pole fan, then the result should be divided by 2.

Fan Spin-Up

The ADT7462 has a unique fan spin-up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. The advantage of this process is that fans have different spin-up characteristics and require different times to overcome inertia. The ADT7462 runs the fans just fast enough to overcome inertia and the fans are quieter on spin-up than fans programmed to spin up for a given spin-up time.

Fan Startup Timeout

To prevent false interrupts being generated as a fan spins up (because it is below running speed), the ADT7462 includes a fan startup timeout function. During this time, the ADT7462 looks for two TACH pulses. If two TACH pulses are not detected, an interrupt is generated. Using Configuration Register 1 (0x01), Bit 4, this functionality can be changed to spinning the fans for a programmable time instead of two TACH pulses.

The startup timeout for each PWM drive is programmed by Bits [2:0] in the PWMx configuration registers.

PWM1 Configuration Register = Register 0x21

PWM2 Configuration Register = Register 0x22

PWM3 Configuration Register = Register 0x23

PWM4 Configuration Register = Register 0x24

Table 26. FAN STARTUP TIMEOUT

Bit Code	Startup Timeout
000	No Startup Timeout
001	100 ms
010	250 ms
011	400 ms
100	667 ms
101	1 sec
110	2 sec
111	32 sec

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non-inverted) or low for 100% duty cycle (inverted). This is programmed for each PWM drive in the PWMx Configuration Registers using the INV bit (Bit 4).

0 = Active high PWM outputs.

1 = Active low PWM outputs.

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. The ADT7462 supports both high frequency and low frequency PWM. High or low frequency PWM mode is selected in Register 0x02, Bit 2. In high frequency mode, the PWM drive frequency is always 22.5 kHz and cannot be changed. Register 0x25 and Register 0x26 configure the PWM frequency in low frequency mode for PWM1 to PWM4.

PWM Drive Frequency 1 is set using Bits [4:2] of the PWM1 and PWM2 frequency register (0x25).

PWM Drive Frequency 2 is set using Bits [7:5] of the PWM1 and PWM2 frequency register (0x25).

PWM Drive Frequency 3 is set using Bits [4:2] of the PWM3 and PWM4 frequency register (0x26).

PWM Drive Frequency 4 is set using Bits [7:5] of the PWM3 and PWM4 frequency register (0x26).

Table 27. LOW FREQUENCY PWM OPTIONS

Bit Code	Frequency
000	11 Hz
001	14.7 Hz
010	22.1 Hz
011	29.4 Hz
100	35.3 Hz
101	44.1 Hz
110	58.8 Hz
111	88.2 Hz

Fan Speed Control

The ADT7462 controls fan speed using two different modes: automatic and manual.

In automatic fan speed control mode, fan speed is automatically varied with temperature and without CPU intervention, after initial parameters are set up. The advantage of this mode is that if the system hangs, the system is protected from overheating. The automatic fan speed control incorporates a feature called dynamic T_{MIN} calibration. This feature reduces the design effort required to program the automatic fan speed control loop. For more information on how to program the automatic fan speed control loop and dynamic T_{MIN} operation, see the Programming the Automatic Fan Speed Control Loop section.

In manual fan speed control mode, the ADT7462 allows the duty cycle of any PWM output to be manually adjusted. This is useful if the user wants to change fan speed in the software or adjust PWM duty cycle output for test purposes. Bits [7:5] of Register 0x21 to Register 0x24 (PWM configuration registers) control the behavior of each PWM output. Under manual control, each PWM output can be manually updated by writing to Register 0xAA to Register 0xAD (PWM duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = $PWM_{MIN}/0.39$

Example 1: For a PWM duty cycle of 50%,

Value (decimal) = 50/0.39 = 128 decimal

Value = 128 decimal or 0x80

Example 2: For a PWM duty cycle of 33%,

Value (decimal) = 33/0.39 = 85 decimal

Value = 84 decimal or 0x54

PWM Duty Cycle Registers

Register 0xAA PWM1 Duty Cycle = 0x00 (0% default)

Register 0xAB PWM2 Duty Cycle = 0x00 (0% default)

Register 0xAC PWM3 Duty Cycle = 0x00 (0% default)

Register 0xAD PWM4 Duty Cycle = 0x00 (0% default)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode.

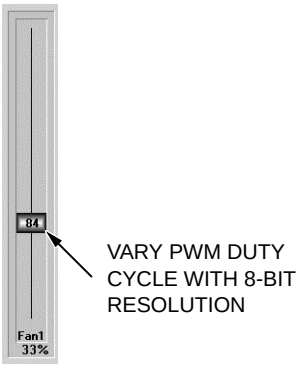


Figure 50. Control PWM Duty Cycle Manually with a Resolution of 0.39%

Programming the Automatic Fan Speed Control Loop

Note that to better understand the automatic fan speed control loop, use of the ADT7462 evaluation board and software is strongly recommended while reading this section.

This section provides the system designer with an understanding of the automatic fan control loop and provides step-by-step guidance on effectively evaluating and selecting critical system parameters. To optimize system characteristics, the designer needs to carefully plan system configuration, including the number of fans, where they are located, and what temperatures are being measured in the particular system.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of the process.

Automatic Fan Control Overview

The ADT7462 can automatically control the speed of fans based upon the measured temperature. This is done independently from CPU intervention once initial parameters are set up.

The ADT7462 has a local temperature sensor and up to three remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel Pentium class and other CPUs/GPUs). These four temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible, owing to the number of programmable parameters, including T_{MIN} and T_{RANGE}. The T_{MIN} and

T_{RANGE} values for a temperature channel and, therefore, for a given fan, are critical because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so these values should be selected carefully.

Figure 51 gives a top-level overview of the automatic fan control circuitry on the ADT7462. From a systems-level perspective, up to four system temperatures can be monitored and used to control four PWM outputs. The four PWM outputs can be used to control up to eight fans. The ADT7462 allows the speed of eight fans to be monitored. The Remote 1 and Remote 2 temperature channels have a thermal calibration block, allowing the designer to individually configure the thermal characteristics of those temperature channels. For example, the CPU fan can be run when CPU temperature increases above 60°C and a chassis fan can be run when the local temperature increases above 45°C. At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 51 shows controls that are fan-specific. The designer has control over individual parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control, then, ultimately allows graceful fan speed changes that are less perceptible to the system user.

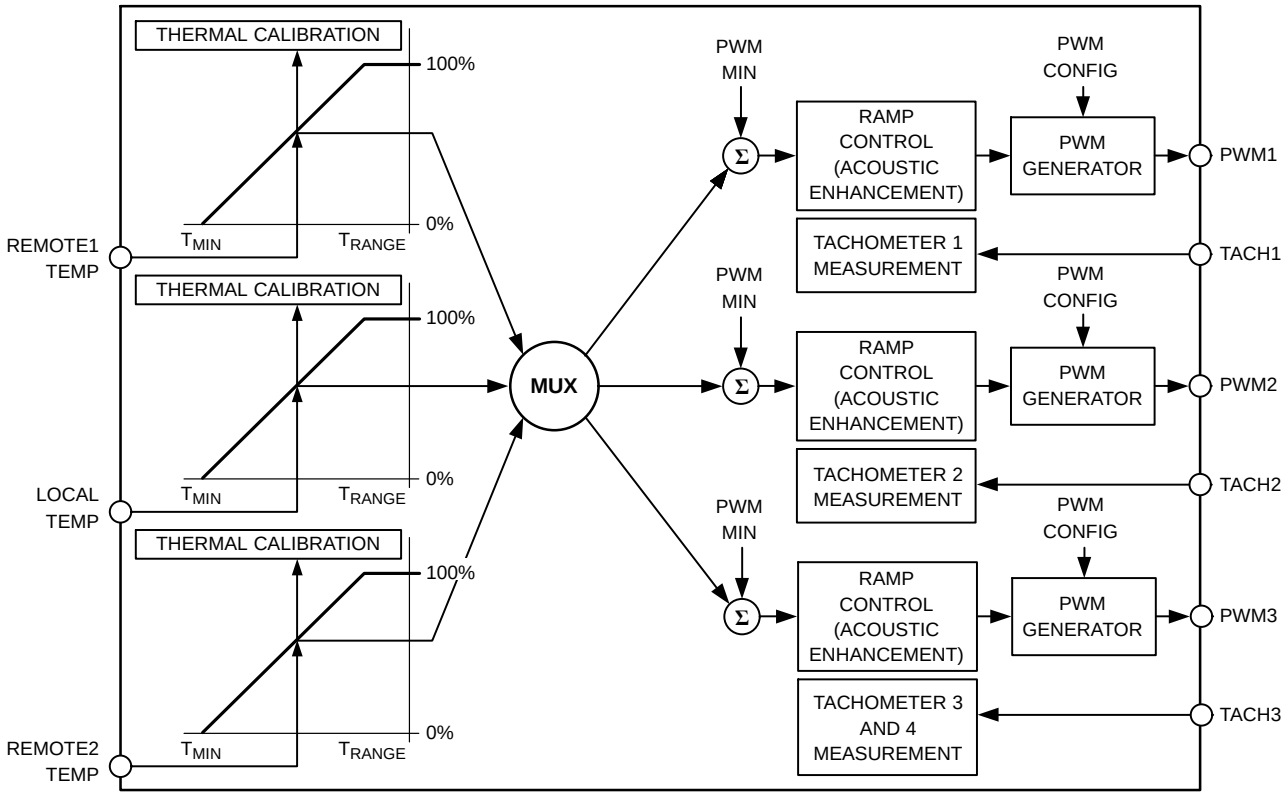


Figure 51. Automatic Fan Control Block Diagram

Step 1 − Configuring the MUX

First, the user needs to decide how many temperature channels are being measured and how many fans need to be controlled and monitored. When these decisions have been made, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control; they can be run manually (under software control) or they can be run at the fastest speed calculated by multiple temperature channels. The MUX is the bridge between temperature measurement channels and the three PWM outputs.

Bits [7:5] (BHVR) of Register 0x21, Register 0x22, Register 0x23, and Register 0x24 (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, PWM3, and PWM4 outputs. The values selected for these bits determine how the MUX connects a temperature measurement channel to a PWM output (see Figure 52).

Automatic Fan Control MUX Options

Bits [7:5] (BHVR), of Register 0x21, Register 0x22, Register 0x23, and Register 0x24, control the behavior of the corresponding PWM outputs (see Table 61 and Table 62).

The fastest speed calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example is the fan turning on when the Remote 1 temperature exceeds 60°C or when the local temperature exceeds 45°C.

Step 2 − T_{MIN} Settings for Thermal Calibration Channels

T_{MIN} is the temperature at which the fans start to turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen are temperature channel-specific; for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8-bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel: local, Remote 1, Remote 2, and Remote 3. When the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off after the temperature has dropped below $T_{MIN} - T_{HYST}$.

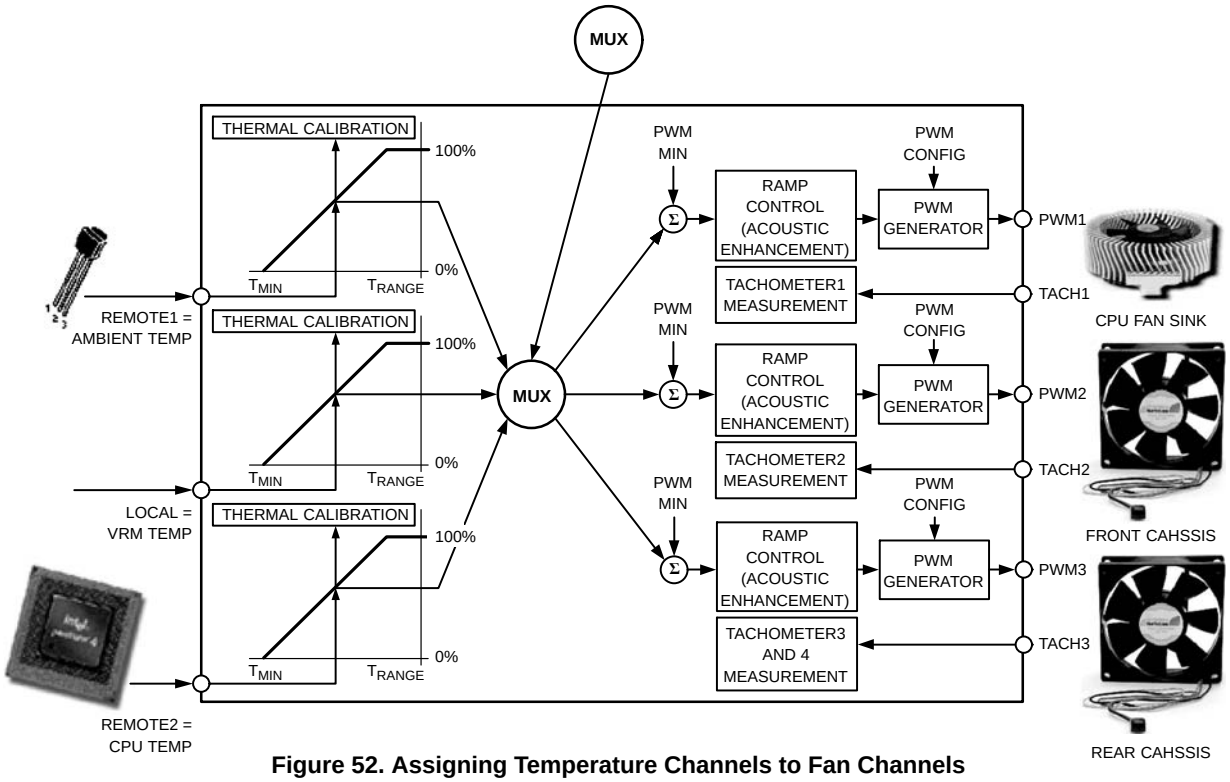


Figure 52. Assigning Temperature Channels to Fan Channels

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Spin-Up section for more details. In some cases, primarily for psycho-acoustic reasons, the fan should never switch off below T_{MIN}. The corresponding bits in Register 0x25 and Register 0x26 should be set to keep the fans running at the PWM minimum duty cycle, if the temperature falls below T_{MIN}.

T_{MIN} Registers

Register 0x5C, Local Temperature T_{MIN} = 0x9A (90°C)

Register 0x5D, Remote 1 Temperature T_{MIN} = 0x9A (90°C)

Register 0x5E, Remote 2 Temperature T_{MIN} = 0x9A (90°C)

Register 0x5F, Remote 3 Temperature T_{MIN} = 0x9A (90°C)

PWM1 and PWM2 Frequency Register (0x25)

Bit 0 (MIN 1) = 0. PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 0 (MIN 1) = 1. PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 1 (MIN 2) = 0. PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 1 (MIN 2) = 1. PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

PWM3 and PWM4 Frequency Register (0x26)

Bit 0 (MIN 3) = 0. PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 0 (MIN 3) = 1. PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 1 (MIN 4) = 0. PWM4 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 1 (MIN 4) = 1. PWM4 runs at PWM4 minimum duty cycle below $T_{MIN} - T_{HYST}$.

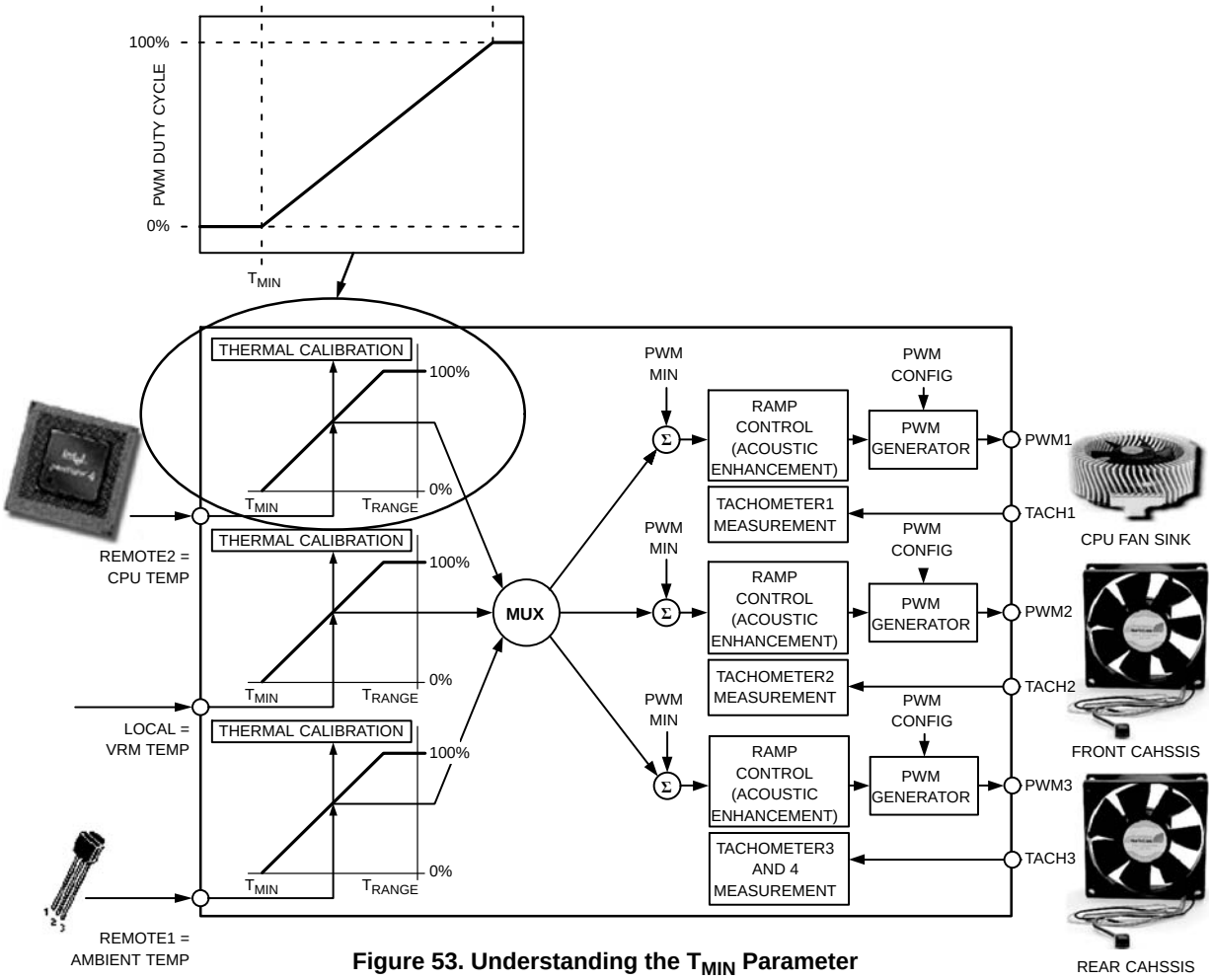


Figure 53. Understanding the T_{MIN} Parameter

Step 3 − PWM_{MIN} for Each PWM (Fan) Output

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan under automatic fan control when the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33% duty cycle range. This value can be found through fan validation.

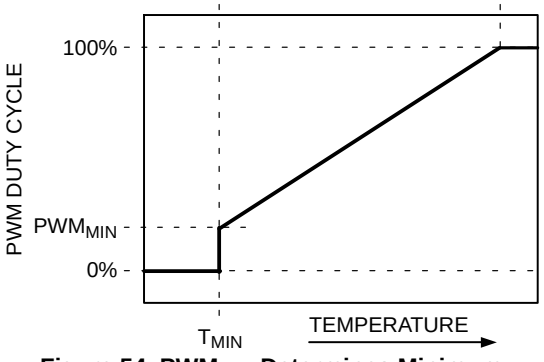


Figure 54. PWM_{MIN} Determines Minimum PWM Duty Cycle

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two different fans are used on PWM1 and PWM2, the fan characteristics can be set up differently. As a result, Fan 1, driven by PWM1, can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. Figure 55 illustrates this as $PWM1_{MIN}$ (the front fan) turns on at a minimum duty cycle of 20%, while $PWM2_{MIN}$ (the rear fan) turns on at a minimum duty cycle of 40%. Note, however, that both fans turn on at exactly the same temperature, defined by T_{MIN}.

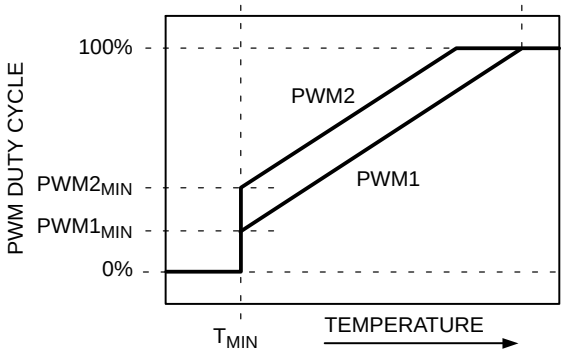


Figure 55. Operating Two Different Fans from a Single Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = PWM_{MIN} /0.39

Example 1: For a minimum PWM duty cycle of 50%,
Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a minimum PWM duty cycle of 33%,
Value (decimal) = 33/0.39 = 85 (decimal)
Value = 85 (decimal) or 0x54 (hexadecimal)

PWM_{MIN} Registers

Register 0x28, Minimum PWM1 Duty Cycle = 0x80 (50% Default)

Register 0x29, Minimum PWM2 Duty Cycle = 0x80 (50% Default)

Register 0x2A, Minimum PWM3 Duty Cycle = 0x80 (50% Default)

Register 0x2B, Minimum PWM4 Duty Cycle = 0x80 (50% Default)

Note on Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in rpm. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle actually runs the fan at closer to 50% of its full speed. This is because fan speed in % rpm generally relates to the square root of PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in rpm approximates to:

$$\%\ \text{fanspeed} = \sqrt{\text{PWM duty cycle} \times 10}$$

Step 4 − PWM_{MAX} for PWM (Fan) Outputs

PWM_{MAX} is the maximum duty cycle that each fan in the system runs at under the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible but should be capable of maintaining the processor temperature limit at an acceptable level. If the $\overline{\text{THERM}}$ temperature limit is exceeded, the fans are still boosted to 100% for fail-safe cooling.

There is one PWM_{MAX} limit (Register 0x2C) for all fan channels.

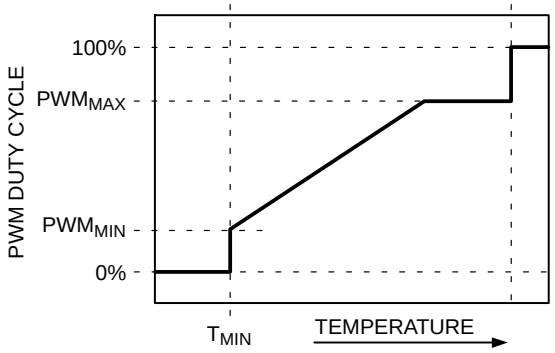


Figure 56. PWM_{MAX} Determines Maximum PWM Duty Cycle Below the $\overline{\text{THERM}}$ Temperature Limit

Programming the PWM_{MAX} Register

The PWM_{MAX} register (0x2C) is an 8-bit register that allows the maximum PWM duty cycle for the outputs to be configured anywhere from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MAX} register is given by:

Value (decimal) = PWM_{MAX}/0.39

Example 1: For a maximum PWM duty cycle of 50%,
Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a maximum PWM duty cycle of 75%,
Value (decimal) = 75/0.39 = 192 (decimal)
Value = 192 (decimal) or 0xC0 (hexadecimal)

PWM_{MAX} Register

Register 0x2C, Maximum PWM1 to PWM4 Duty Cycle = 0xC0 (75% default)

See the Note on Fan Speed and PWM Duty Cycle section for more information.

Step 5 − T_{RANGE} for Temperature Channels

T_{RANGE} is the range of temperatures over which automatic fan control occurs when the programmed T_{MIN} temperature is exceeded. T_{RANGE} is a temperature slope, not an arbitrary value; that is, a T_{RANGE} of 40°C holds true only for PWM_{MIN} = 33%. If PWM_{MIN} is increased or decreased, the effective T_{RANGE} changes.

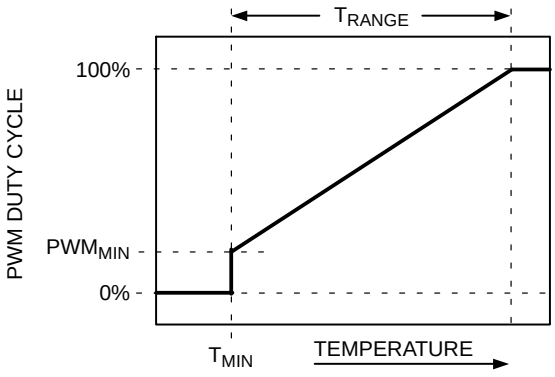


Figure 57. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} or fan control slope is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Determine experimentally the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. (For example, 70°C is reached when the fans are running at 50% PWM duty cycle.)
3. Determine the slope of the required control loop to meet these requirements.
4. Using the ADT7462 evaluation software, this functionality can be graphically programmed and visualized.

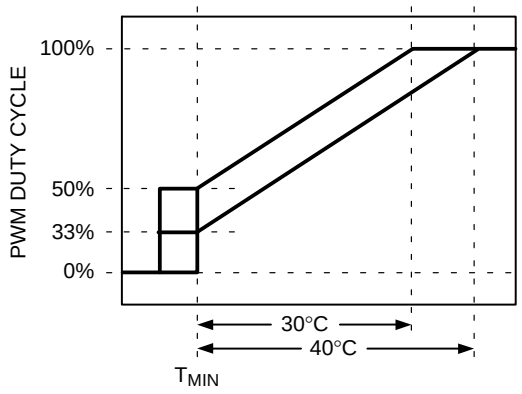


Figure 58. Adjusting PWM_{MIN} Affects T_{RANGE}

T_{RANGE} is implemented as a slope, which means that as PWM_{MIN} is changed, T_{RANGE} changes, but the actual slope remains the same. The higher the PWM_{MIN} value, the smaller the effective T_{RANGE}; that is, the fan reaches full speed (100%) at a lower temperature.

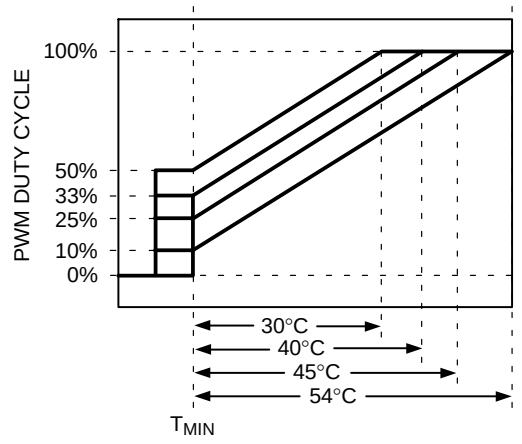


Figure 59. Increasing PWM_{MIN} Changes Effective T_{RANGE}

For a given T_{RANGE} value, the temperature at which the fan runs at full speed for different PWM_{MIN} values can be easily calculated by:

$$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170$$

where:

T_{MAX} is the temperature at which the fan runs full speed.
T_{MIN} is the temperature at which the fan turns on.
Max DC is the maximum duty cycle (100%) = 255 decimal.
Min DC is equal to PWM_{MIN}.
T_{RANGE} is the PWM duty cycle vs. temperature slope.

Example 1

Calculate T_{MAX}, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 10% duty cycle = 26 (decimal).

$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170$
$T_{MAX} = 30°C + (100\% - 10\%) \times 40°C/170$
$T_{MAX} = 30°C + (255 - 26) \times 40°C/170$
$T_{MAX} = 84°C$ (effective T_{RANGE} = 54°C)

Example 2

Calculate T_{MAX}, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 25% duty cycle = 64 (decimal).

$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170$
$T_{MAX} = 30°C + (100\% - 25\%) \times 40°C/170$
$T_{MAX} = 30°C + (255 - 64) \times 40°C/170$
$T_{MAX} = 75°C$ (effective T_{RANGE} = 45°C)

Example 3

Calculate T_{MAX}, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 33% duty cycle = 85 (decimal).

$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170$
$T_{MAX} = 30°C + (100\% - 33\%) \times 40°C/170$
$T_{MAX} = 30°C + (255 - 85) \times 40°C/170$
$T_{MAX} = 70°C$ (effective T_{RANGE} = 40°C)

Example 4

Calculate T_{MAX}, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 50% duty cycle = 128 (decimal).

$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170$
$T_{MAX} = 30°C + (100\% - 50\%) \times 40°C/170$
$T_{MAX} = 30°C + (255 - 128) \times 40°C/170$
$T_{MAX} = 60°C$ (effective T_{RANGE} = 30°C)

Selecting a T_{RANGE} Slope

The T_{RANGE} value can be selected for each temperature channel: local, Remote 1, Remote 2, and Remote 3. Bits [7:4] (RANGE) of Register 0x60 to Register 0x63 define the T_{RANGE} value for each temperature channel (see Table 85 and Table 86).

Summary of T_{RANGE} Function

When using the automatic fan control function, the temperature at which the fan reaches full speed can be calculated by:

$$T_{MAX} = T_{MIN} + T_{RANGE} \quad \text{(eq. 6)}$$

Equation 6 holds true only when PWM_{MIN} is equal to 33% PWM duty cycle.

Increasing or decreasing PWM_{MIN} changes the effective T_{RANGE}, although the fan control still follows the same PWM duty cycle to temperature slope. The effective

T_{RANGE} for different PWM_{MIN} values can be calculated using Equation 7.

$$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170 \quad \text{(eq. 7)}$$

where (Max DC − Min DC) × T_{RANGE}/170 is the effective T_{RANGE} value.

Figure 60 shows PWM duty cycle vs. temperature for each T_{RANGE} setting. The lower graph shows how each T_{RANGE} setting affects fan speed vs. temperature. As shown in the graph, the effect on fan speed is nonlinear.

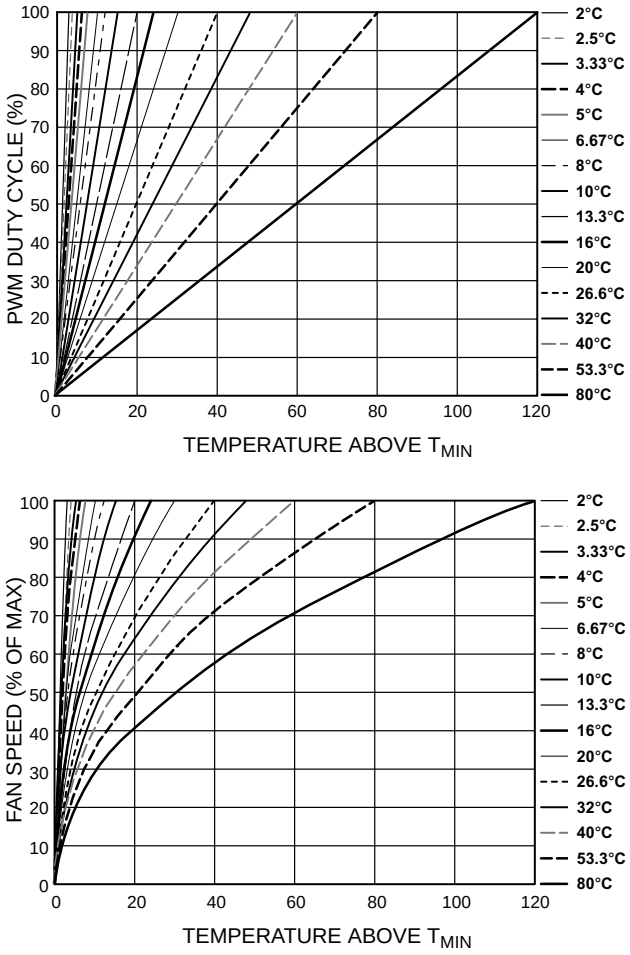


Figure 60. T_{RANGE} vs. Actual Fan Speed Profile

The graphs in Figure 60 assume that the fan starts from 0% PWM duty cycle. Clearly, the minimum PWM duty cycle, PWM_{MIN}, needs to be factored in to see how the loop actually performs in the system. Figure 61 shows how T_{RANGE} is affected when the PWM_{MIN} value is set to 20%. It can be seen that the fan runs about 45% fan speed when the temperature exceeds T_{MIN}.

Example: Determining T_{RANGE} for Each Temperature Channel

The following example shows how the different T_{MIN} and T_{RANGE} settings can be applied to three different thermal zones. In this example, the following T_{RANGE} values apply:

T_{RANGE} = 80°C for Ambient Temperature
T_{RANGE} = 53.3°C for CPU Temperature
T_{RANGE} = 40°C for VRM Temperature

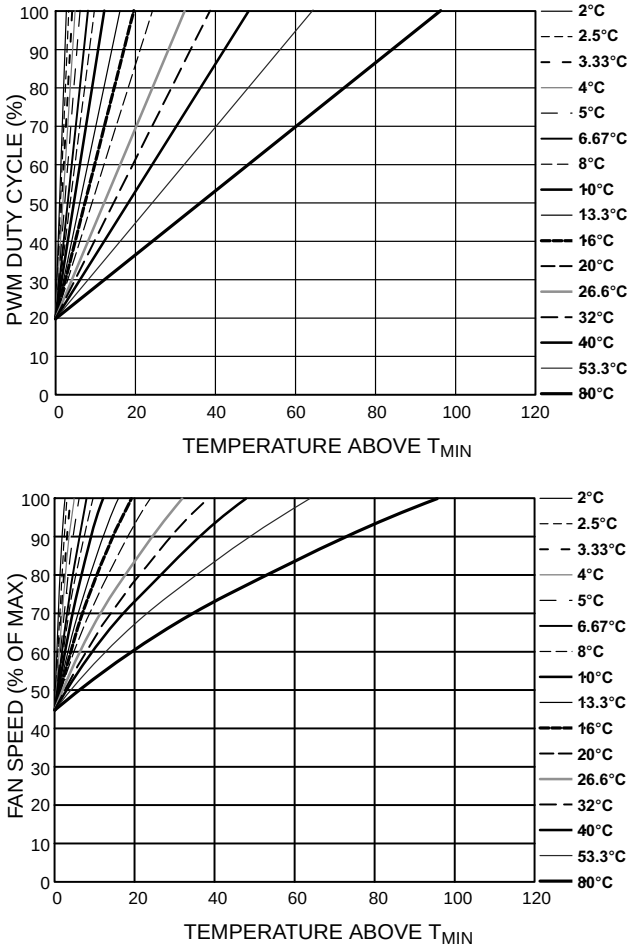


Figure 61. T_{RANGE} vs. % Fan Speed Slopes with PWM_{MIN} = 20%

This example uses the MUX configuration described in the Step 1 − Configuring the MUX section. Both CPU temperature and VRM temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3.

The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note on 4-wire Fans

The control range for 4-wire fans is much wider than that of 2-wire or 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20%.

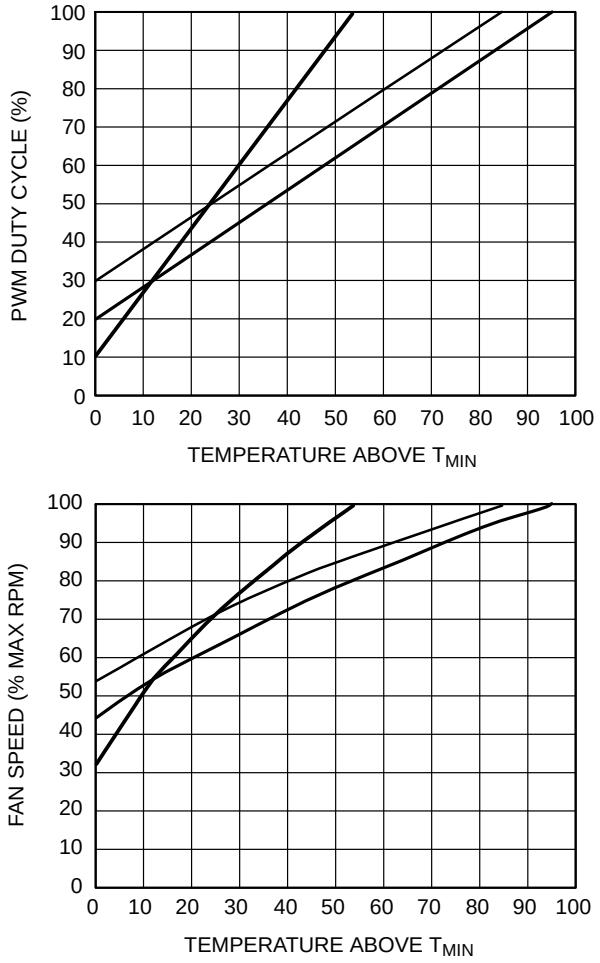


Figure 62. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

Step 6 − $T_{\overline{THERM}}$ for Temperature Channels

$T_{\overline{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM might be operating beyond its safe operating limit. When the measured temperature exceeds $T_{\overline{THERM}}$, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling. The fans remain running at 100% until the temperature drops below $T_{\overline{THERM}}$ minus hysteresis, where hysteresis is the number programmed into Local/Remote 1 Hysteresis Register 0x54 and Remote 2/Remote 3 Hysteresis Register 0x55. The default hysteresis value is 4°C.

The $T_{\overline{THERM}}$ limit should be considered as the maximum worst-case operating temperature of the system. Because exceeding any $T_{\overline{THERM}}$ limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and it must not be exceeded under normal system operating conditions.

Note that the $T_{\overline{THERM}}$ limits cannot be masked, and they affect the fan speed no matter how the automatic fan control settings are configured. This allows some flexibility because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C), can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

$\overline{THERM}$ Registers

Register 0x4C, Local $\overline{THERM1}$ temperature limit = 0xA4 (100°C Default)

Register 0x4D, Remote 1 $\overline{THERM1}$ temperature limit = 0xA4 (100°C Default)

Register 0x4E, Remote 2 $\overline{THERM1}$ temperature limit = 0xA4 (100°C Default)

Register 0x4F Remote 3 $\overline{THERM1}$ temperature limit = 0xA4 (100°C Default)

Register 0x50, Local $\overline{THERM2}$ temperature limit = 0xA4 (100°C Default)

Register 0x51, Remote 1 $\overline{THERM2}$ temperature limit = 0xA4 (100°C Default)

Register 0x52, Remote 2 $\overline{THERM2}$ temperature limit = 0xA4 (100°C Default)

Register 0x53 Remote 3 $\overline{THERM2}$ temperature limit = 0xA4 (100°C Default)

Hysteresis Registers

Register 0x54, Local/Remote 1 Temperature Hysteresis Register

Bits [7:4], Local temperature hysteresis (4°C Default)

Bits [3:0], Remote 1 temperature hysteresis (4°C Default)

Register 0x55, Remote 2/Remote 3 Temperature Hysteresis Register

Bits [7:4], Remote 2 temperature hysteresis (4°C Default)

Bits [3:0], Remote 3 temperature hysteresis (4°C Default)

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended that hysteresis values ever be programmed to 0°C, because this value disables hysteresis. In effect, this value causes the fans to cycle between normal speed and 100% speed, creating unsettling acoustic noise.

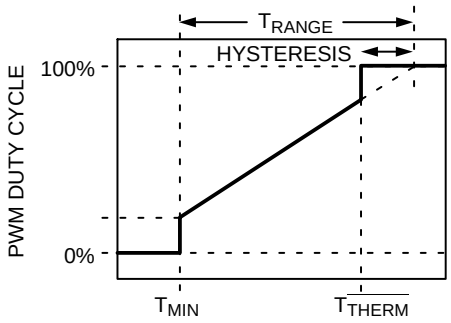


Figure 63. How $T_{\overline{THERM}}$ Relates to Automatic Fan Control

Step 7 − T_{HYST} for Temperature Channels

T_{HYST} is the amount of extra cooling a fan provides after the temperature measured has dropped back below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that without it, the fan would merely chatter or cycle on and off regularly whenever the temperature hovers near the T_{MIN} setting.

The T_{HYST} value chosen determines the amount of time needed for the system to cool down or heat up as the fan is turning on and off. Values of hysteresis are programmable in the range of 1°C to 15°C. Larger values of T_{HYST} prevent the fans from chattering on and off. The T_{HYST} default value is set at 4°C.

Hysteresis Register

Register 0x60, Bits [3:0] Local HYS

Register 0x61, Bits [3:0] Remote 1 HYS

Register 0x62, Bits [3:0] Remote 2 HYS

Register 0x63, Bits [3:0] Remote 3 HYS

In some applications, it is required that fans not turn off below T_{MIN} but remain running at PWM_{MIN}. Bits [1:0] of the PWM1, PWM2 Frequency Register (0x25) and the PWM3, PWM4 Frequency Register (0x26) allow the fans to be turned off or to be kept spinning below T_{MIN}. If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN}.

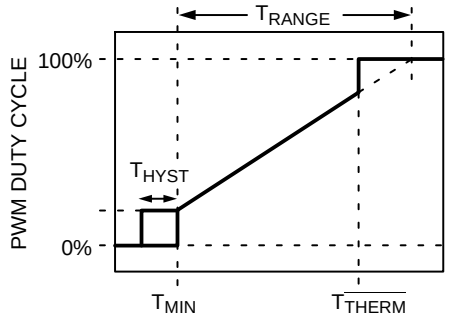


Figure 64. T_{HYST} Value Applies to Fan On/Off Hysteresis

Dynamic T_{MIN} Control Mode

In addition to the automatic fan speed control mode described in the Automatic Fan Control Overview section, the ADT7462 has a mode that extends the basic automatic fan speed control loop. Dynamic T_{MIN} control allows the ADT7462 to intelligently adapt the system's cooling solution for best system performance or lowest possible system acoustics, depending on user or design requirements. Use of dynamic T_{MIN} control alleviates the need to design for worst-case conditions and significantly reduces system design and validation time.

Designing for Worst-Case Conditions

System design must always allow for worst-case conditions. In PC design, the worst-case conditions include, but are not limited to, the following:

- Worst-Case Altitude
  A computer can be operated at different altitudes. Altitude affects the relative air density, which alters the effectiveness of the fan cooling solution. For example, when comparing 40°C air temperature at 10,000 feet to 20°C air temperature at sea level, relative air density is increased by 40%. This means that the fan can spin 40% slower and make less noise at sea level than at 10,000 feet while keeping the system at the same temperature at both locations.
- Worst-Case Fan
  Due to manufacturing tolerances, fan speeds in rpm are normally quoted with a tolerance of ±20%. The designer must assume that the fan rpm can be 20% below tolerance. This translates to reduced system airflow and elevated system temperature. Note that fans 20% out of tolerance can negatively impact system acoustics because they run faster and generate more noise.
- Worst-Case Chassis Airflow
  The same motherboard can be used in a number of different chassis configurations. The design of the chassis and the physical location of fans and components determine the system's thermal characteristics. Moreover, for a given chassis, the addition of add-in cards, cables, or other system configuration options can alter the system airflow and reduce the effectiveness of the system cooling solution. The cooling solution can also be inadvertently altered by the end user. (For example, placing a computer against a wall can block the air ducts and reduce system airflow.)

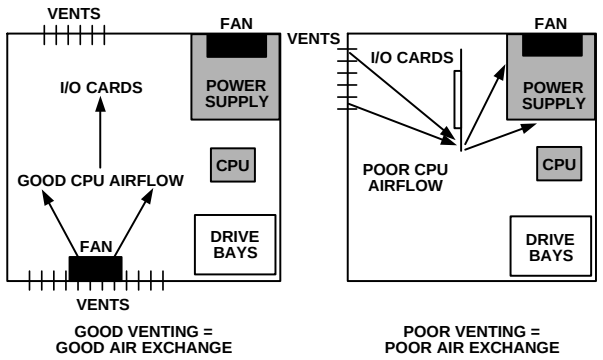


Figure 65. Chassis Airflow Issues

- Worst-Case Processor Power Consumption
  This data sheet maximum does not necessarily reflect the true processor power consumption. Designing for worst-case CPU power consumption can result in a processor becoming over-cooled (generating excess system noise).
- Worst-Case Peripheral Power Consumption
  The tendency is to design to data sheet maximums for peripheral components (again over-cooling the system).
- Worst-Case Assembly
  Every system manufactured is unique because of manufacturing variations. Heat sinks may be loose fitting or slightly misaligned. Too much or too little thermal grease may be used. Variations in application pressure for thermal interface material can affect the efficiency of the thermal solution. Accounting for manufacturing variations in every system is difficult; therefore, the system must be designed for the worst-case.

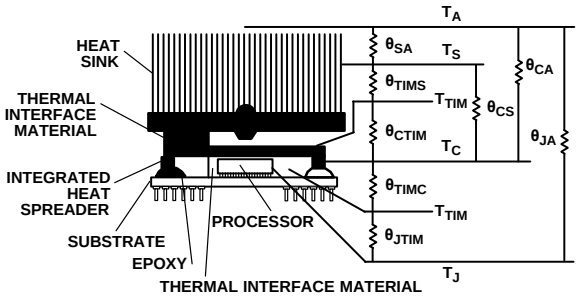


Figure 66. Thermal Model

Although a design usually accounts for worst-case conditions in all these cases, the actual system is almost never operated at worst-case conditions. The alternative to designing for the worst case is to use the dynamic T_{MIN} control function.

Dynamic T_{MIN} Control Overview

Dynamic T_{MIN} control mode builds upon the basic automatic fan control loop by adjusting the T_{MIN} value based on system performance and measured temperature. This is important because, instead of designing for the worst case, the system thermals can be defined as operating zones. The ADT7462 can self-adjust its fan control loop to maintain either an operating zone temperature or a system target temperature. For example, it can be specified that ambient temperature in a system be maintained at 50°C. If the temperature is below 50°C, the fans might not need to run or might run very slowly. If the temperature is higher than 50°C, the fans need to throttle up.

The challenge presented by any thermal design is finding the right settings to suit the system's fan control solution. This can involve designing for the worst case, followed by weeks of system thermal characterization and, finally, fan acoustic optimization (for psycho-acoustic reasons).

Obtaining the greatest benefit from the automatic fan control mode involves characterizing the system to find the best T_{MIN} and T_{RANGE} settings for the control loop and the best PWM_{MIN} value for the quietest fan speed setting. Using the ADT7462 dynamic T_{MIN} control mode, however, shortens the characterization time and alleviates tweaking the control loop settings, because the device can self-adjust during system operation.

Dynamic T_{MIN} control mode is operated by specifying the operating zone temperatures required for the system. Remote 1 and Remote 2 channels have dedicated operating point registers. This allows the system thermal solution to be broken down into distinct thermal zones. For example, CPU operating temperature is 70°C, VRM operating temperature is 80°C, and ambient operating temperature is 50°C. The ADT7462 dynamically alters the control solution to maintain each zone temperature as close as possible to its target operating point.

Figure 67 shows an overview of the parameters that affect the operation of the dynamic T_{MIN} control loop.

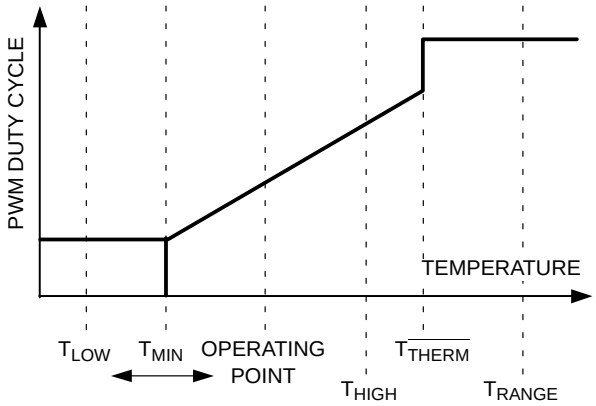


Figure 67. Dynamic T_{MIN} Control Loop

Table 28 provides a brief description of each parameter.

Table 28. T_{MIN} CONTROL LOOP PARAMETERS

Parameter	Description
T_{LOW}	If the temperature drops below the T_{LOW} limit, an error flag is set in a status register and an $\overline{\text{SMBALERT}}$ interrupt can be generated.
T_{HIGH}	If the temperature exceeds the T_{HIGH} limit, an error flag is set in a status register and an $\overline{\text{SMBALERT}}$ interrupt can be generated.
T_{MIN}	The temperature at which the fan turns on under automatic fan speed control.
Operating Point	The maximum target temperature for a particular temperature zone. The system attempts to maintain system temperature around the operating point by adjusting the T_{MIN} parameter of the control loop.
$T_{\overline{THERM}}$	If the temperature exceeds this critical limit, the fans can be run at 100% for maximum cooling.
T_{RANGE}	Programs the PWM duty cycle vs. temperature control slope.

Dynamic T_{MIN} Control Programming

Because the dynamic T_{MIN} control mode is a basic extension of the automatic fan control mode, the automatic fan control mode parameters should be programmed first (see Step 1 − Configuring the MUX through Step 8 − Operating Points for Temperature Channels). Then proceed with dynamic T_{MIN} control mode programming.

Step 8 − Operating Points for Temperature Channels

The operating point for each temperature channel is the optimal temperature for that thermal zone. The hotter each zone is allowed to be, the quieter the system, because the fans are not required to run as fast. The ADT7462 increases or decreases fan speeds as necessary to maintain the operating point temperature, allowing for system-to-system variation and removing the need for worst-case design. If a sensible operating point value is chosen, any T_{MIN} value can be selected in the system characterization. If the T_{MIN} value is too low, the fans run sooner than required, and the temperature is below the operating point. In response, the ADT7462 increases T_{MIN} to keep the fans off longer and to allow the temperature zone to get closer to the operating point. Likewise, too high a T_{MIN} value causes the operating point to be exceeded, and in turn, the ADT7462 reduces T_{MIN} to turn the fans on sooner to cool the system.

Programming the Operating Point Registers

There are two operating point registers, one for the Remote 1 temperature channel and one for the Remote 2 temperature channel. These 8-bit registers allow the operating point temperatures to be programmed with 1°C resolution.

Operating Point Registers

Register 0x5A, Remote 1 Operating Point = 0xA4 (100°C Default)

Register 0x5B, Remote 2 Operating Point = 0xA4 (100°C Default)

Operating Point Hysteresis Register

The operating point hysteresis register sets the value below the operating point at which T_{MIN} begins to reduce.

Register 0x64, Bits [7:4] Operating Point Hysteresis = 0x40 (4°C Default)

Step 9 − High and Low Limits for Temperature Channels

The low limit defines the temperature at which the T_{MIN} value starts to be increased, if temperature falls below this value. This has the net effect of reducing the fan speed, allowing the system to get hotter. An interrupt can be generated when the temperature drops below the low limit.

The high limit should be set above the operating point but below the critical $\overline{\text{THERM}}$ point. An interrupt can be generated when the temperature rises above the high limit.

How Dynamic T_{MIN} Control Works

The basic operation of dynamic T_{MIN} control is as follows:

1. Set the target temperature for the temperature zone, which could be, for example, the Remote 1 thermal diode. This value is programmed to the Remote 1 operating point register.
2. As the temperature in that zone rises toward and exceeds the operating point temperature minus hysteresis, T_{MIN} is reduced and fan speed increases.
3. As the temperature drops below the low limit value, T_{MIN} is increased and the fan speed is reduced.

Short Cycle and Long Cycle

The ADT7462 implements two loops: a short (or decrease) cycle and a long (or increase) cycle. The short cycle takes place every n monitoring cycles. The long cycle takes place every 2n monitoring cycles. The value of n is programmable for each temperature channel. The bits are located at the following register locations.

Dynamic T_{MIN} Control Register 2 (0x0C)

Bits [2:0] (CYR1) = Remote 1

Bits [5:3] (CYR2) = Remote 2

Table 29. CYCLE BIT ASSIGNMENTS

Code	Short Cycle	Duration	Long Cycle	Duration
000	8 cycles	1 sec	16 cycles	2 sec
001	16 cycles	2 sec	32 cycles	4 sec
010	32 cycles	4 sec	64 cycles	8 sec
011	64 cycles	8 sec	128 cycles	16 sec
100	128 cycles	16 sec	256 cycles	32 sec
101	256 cycles	32 sec	512 cycles	64 sec
110	512 cycles	64 sec	1024 cycles	128 sec
111	1024 cycles	128 sec	2048 cycles	256 sec

The cycle time must be chosen carefully. A long cycle time means that T_{MIN} is updated less often. If a system has very fast temperature transients, the dynamic T_{MIN} control loop is always lagging. If a cycle time that is too short is chosen, the full benefit of changing T_{MIN} is not realized and T_{MIN} needs to change again on the next cycle. In effect, it is overshooting. It is necessary to carry out some calibration to identify the most suitable response time.

Figure 68 shows the steps taken during the short cycle.

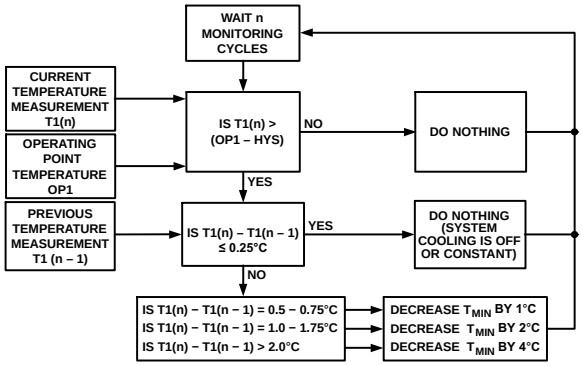


Figure 68. Short Cycle Steps

Figure 69 shows the steps taken during the long cycle.

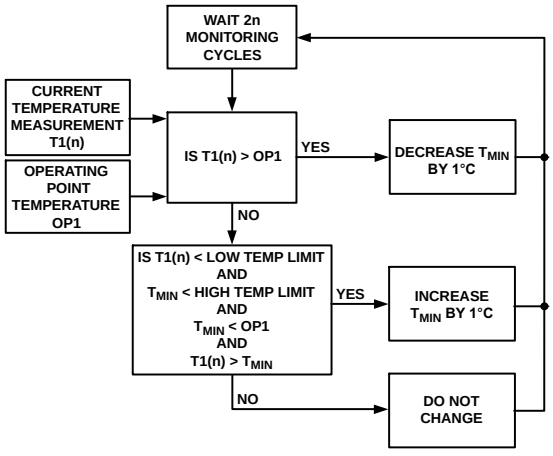


Figure 69. Long Cycle Steps

The following examples illustrate some of the circumstances that may cause T_{MIN} to increase, decrease, or stay the same.

Example 1: Normal Operation, No T_{MIN} Adjustment

1. If the measured temperature never exceeds the programmed operating point minus the hysteresis temperature, T_{MIN} is not adjusted; that is, it remains at its current setting.
2. If the measured temperature never drops below the low temperature limit, T_{MIN} is not adjusted.

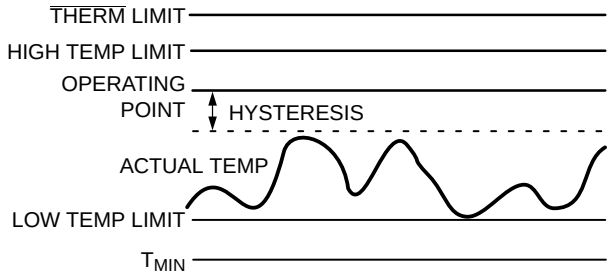


Figure 70. Temperature Between the Operating Point and the Low Temperature Limit

Because neither the operating point minus the hysteresis temperature nor the low temperature limit has been exceeded, the T_{MIN} value is not adjusted, and the fan runs at a speed determined by the fixed T_{MIN} and T_{RANGE} values defined in the automatic fan speed control mode.

Example 2: Operating Point Exceeded, T_{MIN} Reduced

When the measured temperature is below the operating point temperature minus the hysteresis, T_{MIN} remains the same. Once the temperature exceeds the operating temperature minus the hysteresis (OP − Hyst), T_{MIN} starts to decrease as illustrated in Figure 71. This occurs during the short cycle (see Figure 68). The rate at which T_{MIN} decreases depends on the programmed value of n. It also depends on how much the temperature has increased between this monitoring cycle and the last monitoring cycle; that is, if the temperature has increased by 1°C, then T_{MIN} is reduced by 2°C. Decreasing T_{MIN} has the effect of increasing the fan speed, thus providing more cooling to the system.

If the temperature is slowly increasing only in the range (OP − Hyst), that is, ≤0.25°C per short monitoring cycle, then T_{MIN} does not decrease. This allows small changes in temperature in the desired operating zone without changing T_{MIN}. The long cycle makes no change to T_{MIN} in the temperature range (OP − Hyst), because the temperature has not exceeded the operating temperature.

When the temperature exceeds the operating temperature, the long cycle causes T_{MIN} to be reduced by 1°C every long cycle while the temperature remains above the operating temperature. This takes place in addition to the decrease in T_{MIN} that would occur due to the short cycle. In Figure 70, because the temperature is increasing at a rate ≤0.25°C per short cycle, no reduction in T_{MIN} takes place during the short cycle.

When the temperature falls below the operating temperature, T_{MIN} stays the same. Even when the temperature starts to increase slowly, T_{MIN} stays the same, because the temperature increases at a rate of ≤0.25°C per cycle.

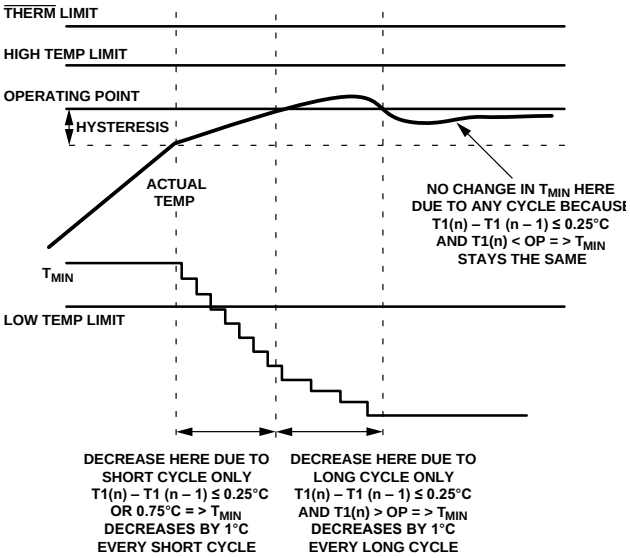


Figure 71. Effect of Exceeding Operating Point Minus Hysteresis Temperature

Example 3: Temperature Below Low Limit, T_{MIN} Increased

When the temperature drops below the low temperature limit, T_{MIN} may increase, as shown in Figure 72. Increasing T_{MIN} has the effect of running the fan more slowly and, therefore, more quietly. The long cycle diagram in Figure 69 shows the conditions that need to be true for T_{MIN} to increase. The following is a quick summary of those conditions and the reasons they need to be true:

T_{MIN} may increase, if

- The measured temperature has fallen below the low temperature limit. This means the user must choose the low limit carefully. It should not be so low that the temperature never falls below it, because T_{MIN} would never increase and the fans would run faster than necessary.
- T_{MIN} is below the high temperature limit. T_{MIN} is never allowed to increase above the high temperature limit. As a result, the high limit should be sensibly chosen, because it determines how high T_{MIN} can go.
- T_{MIN} is below the operating point temperature. T_{MIN} should never be allowed to increase above the operating point temperature, because the fans do not switch on until the temperature rises above the operating point.
- The temperature is above T_{MIN}. The dynamic T_{MIN} control is turned off below T_{MIN}.

Figure 72 shows how T_{MIN} increases when the current temperature is above T_{MIN} and below the low temperature limit, and T_{MIN} is below the high temperature limit and below the operating point. When the temperature rises above the low temperature limit, T_{MIN} stays the same.

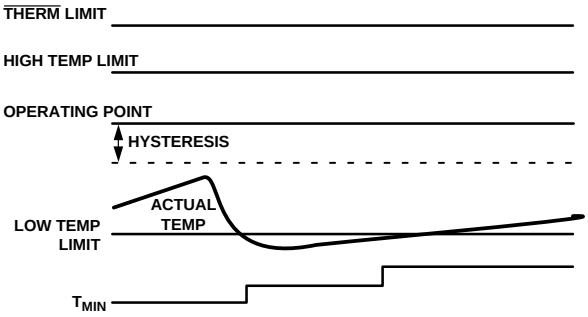


Figure 72. Increasing T_{MIN} for Quieter Operation

Example 4: Preventing T_{MIN} from Reaching Full Scale

Because T_{MIN} is dynamically adjusted, it is undesirable for T_{MIN} to reach full scale (191°C), because the fan would never switch on. As a result, T_{MIN} is allowed to vary only within a specified range.

- The lowest possible value for T_{MIN} is −64°C.
- T_{MIN} cannot exceed the high temperature limit.
- If the temperature is below T_{MIN}, the fan is switched off or is running at minimum speed, and dynamic T_{MIN} control is disabled.

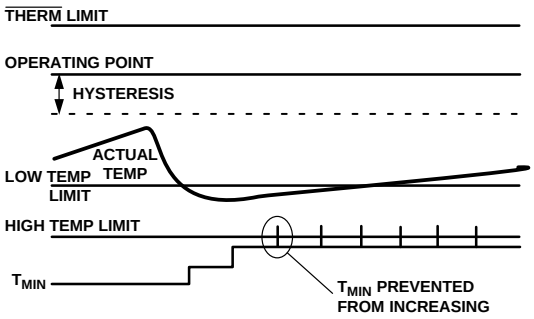


Figure 73. T_{MIN} Adjustments Limited by High Temperature Limit

Enabling Dynamic T_{MIN} Control Mode

Bits [1:0] of Dynamic T_{MIN} Control Register 1 (0x0B) enable/disable dynamic T_{MIN} control on the temperature channels (see Table 43).

Dynamic T_{MIN} Control Register 1 (0x0B)

Bit 1 (Remote 2 En) = 1 enables dynamic T_{MIN} control on the Remote 2 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.

Bit 1 (Remote 2 En) = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted and the channel behaves as described in the Automatic Fan Control Overview section.

Bit 0 (Remote 1 En) = 1 enables dynamic T_{MIN} control on the Remote 1 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.

Bit 0 (Remote 1 En) = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control Overview section.

Step 10 − Monitoring $\overline{\text{THERM}}$

Using the operating point limit ensures that the dynamic T_{MIN} control mode is operating in the best possible acoustic position, while ensuring that the temperature never exceeds the maximum operating temperature. Using the operating point limit allows T_{MIN} to be independent of system-level issues because of its self-corrective nature. In PC design, the operating point for the chassis is usually the worst-case internal chassis temperature.

The optimal operating point for the processor is determined by monitoring the thermal monitor in the Intel Pentium® 4 processor. To do this, the $\overline{\text{PROCHOT}}$ output of the Pentium® 4 is connected to the $\overline{\text{THERM}}$ input of the ADT7462.

The operating point for the processor can be determined by allowing the current temperature to be copied to the operating point register when the $\overline{\text{PROCHOT}}$ output pulls the $\overline{\text{THERM}}$ input low on the ADT7462. This gives the maximum temperature at which the Pentium® 4 can run before clock modulation occurs.

Enabling the $\overline{\text{THERM}}$ Trip Point as the Operating Point

Bits [5:2] of Dynamic T_{MIN} Control Register 1 (0x0B) enable/disable $\overline{\text{THERM}}$ monitoring to program the operating point. Table 43 details how the remote temperatures can be copied into the operating point registers on a $\overline{\text{THERM}}$ assertion. Setting these bits to 1 uses the remote temperature as the operating point temperature, overwriting the programmed operating point value in the event of a $\overline{\text{THERM}}$ assertion. Setting these bits to 0 ignores a $\overline{\text{THERM}}$ assertion, and the operating point register remains at the programmed value.

Enhancing System Acoustics

Automatic fan speed control mode reacts instantaneously to changes in temperature; that is, the PWM duty cycle responds immediately to temperature change. Any impulses in temperature can cause an impulse in fan noise. For psycho-acoustic reasons, the ADT7462 can prevent the PWM output from reacting instantaneously to temperature changes. Enhanced acoustic mode controls the maximum change in PWM duty cycle at a given time. The objective is to prevent the fan from cycling up and down, annoying the user.

Acoustic Enhancement Mode Overview

Figure 74 gives a top-level overview of the automatic fan control circuitry on the ADT7462 and shows where acoustic enhancement fits in. Acoustic enhancement is intended as a post-design tweak made by a system or mechanical engineer evaluating best settings for the system. Having determined the optimal settings for the thermal solution, the engineer can adjust the system acoustics. The goal is to implement a system that is acoustically pleasing without causing user annoyance due to fan cycling. It is important to realize that although a system might pass an acoustic noise requirement specification (for example, 36 dB), if the fan is annoying, it fails the consumer test.

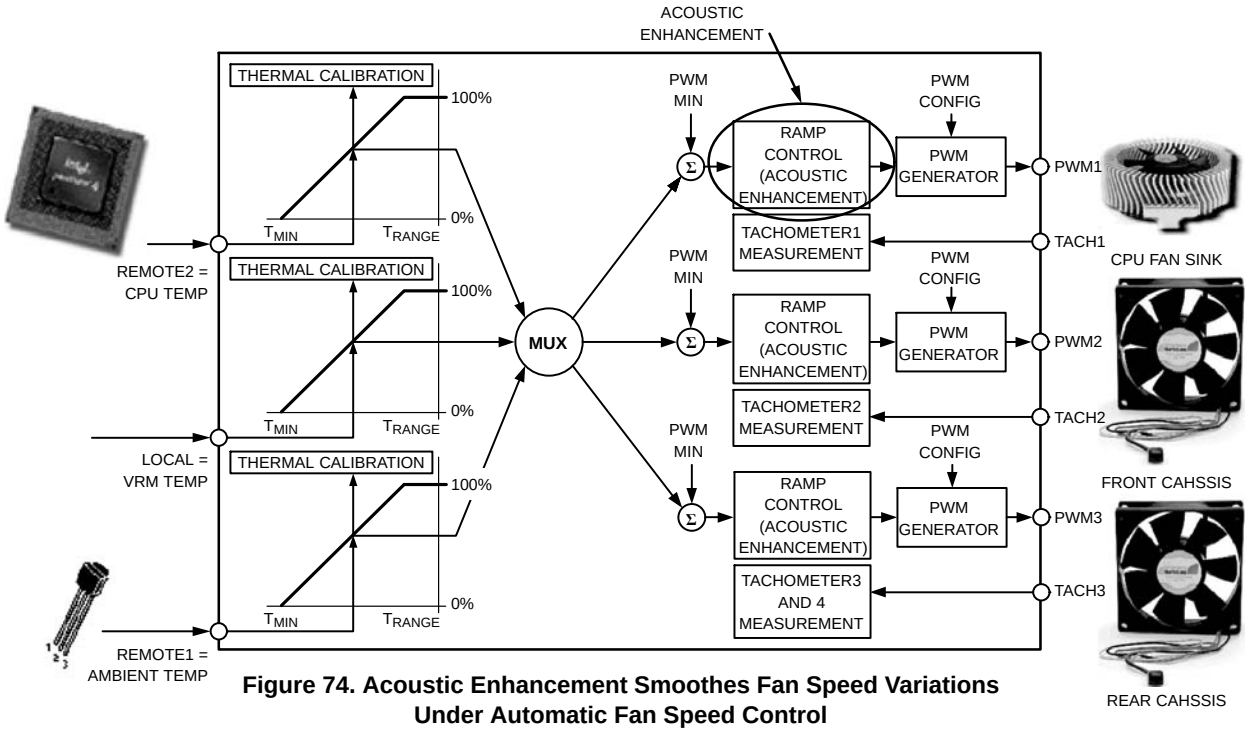


Figure 74. Acoustic Enhancement Smoothes Fan Speed Variations Under Automatic Fan Speed Control

Approaches to System Acoustic Enhancement

There are two different approaches to implementing system acoustic enhancement: temperature-centric and fan-centric.

The temperature-centric approach involves smoothing transient temperatures as they are measured by a temperature source (for example, Remote 1 temperature). The temperature values used to calculate the PWM duty cycle values are smoothed, reducing fan speed variation. However, this approach causes an inherent delay in updating fan speed and causes the thermal characteristics of the system to change. It also causes the system fans to stay on longer than necessary, because the fan's reaction is merely delayed. The user has no control over noise from different fans driven by the same temperature source. Consider, for example, a system in which control of a CPU cooler fan (on PWM1) and a chassis fan (on PWM2) uses Remote 1 temperature. Because the Remote 1 temperature is smoothed, both fans are updated at exactly the same rate. If the chassis fan is much louder than the CPU fan, there is no way to improve its acoustics without changing the thermal solution of the CPU cooling fan.

The fan-centric approach to system acoustic enhancement controls the PWM duty cycle, driving the fan at a fixed rate (for example, 6%). Each time the PWM duty cycle is updated, it is incremented by a fixed 6%. As a result, the fan ramps smoothly to its newly calculated speed. If the temperature starts to drop, the PWM duty cycle immediately decreases by 6% at every update. Therefore, the fan ramps smoothly up or down without inherent system delay.

Consider, for example, controlling the same CPU cooler fan (on PWM1) and chassis fan (on PWM2) using Remote 1 temperature. The T_{MIN} and T_{RANGE} settings have already been defined in automatic fan speed control mode; that is, thermal characterization of the control loop has been optimized. The chassis fan is noisier than the CPU cooling fan. Using the fan-centric approach, PWM2 can be placed into acoustic enhancement mode independently of PWM1. The acoustics of the chassis fan can, therefore, be adjusted without affecting the acoustic behavior of the CPU cooling fan, even though both fans are controlled by Remote 1 temperature. The fan centric approach is how acoustic enhancement works on the ADT7462.

Enabling Acoustic Enhancement for Each PWM Output

Enhanced Acoustics Register 1 (0x1A)

Bit 0 (En1) = 1 enables acoustic enhancement on PWM1 output.

Bit 1 (En2) = 1 enables acoustic enhancement on PWM2 output.

Enhanced Acoustics Register 2 (0x1B)

Bit 0 (En3) = 1 enables acoustic enhancement on PWM3 output.

Bit 1 (En4) = 1 enables acoustic enhancement on PWM4 output.

Effect of Ramp Rate on Enhanced Acoustic Mode

The PWM signal driving the fan has a period, t, given by the PWM drive frequency, f, because t = 1/f. For a given PWM period, t, the PWM period is subdivided into 255 equal time slots. One time slot corresponds to the smallest possible increment in the PWM duty cycle. A PWM signal of 33% duty cycle is, therefore, high for $1/3 \times 255$ time slots and low for $2/3 \times 255$ time slots. Therefore, a 33% PWM duty cycle corresponds to a signal that is high for 85 time slots and low for 170 time slots.

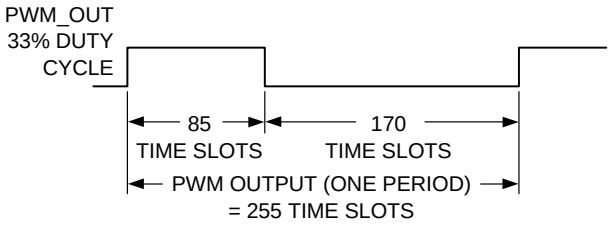


Figure 75. 33% PWM Duty Cycle Represented in Time Slots

The ramp rates in the enhanced acoustics mode are selectable from 1 to 8. The ramp rates are discrete time slots. For example, if the ramp rate is 8, then eight time slots are added to the PWM high duty cycle each time the PWM duty cycle needs to be increased. If the PWM duty cycle value needs to be decreased, it is decreased by eight time slots. Figure 76 shows how the enhanced acoustics mode algorithm operates.

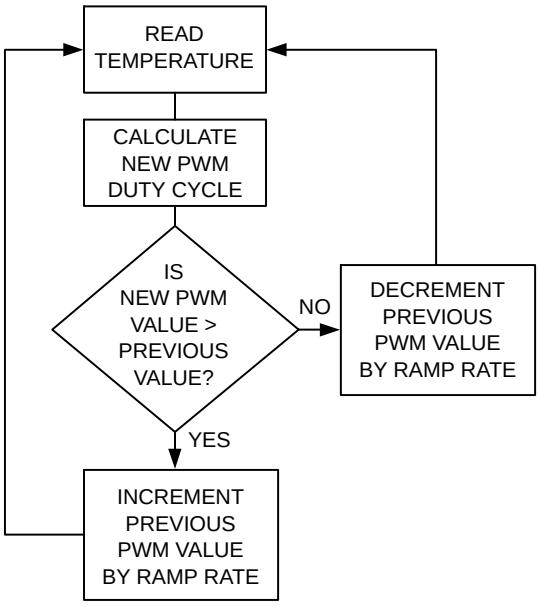


Figure 76. Enhanced Acoustics Mode Algorithm

The enhanced acoustics mode algorithm calculates a new PWM duty cycle based on the temperature measured. If the new PWM duty cycle value is greater than the previous PWM value, the previous PWM duty cycle value is incremented by either 1, 2, 3, 5, 8, 12, 24, or 48 time slots, depending on the settings of the enhanced acoustics registers. If the new PWM duty cycle value is less than the

previous PWM value, the previous PWM duty cycle is decremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots. Each time the PWM duty cycle is incremented or decremented, its value is stored as the previous PWM duty cycle for the next comparison.

A ramp rate of 1 corresponds to one time slot, which is 1/255 of the PWM period. In enhanced acoustics mode, incrementing or decrementing by 1 changes the PWM output by 1/255 × 100%.

Step 11 − Ramp Rate for Acoustic Enhancement

The optimal ramp rate for acoustic enhancement can be found through system characterization after the thermal optimization has been finished. The effect of each ramp rate should be logged, if possible, to determine the best setting for a given solution.

Enhanced Acoustics Register 1 (0x1A)

Bits [4:2] RR1 select the ramp rate for PWM1.

000 = 1 time slot = 35 seconds
001 = 2 time slots = 17.6 seconds
010 = 3 time slots = 11.8 seconds
011 = 5 time slots = 7 seconds
100 = 8 time slots = 4.4 seconds
101 = 12 time slots = 3 seconds
110 = 24 time slots = 1.6 seconds
111 = 48 time slots = 0.8 seconds

Bits [7:5] RR2 select the ramp rate for PWM2.

000 = 1 time slot = 35 seconds
001 = 2 time slots = 17.6 seconds
010 = 3 time slots = 11.8 seconds
011 = 5 time slots = 7 seconds
100 = 8 time slots = 4.4 seconds
101 = 12 time slots = 3 seconds
110 = 24 time slots = 1.6 seconds
111 = 48 time slots = 0.8 seconds

Enhanced Acoustics Register 2 (0x1B)

Bits [4:2] RR3 select the ramp rate for PWM3.

000 = 1 time slot = 35 seconds
001 = 2 time slots = 17.6 seconds
010 = 3 time slots = 11.8 seconds
011 = 5 time slots = 7 seconds
100 = 8 time slots = 4.4 seconds
101 = 12 time slots = 3 seconds
110 = 24 time slots = 1.6 seconds
111 = 48 time slots = 0.8 seconds

Bits [7:5] RR4 select the ramp rate for PWM4.

000 = 1 time slot = 35 seconds
001 = 2 time slots = 17.6 seconds
010 = 3 time slots = 11.8 seconds
011 = 5 time slots = 7 seconds
100 = 8 time slots = 4.4 seconds
101 = 12 time slots = 3 seconds
110 = 24 time slots = 1.6 seconds
111 = 48 time slots = 0.8 seconds

Another way to view the ramp rates is to measure the time it takes for the PWM output to ramp up from 0% to 100% duty cycle for an instantaneous change in temperature. This can be tested by putting the ADT7462 into manual mode and changing the PWM output from 0% to 100% PWM duty cycle. The PWM output takes 35 seconds to reach 100% when a ramp rate of one time slot is selected.

Figure 77 shows remote temperature plotted against PWM duty cycle for enhanced acoustics mode. The ramp rate is set to 48, which corresponds to the fastest ramp rate. Assume that a new temperature reading is available every 115 ms. With these settings, it takes approximately 0.76 seconds to go from 33% duty cycle to 100% duty cycle (full speed). Even though the temperature increases very rapidly, the fan ramps up to full speed gradually.

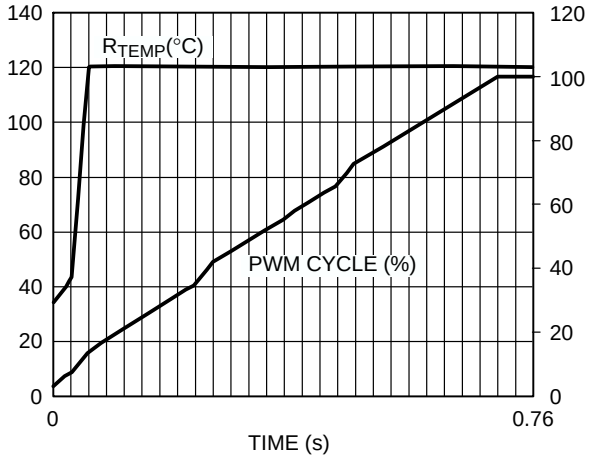


Figure 77. Enhanced Acoustics Mode with Ramp Rate = 48

Figure 78 shows how changing the ramp rate from 48 to 8 affects the control loop. The overall response of the fan is slower. Because the ramp rate is reduced, it takes longer for the fan to achieve full running speed. In this case, it takes approximately 4.4 seconds for the fan to reach full speed.

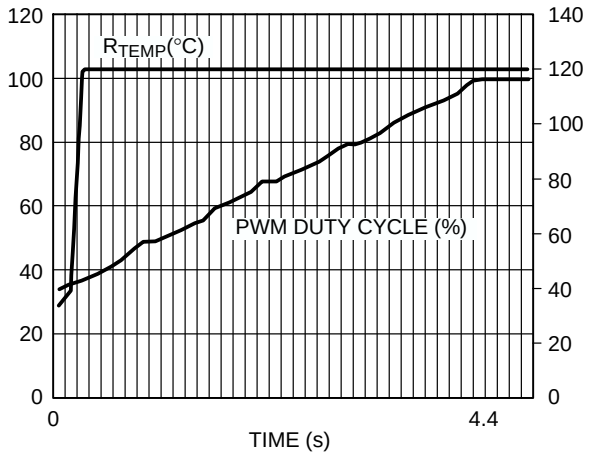


Figure 78. Enhanced Acoustics Mode with Ramp Rate = 8

Figure 79 shows the PWM output response for a ramp rate of 2. In this instance, the fan takes about 17.6 seconds to reach full running speed.

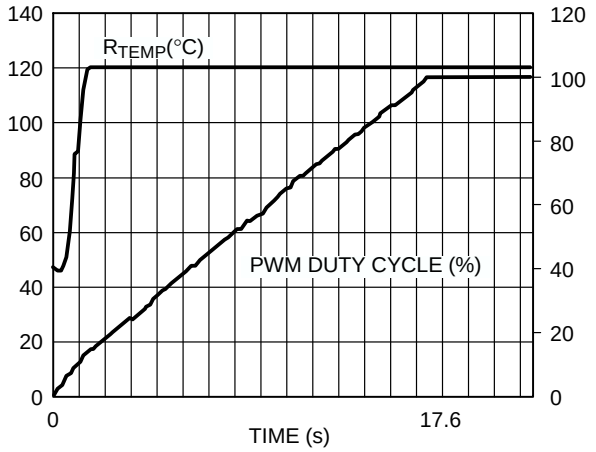


Figure 79. Enhanced Acoustics Mode with Ramp Rate = 2

Figure 80 shows how the control loop reacts to temperature with the slowest ramp rate. The ramp rate is set to 1, while all other control parameters remain the same. With the slowest ramp rate selected, it takes 35 seconds for the fan to reach full speed.

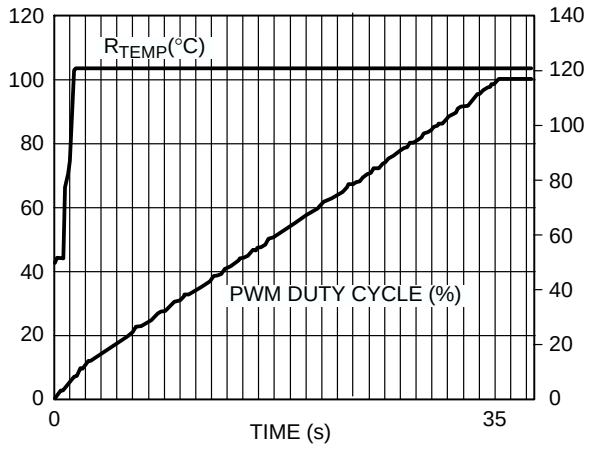


Figure 80. Enhanced Acoustics Mode with Ramp Rate = 1

As Figure 77 to Figure 80 show, the rate at which the fan reacts to temperature change is dependent on the ramp rate selected in the enhanced acoustics registers. The higher the ramp rate, the faster the fan reaches the newly calculated fan speed.

Figure 81 shows the behavior of the PWM output as temperature varies. As the temperature increases, the fan speed ramps up. Small drops in temperature do not affect the ramp-up function, because the newly calculated fan speed is still higher than the previous PWM value. Enhanced acoustics mode allows the PWM output to be made less sensitive to temperature variations. This is dependent on the ramp rate selected and programmed into the enhanced acoustics registers.

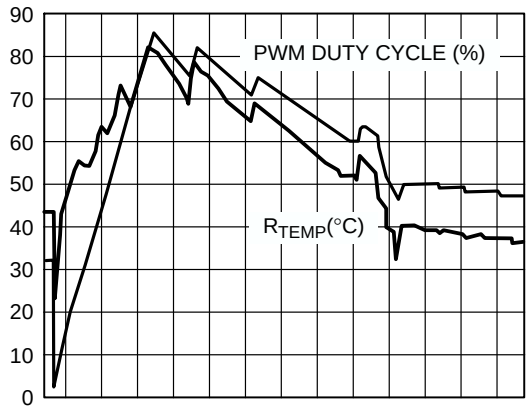


Figure 81. How Fan Reacts to Temperature Variations in Enhanced Acoustics Mode

Slower Ramp Rates

The ADT7462 can be programmed for much longer ramp times by slowing the ramp rates. Each ramp rate can be slowed by a factor of 4.

PWM1 Configuration Register (0x21)

PWM2 Configuration Register (0x22)

PWM3 Configuration Register (0x23)

PWM4 Configuration Register (0x24)

Setting Bit 3 (the SLOW bit) to 1 in the PWM1 to PWM4 configuration registers slows the ramp rate for PWM1 to PWM4 by 4.

Fan Freewheeling Test Mode

The fan freewheeling test mode is intended to diagnose whether fans connected to the ADT7462 are working properly. It is particularly useful where fans coupled in the duct can affect the airflow of another fan. If one fan has failed, it may not be apparent, because moving air from other fans can cause air to flow through the faulty fan, which in turn can cause the faulty fan to rotate.

The fan freewheeling test is most useful in a system using primary and redundant setup. In such a system, the following setup is recommended. The primary fans are Fan 1, Fan 2, Fan 3, and Fan 4. The redundant fans are Fan 5, Fan 6, Fan 7, and Fan 8. In this setup, each primary and redundant fan can be driven separately because they are driven by different PWMs.

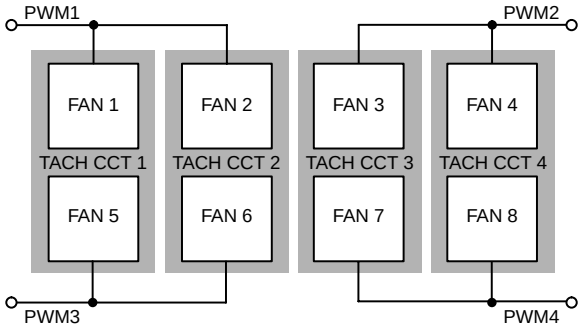


Figure 82. Fan Freewheeling Test Mode Setup

The freewheeling test procedure is as follows:

1. PWM1 and PWM2 go to full speed, and PWM3 and PWM4 are switched off.
2. After the spin-up time of PWM1 and PWM2 has elapsed, the speed of Fan 1, Fan 2, Fan 3, and Fan 4 is measured.
3. After the speed of Fan 1 and Fan 2 is measured, PWM1 is switched off and PWM3 is spun up. After the spin-up time for PWM3 has elapsed, the speed of Fan 5 and Fan 6 is measured.
4. After the speed of Fan 3 and Fan 4 is measured, PWM2 is switched off and PWM4 is switched on. After the spin-up time of PWM4 has elapsed, the speed of Fan 7 and Fan 8 is measured.
5. After the speed of all eight fans has been measured, the TACH and PWM configurations return to their previous values.
   - Fans must be in continuous mode for the freewheeling test; that is, the dc bits must be set (Register 0x08).
   - To enable the freewheeling test, set the freewheeling test enable register (0x1E) to a nonzero value. Set Bit 0 = 1 to enable the freewheeling test for Fan 1, and set Bit 1 for Fan 2, all the way to Bit 7 for Fan 8. The freewheeling test enable register should be programmed after the fans present register is programmed. If the fans present register is not programmed first, then the values in the two registers do not match, and the ADT7462 assumes that a fan is missing.

The following registers must be programmed for the fan freewheeling test:

Fans Present Register (0x1D)

Set Bit 0 to 1 when a fan is connected to TACH1.
Set Bit 1 to 1 when a fan is connected to TACH2.
Set Bit 2 to 1 when a fan is connected to TACH3.
Set Bit 3 to 1 when a fan is connected to TACH4.
Set Bit 4 to 1 when a fan is connected to TACH5.
Set Bit 5 to 1 when a fan is connected to TACH6.
Set Bit 6 to 1 when a fan is connected to TACH7.
Set Bit 7 to 1 when a fan is connected to TACH8.

Fan Freewheeling Test Enable Register (0x1E)

Set Bit 0 to 1 to enable the freewheeling test for Fan 1.
Set Bit 1 to 1 to enable the freewheeling test for Fan 2.
Set Bit 2 to 1 to enable the freewheeling test for Fan 3.
Set Bit 3 to 1 to enable the freewheeling test for Fan 4.
Set Bit 4 to 1 to enable the freewheeling test for Fan 5.
Set Bit 5 to 1 to enable the freewheeling test for Fan 6.
Set Bit 6 to 1 to enable the freewheeling test for Fan 7.
Set Bit 7 to 1 to enable the freewheeling test for Fan 8.

Fan Freewheeling Test Register (0x1C)

Both the Fans Present register (0x1D) and the freewheeling test enable register (0x1E) should be programmed before setting the relevant bits in the fan freewheeling test register (0x1C). The host fan status register (0xBD) should be read directly after completion of the test.

$\overline{\text{THERM}}$ I/O Operation

This section describes the operation of $\overline{\text{THERM1}}$ and $\overline{\text{THERM2}}$. Pin 28 and Pin 29 can both be configured as $\overline{\text{THERM}}$ inputs or outputs.

$\overline{\text{THERM}}$ Output

$\overline{\text{THERM}}$ is not enabled as an output by default on powerup, but it can be enabled by setting the appropriate bits in Register 0x0E ($\overline{\text{THERM1}}$ configuration register) and Register 0x0F ($\overline{\text{THERM2}}$ configuration register). $\overline{\text{THERM1}}$ and $\overline{\text{THERM2}}$ can be configured to assert whenever a specific channel exceeds the specified $\overline{\text{THERM}}$ limit (see Table 30).

Table 30. $\overline{\text{THERM}}$ OUTPUT CHANNEL SELECT AND LIMITS

Channel Enable	Configuration		Limit Registers	
	$\overline{\text{THERM1}}$, Register 0x0E	$\overline{\text{THERM2}}$, Register 0x0F	$\overline{\text{THERM1}}$	$\overline{\text{THERM2}}$
Local	Bit 1 = 1	Bit 1 = 1	0x4C	0x50
Remote 1	Bit 2 = 1	Bit 2 = 1	0x4D	0x51
Remote 2	Bit 3 = 1	Bit 3 = 1	0x4E	0x52
Remote 3	Bit 4 = 1	Bit 4 = 1	0x4F	0x53

As an output, $\overline{\text{THERM}}$ is asserted low to signal that the measured $\overline{\text{THERM}}$ temperature has exceeded pre-programmed $\overline{\text{THERM}}$ temperature limits. The output is automatically pulled high again when the temperature falls below the ($\overline{\text{THERM}}$ − Hysteresis) limit. The value of hysteresis for each channel is programmable in Register 0x54 and Register 0x55, where 1 LSB = 1°C, and the maximum hysteresis for each channel is 15°C.

Setting the $\overline{\text{THERM}}$ boost bits, Bit 0 and Bit 1, to Logic 0 (default setting) in the $\overline{\text{THERM}}$ configuration register (0x0D), sets the fans to full speed on an internal $\overline{\text{THERM}}$ event.

$\overline{\text{THERM}}$ Input

To configure $\overline{\text{THERM}}$ as an input, the $\overline{\text{THERM1}}$_Timer_Enable (T1TE) bit (Bit 0) in the $\overline{\text{THERM1}}$ configuration register (0x0E) and the $\overline{\text{THERM2}}$_Timer_Enable (T2TE) bit (Bit 0) in the $\overline{\text{THERM2}}$ configuration register (0x0F) must be set to Logic 1. The ADT7462 can then be used to detect when the $\overline{\text{THERM}}$ pins are asserted low. The $\overline{\text{THERM}}$ pins can be connected to a trip point temperature sensor or to the $\overline{\text{PROCHOT}}$ output of a CPU.

With processor core voltages reducing all the time, the threshold for the AGTL + $\overline{\text{PROCHOT}}$ output is also reduced as new processors become available.

Because the $\overline{\text{THERM}}$ input is typically an AGTL + input, the thresholds can be referenced to V_{CCP}. By setting Bit 4 of Configuration Register 3 (0x03) to 1, the $\overline{\text{THERM}}$ threshold

is 2/3 × V_{CCP}, the correct threshold for an AGTL + signal. The $\overline{\text{THERM}}$ assert bits in Host Thermal Status Register 2 (0xB9) are set to Logic 1 whenever the $\overline{\text{THERM}}$ input is asserted low. The $\overline{\text{THERM}}$ state bits in Host Thermal Status Register 2 (0xB9) indicate that a high-to-low transition has taken place on the $\overline{\text{THERM}}$ pin.

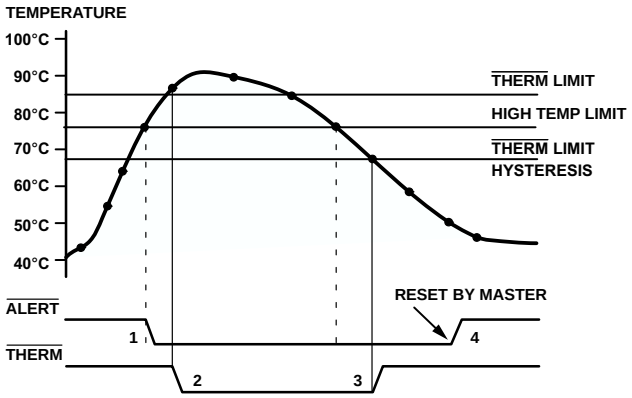


Figure 83. $\overline{\text{THERM}}$ Behavior

$\overline{\text{THERM}}$ Timer

The ADT7462 can also measure assertion times on the $\overline{\text{THERM}}$ inputs as a percentage of a timer window. The timer window for the $\overline{\text{THERM1}}$ input is programmed using Bits [4:2] of the $\overline{\text{THERM}}$ configuration register (0x0D). The timer window for the $\overline{\text{THERM2}}$ input is programmed using Bits [7:5] of the $\overline{\text{THERM}}$ configuration register (0x0D). Values from 0.25 sec to 8 sec are programmable (see Table 31).

Table 31. $\overline{\text{THERM}}$ TIMER WINDOW

Code	$\overline{\text{THERM}}$ Timer Window
000	0.25 sec
001	0.5 sec
010	1 sec
011	2 sec
100	4 sec
101	8 sec
110	8 sec
111	8 sec

The assertion time as a percentage of the timer window is stored in the $\overline{\text{THERM}}$ % on-time registers. This is a cumulative sum of the percentage of time during the $\overline{\text{THERM}}$ timer window that $\overline{\text{THERM}}$ is asserted. The % on-time and associated timer limit registers are listed in Table 32.

Table 32. $\overline{\text{THERM}}$ ON-TIME AND TIMER LIMIT REGISTER

Channel	% On-Time Register	% Timer Limit Register
$\overline{\text{THERM1}}$	0xAE	0x80
$\overline{\text{THERM2}}$	0xAF	0x81

When the measured percentage exceeds the corresponding percentage limit, the T1% bit in Host Thermal Status Register 2 (0xB9) is asserted, and an $\overline{\text{ALERT}}$ is generated (that is, if the mask bit is not set). If the limit is set to 0x00, an $\overline{\text{ALERT}}$ is generated on the first assertion. If the limit is set to 0xFF, an $\overline{\text{ALERT}}$ is never generated because 0xFF corresponds to the $\overline{\text{THERM}}$ input being asserted all the time.

When $\overline{\text{THERM}}$ is configured as an input only, setting Bits [4:1] of the $\overline{\text{THERM}}$ zone in the $\overline{\text{THERM1}}$ configuration register (0x0E) and the $\overline{\text{THERM2}}$ configuration register (0x0F) allows Pin 28/Pin 29 to operate as an I/O.

$\overline{\text{THERM}}$ Timer Limit Register

The $\overline{\text{THERM}}$ timer limit is programmed to Register 0x80 and Register 0x81. If $\overline{\text{THERM}}$ is asserted for longer than the programmed percentage limit, then an $\overline{\text{ALERT}}$ is generated. The limit is programmed as a percentage of the chosen $\overline{\text{THERM}}$ timer window.

EXAMPLE: The $\overline{\text{THERM}}$ timer window is eight seconds, and an $\overline{\text{ALERT}}$ should be generated if $\overline{\text{THERM}}$ is asserted for more than one second.

$$\%\text{Limit} = \frac{1}{8} \times 100 = 12.5\%$$

The $\overline{\text{THERM}}$ timer limit register is an 8−bit register.

$$0 \times 00 = 0\%;\ 0 \times \text{FF} = 100\%$$

Therefore, 1 LSB = 0.39%

$$\frac{12.5\%}{0.39\%} = 32 \text{ decimal} = 0 \times 20 = 00100000$$

When the time window has elapsed, if the $\overline{\text{THERM}}$ limit has been exceeded, then an $\overline{\text{ALERT}}$ is generated.

General-Purpose I/O Pins

The ADT7462 has eight open-drain GPIO pins. GPIO1 to GPIO4 can be configured to enable event driven outputs (EDOs), and GPIO5 and GPIO6 can act as EDOs, if the EDO functionality is enabled. Two other GPIOs (GPIO7 and GPIO8) are standard GPIO pins that are dedicated to general-purpose logic input/output.

Each GPIO pin has five data bits associated with it: three bits in a GPIO configuration register (0x09 and 0x0A), one in the GPIO status register (0xBF), and one in the GPIO mask register (0x36).

Setting a direction bit to 1 in a GPIO configuration register makes the corresponding GPIO pin an output.

Clearing the direction bit to 0 makes the corresponding GPIO pin an input.

Setting a polarity bit to 1 in a GPIO configuration register makes the corresponding GPIO pin active high.

Clearing the polarity bit to 0 makes the corresponding GPIO pin active low.

When a GPIO pin is configured as an input, the corresponding bit in the GPIO status register is read-only, and it is set when the input is asserted (“asserted” can be high or low, depending on the setting of the polarity bit).

When a GPIO pin is configured as an output, the corresponding bit in the GPIO status register becomes read/write. Setting this bit then asserts the GPIO output. (Again, “asserted” can be high or low, depending on the setting of the polarity bit.) The effect of a GPIO status register bit on the $\overline{\text{ALERT}}$ output can be masked by setting the corresponding bit in one of the GPIO mask registers.

When the pin is configured as an output, the corresponding status bit is automatically masked to prevent the data written to the status bit from causing an interrupt. When configured as inputs, the GPIO pins can be connected to external interrupt sources such as temperature sensors with digital output.

EDO Circuitry

The ADT7462 has the added functionality that the assertion of one of the four GPIOs (GPIO1 to GPIO4) can be used to latch one of the two EDOs high or low. The ADT7462 has two EDO event mask registers (0x37 and 0x38): one mask for each EDO. See Table 33 for an explanation of event mask register functionality.

The polarity of the EDOs is set in the GPIO configuration registers (0x09 and 0x0A).

Setting a polarity bit to 1 in one of the GPIO configuration registers makes the corresponding GPIO pin active high.

Clearing the polarity bit to 0 makes it active low.

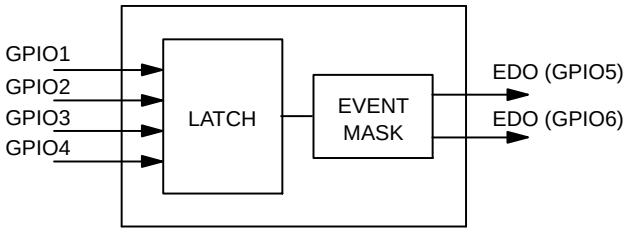


Figure 84. EDO Circuit

Bits [7:5] of each event mask register (0x37 and 0x38) allow the EDO output to be driven high or low (depending on the polarity bit of the configuration register) and latched (depending on the EDO latch bit of the configuration register), if the ADT7462 detects an overtemperature, an over/undervoltage, or a fan failure condition.

Table 33. EDO CONTROL (MASK) REGISTER 0X37 AND REGISTER 0X38

Bit 7: Overvoltage/ Undervoltage	Bit 6: $\overline{\text{THERM}}$	Bit 5: Fan Fail	Bit 3	Bit 2	Bit 1	Bit 0	Behavior: What Drives and Latches Output X (G = GPIO)
0 = Drive Output X	0 = Drive Output X	0 = Drive Output X	0	0	0	0	G4 or G3 or G2 or G1
1 = Ignore Event	1 = Ignore Event	1 = Ignore Event	0	0	0	1	G4 or G3 or G2
			0	0	1	0	G4 or G3 or G1
			0	0	1	1	G4 or G3
			0	1	0	0	G4 or G2 or G1
			0	1	0	1	G4 or G2
			0	1	1	0	G4 or G1
			0	1	1	1	G4
			1	0	0	0	G3 or G2 or G1
			1	0	0	1	G3 or G2
			1	0	1	0	G3 or G1
			1	0	1	1	G3
			1	1	0	0	G2 or G1
			1	1	0	1	G2
			1	1	1	0	G1
			1	1	1	1	GPIO Events Ignored by Output X

Table 33 shows that any of the four designated GPIO pins can be used to set or reset either one of the two EDO outputs.

Using this functionality, it is possible to have the ADT7462 drive LEDs or signals based on rules. For example, if a GPIO1 (power fail), a GPIO2 (overcurrent), or an overtemperature condition occurs, EDO1 (power supply fault LED) can be latched. This does not require software handling and makes the part more autonomous.

Other Digital Inputs

The ADT7462 contains other specific digital inputs that can be found on PC motherboards. These inputs can be monitored and configured for actions to occur on their assertion.

VR_HOT Inputs

Pin 25 and Pin 26 can be configured as VR_HOT inputs. These are specific digital signals from the CPU voltage regulator that indicate an overtemperature. On assertion of these inputs, the relevant status bits are set in Thermal Status Register 2 (Host Register 0xB9 or BMC Register 0xC1). Assertion of these inputs can also be used to boost the fans to full speed, thus providing emergency cooling in the event of VR overtemperature. This is set using Bit 3 (VRD1) and Bit 4 (VRD2) of Configuration Register 2 (0x02). There is also an associated mask bit in Register 0x31 to mask the assertion of these inputs from the $\overline{\text{ALERT}}$ output.

SCSI_TERM Inputs

Pin 16 and Pin 20 can be configured as SCSI_TERM inputs. An assertion on the SCSI_TERM is recorded in Bit 4 and Bit 5 of Host Digital Status Register (0xBE) or BMC Digital Status Register (0xC6). There is also an associated mask bit in Register 0x35 to mask the assertion of these inputs from the $\overline{\text{ALERT}}$ output.

Reset I/O

The ADT7462 includes an active low reset pin (Pin 14). The $\overline{\text{RESET}}$ pin can be both a reset input and output. $\overline{\text{RESET}}$ monitors the V_{CC} input to the ADT7462. At powerup, $\overline{\text{RESET}}$ is asserted (pulled low) until 180 ms after the power supply has risen above the supply threshold. A power-on reset initializes all registers to the default values.

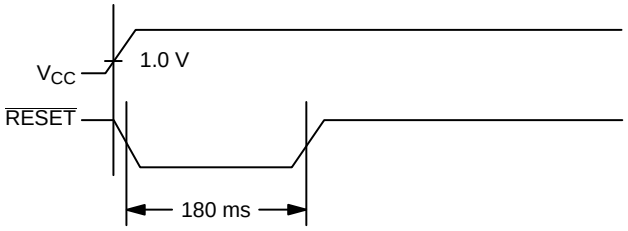


Figure 85. Operation of $\overline{\text{RESET}}$ Output on Powerup

The $\overline{\text{RESET}}$ pin can also function as a reset input. Pulling this pin low externally resets the ADT7462. The user should wait at least 180 ms after powerup before doing a hardware reset. The reset pulse width should be greater than 0.8 ms to ensure that a reset is registered.

A hardware reset differs from a power-on reset in that not all of the registers are reinitialized to the default values. For example, limit registers are not all restored to the default values. This can be useful if the user needs to reset the part but does not want to completely reprogram the device. The Register Map section show, which registers, are reset. Locked registers are not restored to default values by a hardware reset.

Note that if two ADT7462 devices are used in one system, the $\overline{\text{RESET}}$ pins should not be connected together between devices. Doing so causes one device to reset the other on a power-on reset.

Software Reset

The ADT7462 can be reset in software by setting Bit 7 of Configuration Register 0 (0x00). The code 0x6D must be written to Register 0x7B before setting the software reset bit. This register is cleared to the power-on default after the software reset.

Note that not all registers are restored to their default values on a reset. The same registers are reset by a hardware and software reset. The Register Map section provides a complete reference of registers that are reset.

Chassis Intrusion Input

The chassis intrusion (CI) input is an active high input intended for detection and signaling of unauthorized tampering with the system. When this input goes high, the event is latched in Bit 7 of Host Digital Status Register (0xBE), and an interrupt is generated. The bit remains set until cleared by writing a 1 to CI reset (CI_R), Bit 5 of Configuration Register 3 (0x03). The CI reset bit is cleared by writing a 0 to it.

The CI circuit is powered from the V_{BATT} voltage channel. Pin 26 must be configured to monitor V_{BATT} and a battery must be connected to monitor CI events. CI monitoring is disabled if the measured V_{BATT} value (0x93) is less than the lower voltage limit (0x75) of Pin 26.

The CI input detects chassis intrusion events even when the ADT7462 is powered off (provided battery voltage is applied to V_{BATT}) but does not immediately generate an interrupt. When a chassis intrusion event is detected and latched, an interrupt is generated when the system is powered on.

The actual detection of chassis intrusion is performed by an external circuit that detects, for example, when the cover has been removed. A wide variety of techniques can be used for chassis detection. For example,

- A microswitch that opens or closes when the cover is removed
- A reed switch operated by a magnet affixed to the cover
- A hall-effect switch operated by a magnet affixed to the cover
- A photo-transistor that detects light when the cover is removed

Powerup Sequence

The powerup sequence of the ADT7462 is as follows:

1. The temperature of the thermal diode connected to Pin 17 and Pin 18 (only dedicated thermal diode channel) is monitored immediately on powerup of the ADT7462. Ideally, the hottest zone should be connected to this channel so protection is provided immediately on powerup.
2. V_{CCP1} is also monitored immediately on powerup. V_{CCP1} is typically connected to a main power rail.

Switching on the V_{CCP1} rail gates the fan's quiet startup counter.

3. V_{BATT} is monitored immediately on powerup before the setup complete bit (Register 0x01, Bit 5) is set. The chassis intrusion circuit (CI) is powered from V_{BATT}. If the measured V_{BATT} reading is lower than the lower limit (default = 0x80), the CI circuit is turned off.
4. PWM1, PWM2, and PWM4 are not on dedicated pins. Because these pins are shared with inputs, they are allowed to float high on powerup. This means that if a fan is connected to these pins, it spins at full speed on powerup.
5. PWM3 is switched off by default (because this is a dedicated pin). If no SMBus communication takes place within 4.6 seconds of the V_{CCP} rail switching on, this PWM drive is driven to full speed. If SMBus communication does take place, this pin behaves as programmed.
6. No temperature or voltage (other than V_{CCP1}, Diode 2, and V_{BATT}) is monitored until the setup complete bit (Bit 5) is set in Configuration Register 1 (0x01). This allows the user to program the ADT7462 as required before monitoring of all channels is enabled, thereby not generating false $\overline{\text{ALERT}}$s. The setup complete bit should not be set until the device is fully configured for the desired monitoring functions.

The following steps describe how to set up the ADT7462:

1. Powerup the device.
2. Choose the best-suited easy configuration option for the application, changing pin functions as required.
3. Program all appropriate limits for monitored inputs. Program device parameters, fan control parameters, mask bits, and anything else required for the application.
4. Set the setup complete bit. Do not set this bit until the device is fully set up.

XOR Tree Test

The ADT7462 includes an XOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XOR test, it is possible to detect opens or shorts on the system board. Figure 86 shows the signals exercised in the XOR tree test. The XOR tree test is invoked by setting Bit 6 (XOR) of Configuration Register 3 (0x03).

Note that the digital inputs must be selected on multifunctional pins for the XOR tree test mode. Pin 13 is the open-drain output of the XOR tree test.

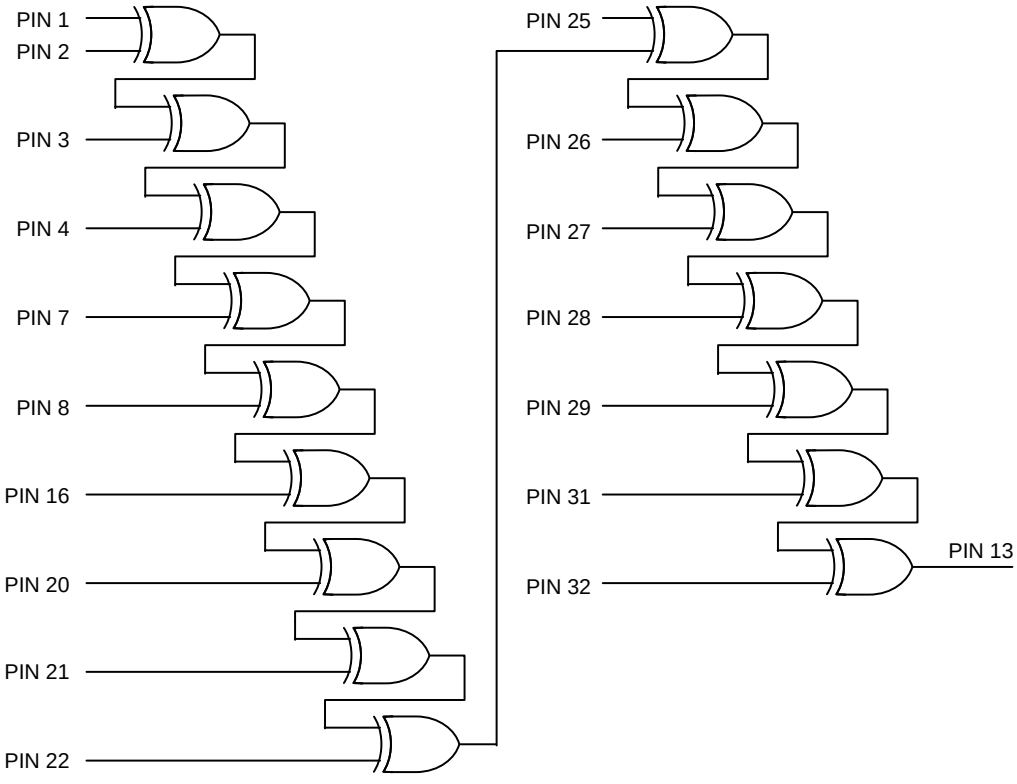


Figure 86. XOR Tree Test

Register Tables

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	SW Reset	Lock able
0x00	Config 0	R/W	SW Reset	VID	# Bytes	# Bytes	#Bytes	# Bytes	# Bytes	# Bytes	0x20	Yes	Yes
0x01	Config 1	R/W	RDY	Lock	SC	DFS	$\overline{\text{ALERT}}$	Res	Res	Mon	0x81	Yes	Yes
0x02	Config 2	R/W	#FP	#FP	FMS	VRD2	VRD1	PWM	Res	FAST	0x80	Yes	Yes
0x03	Config 3	R/W	V_Core_ Low	XOR	CI_R	TT	VID_T	SDA	SCL	GPIO	0x00	Yes	Yes
0x07	TACH Enable	R/W	T8E	T7E	T6E	T5E	T4E	T3E	T2E	T1E	0x00	Yes	Yes
0x08	TACH Config	R/W	Res	Res	Res	Res	DC 4/8	DC 3/7	DC 2/6	DC 1/5	0x0F	Yes	Yes
0x09	GPIO1_ Bhvr	R/W	D4	P4	D3	P3	D2	P2	D1	P1	0x00	Yes	Yes
0x0A	GPIO2_ Bhvr	R/W	D8	P8	D7	P7	D6	P6	D5	P5	0x00	Yes	Yes
0x0B	T_{MIN}_Cal1	R/W	Res	Res	P2R2	P2R1	P1R2	P1R1	R2	R1	0x00	Yes	Yes
0x0C	T_{MIN}_Cal2	R/W	Res	Ctrl Loop Select	CYR2	CYR2	CYR2	CYR1	CYR1	CYR1	0x40	Yes	Yes
0x0D	$\overline{\text{THERM}}$ Conf	R/W	TW2	TW2	TW2	TW1	TW1	TW1	B2	B1	0x00	Yes	Yes
0x0E	Conf_ $\overline{\text{THERM1}}$	R/W	Res	Res	Res	R3	R2	R1	Local	T1TE	0x00	Yes	Yes
0x0F	Conf_ $\overline{\text{THERM2}}$	R/W	Res	Res	Res	R3	R2	R1	Local	T2TE	0x00	Yes	Yes
0x10	Pin Conf 1	R/W	VID	D1	D3	Pin 1	Pin 2	Pin 3	Pin 4	Pin 7	0x7F	Yes	Yes
0x11	Pin Conf 2	R/W	Pin 8	Pin 13	Pin 15	Pin 19	Pin 21	Pin 22	Pin 23	Pin 23	0xCE	Yes	Yes
0x12	Pin Conf 3	R/W	Pin 24	Pin 24	Pin 25	Pin 25	Pin 26	Pin 26	Pin 27	Res	0x42	Yes	Yes
0x13	Pin Conf 4	R/W	Pin 28	Pin 28	Pin 29	Pin 29	Pin 31	Pin 32	Res	Res	0xFC	Yes	Yes
0x14	Easy Conf	R/W	Res	Res	Res	Op5	Op4	Op3	Op2	Op1	0x01	Yes	Yes
0x16	EDO Enable	R/W	CS	CS	CS	CS	CS	SC	EDO2	EDO1	0x00	Yes	Yes
0x18	Attenuators 1 En	R/W	Pin 22	Pin 21	Pin 19	Pin 15	Pin 13	Pin 8	Pin 7	Res	0xFF	Yes	Yes
0x19	Attenuators 2 En	R/W	Res	Res	Pin 29	Pin 28	Res	Pin 25	Pin 24	Pin 23	0x37	Yes	Yes
0x1A	Enhanced Acoustics 1	R/W	RR2	RR2	RR2	RR1	RR1	RR1	En2	En1	0x00	Yes	Yes
0x1B	Enhanced Acoustics 2	R/W	RR4	RR4	RR4	RR3	RR3	RR3	En4	En3	0x00	Yes	Yes
0x1C	Fan Free-wheel Test	R/W	Fan 8	Fan 7	Fan 6	Fan 5	Fan 4	Fan 3	Fan 2	Fan 1	0x00	Yes	Yes
0x1D	Fans Present	R/W	F8P	F7P	F6P	F5P	F4P	F3P	F2P	F1P	0x00	Yes	Yes
0x1E	Fan Free-wheel TestEn	R/W	Fan 8	Fan 7	Fan 6	Fan 5	Fan 4	Fan 3	Fan 2	Fan 1	0x00	Yes	Yes
0x21	PWM1 Config	R/W	BHVR	BHVR	BHVR	INV	SLOW	Spin	Spin	Spin	0x11	Yes	Yes
0x22	PWM2 Config	R/W	BHVR	BHVR	BHVR	INV	SLOW	Spin	Spin	Spin	0x31	Yes	Yes
0x23	PWM3 Config	R/W	BHVR	BHVR	BHVR	INV	SLOW	Spin	Spin	Spin	0x51	Yes	Yes
0x24	PWM4 Config	R/W	BHVR	BHVR	BHVR	INV	SLOW	Spin	Spin	Spin	0x71	Yes	Yes
0x25	PWM1, PWM2 Freq	R/W	F2	F2	F2	F1	F1	F1	Min 2	Min 1	0x90	Yes	Yes
0x26	PWM3, PWM4 Freq	R/W	F4	F4	F4	F3	F3	F3	Min 4	Min 3	0x90	Yes	Yes

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	SW Reset	Lock able
0x28	PWM1 Min	R/W	7	6	5	4	3	2	1	0	0x80	Yes	Yes
0x29	PWM2 Min	R/W	7	6	5	4	3	2	1	0	0x80	Yes	Yes
0x2A	PWM3 Min	R/W	7	6	5	4	3	2	1	0	0x80	Yes	Yes
0x2B	PWM4 Min	R/W	7	6	5	4	3	2	1	0	0x80	Yes	Yes
0x2C	PWM1 to PWM4 Max	R/W	7	6	5	4	3	2	1	0	0xC0	Yes	Yes
0x30	Thermal Mask 1	R/W	R3D	R2D	R1D	R3	R2	R1	Local	Res	0x00	Yes	No
0x31	Thermal Mask 2	R/W	VRD2	VRD1	T2S	T2A	T2%	T1S	T1A	T1%	0xC0	Yes	No
0x32	Voltage Mask 1	R/W	P23	+5V	P19	P15	+3.3V	+12V3	+12V2	+12V1	0x00	Yes	No
0x33	Voltage Mask 2	R/W	+1.5V1 (ICH)	+1.5V2 (3GIO)	P26	P25	P24	Res	Res	Res	0x00	Yes	No
0x34	Fan Mask	R/W	Fan 8	Fan 7	Fan 6	Fan 5	Fan 4	Fan 3	Fan 2	Fan 1	0x00	Yes	No
0x35	Digital Mask	R/W	CI	VID	SCSI2	SCSI1	$\overline{\text{FAN2MAX}}$	Res	Res	Res	0x38	Yes	No
0x36	GPIO Mask	R/W	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	0x00	Yes	No
0x37	EDO Mask 1	R/W	Volt	Temp	Fan	Res	GPIO4	GPIO3	GPIO2	GPIO1	0x00	Yes	No
0x38	EDO Mask 2	R/W	Volt	Temp	Fan	Res	GPIO4	GPIO3	GPIO2	GPIO1	0x00	Yes	No
0x3D	Device ID	R	7	6	5	4	3	2	1	0	0x62	No	N/A
0x3E	Comp ID	R	7	6	5	4	3	2	1	0	0x41	No	N/A
0x3F	Rev No	R	7	6	5	4	3	2	1	0	0x04	No	N/A
0x44	Local Low Temp Limit	R/W	7	6	5	4	3	2	1	0	0x40	No	No
0x45	Remote 1/Pin 15 Low Temp Limit	R/W	7	6	5	4	3	2	1	0	0x40	No	No
0x46	Remote 2 Low Temp Limit	R/W	7	6	5	4	3	2	1	0	0x40	No	No
0x47	Remote 3/Pin 19 Low Temp Limit	R/W	7	6	5	4	3	2	1	0	0x40	No	No
0x48	Local High Limit	R/W	7	6	5	4	3	2	1	0	0x95	No	No
0x49	Remote 1/Pin 15 High Limit	R/W	7	6	5	4	3	2	1	0	0x95	No	No
0x4A	Remote 2 High Limit	R/W	7	6	5	4	3	2	1	0	0x95	No	No
0x4B	Remote 3/Pin 19 High Limit	R/W	7	6	5	4	3	2	1	0	0x95	No	No
0x4C	Local $\overline{\text{THERM1}}$/ +1.5V2 (3GIO) High	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x4D	Remote 1 $\overline{\text{THERM1}}$ Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x4E	Remote 2 $\overline{\text{THERM1}}$ Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x4F	Remote 3 $\overline{\text{THERM1}}$ Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	SW Reset	Lock able
0x50	Local $\overline{\text{THERM2}}$/ +1.5V1 (ICH) High	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x51	Remote 1 $\overline{\text{THERM2}}$ Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x52	Remote 2 $\overline{\text{THERM2}}$ Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x53	Remote 3 $\overline{\text{THERM2}}$ Limit	R/W	7	6	5	4	3	2	1	0	0xA4	No	Yes
0x54	Local/Re-mote1 Temp Hyst	R/W	LH	LH	LH	LH	R1H	R1H	R1H	R1H	0x44	No	Yes
0x55	Remote 2/ Remote 3 Temp Hyst	R/W	R2H	R2H	R2H	R2H	R3H	R3H	R3H	R3H	0x44	No	Yes
0x56	Local Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x57	Remote 1 Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x58	Remote 2 Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x59	Remote 3 Offset	R/W	7	6	5	4	3	2	1	0	0x00	No	Yes
0x5A	Remote 1 Operating Point	R/W	7	6	5	4	3	2	1	0	0xA4	Yes	Yes
0x5B	Remote 2 Operating Point	R/W	7	6	5	4	3	2	1	0	0xA4	Yes	Yes
0x5C	Local Temp T_{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x5D	Remote 1 Temp T_{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x5E	Remote 2 Temp T_{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x5F	Remote 3 Temp T_{MIN}	R/W	7	6	5	4	3	2	1	0	0x9A	Yes	Yes
0x60	Local T_{RANGE}/ Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x61	Remote 1 T_{RANGE}/ Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x62	Remote 2 T_{RANGE}/ Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x63	Remote 3 T_{RANGE}/ Hyst	R/W	Range	Range	Range	Range	Hys	Hys	Hys	Hys	0xC4	Yes	Yes
0x64	Operating Point Hyst	R/W	Hys	Hys	Hys	Hys	Res	Res	Res	Res	0x40	Yes	Yes
0x68	+3.3V High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	No
0x69	Pin 23 Voltage High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	No
0x6A	Pin 24 Voltage High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	No
0x6B	Pin 25 Voltage High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	No

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	SW Reset	Lock able
0x6C	Pin 26 Voltage High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	No
0x6D	+12V1 Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x6E	+12V2 Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x6F	+12V3 Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x70	+3.3V Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x71	+5V Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x72	Pin 23 Voltage Low Limit	R/W	7	6	5	4	3	2	1	0	0x20	No	No
0x73	Pin 24 Voltage Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x74	Pin 25 Voltage Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x75	Pin 26 Voltage Low Limit	R/W	7	6	5	4	3	2	1	0	0x80	No	No
0x76	+1.5V2 (3GIO) Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x77	+1.5V1 (ICH) Low Limit	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0x78	TACH1 Limit/VID	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x79	TACH2 Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x7A	TACH3 Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x7B	TACH4 Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x7C	TACH5/+12 V1 High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x7D	TACH6/+12 V2 High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x7E	TACH7/+5V High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x7F	TACH8/+12 V3 High Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x80	$\overline{\text{THERM1}}$ Timer Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x81	$\overline{\text{THERM2}}$ Timer Limit	R/W	7	6	5	4	3	2	1	0	0xFF	No	Yes
0x88	Local Temp Value, LSBs	R	7	6	5	4	3	2	1	0	0x00	No	No
0x89	Local Temp Value, MSBs	R	7	6	5	4	3	2	1	0	0x00	No	No
0x8A	Remote 1 Temp, LSBs	R	7	6	5	4	3	2	1	0	0x00	No	No

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	SW Reset	Lock able
0x8B	Remote 1 Temp, MSBs, Pin 15 Volt	R	7	6	5	4	3	2	1	0	0x00	No	No
0x8C	Remote 2 Temp, LSBs	R	7	6	5	4	3	2	1	0	0x00	No	No
0x8D	Remote 2 Temp, MSBs	R	7	6	5	4	3	2	1	0	0x00	No	No
0x8E	Remote 3 Temp, LSBs	R	7	6	5	4	3	2	1	0	0x00	No	No
0x8F	Remote 3 Temp, MSBs, Pin 19 Volt	R	7	6	5	4	3	2	1	0	0x00	No	No
0x90	Pin 23 Voltage	R	7	6	5	4	3	2	1	0	0x00	No	No
0x91	Pin 24 Voltage	R	7	6	5	4	3	2	1	0	0x00	No	No
0x92	Pin 25 Voltage	R	7	6	5	4	3	2	1	0	0x00	No	No
0x93	Pin 26 Voltage	R	7	6	5	4	3	2	1	0	0x00	No	No
0x94	+1.5V1 (ICH) Volt	R	7	6	5	4	3	2	1	0	0x00	No	No
0x95	+1.5V2 (3GIO) Voltage	R	7	6	5	4	3	2	1	0	0x00	No	No
0x96	+3.3V Voltage	R	7	6	5	4	3	2	1	0	0x00	No	No
0x97	VID Value	R	7	6	5	4	3	2	1	0	0x00	No	No
0x98	TACH1 Value, LSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0x99	TACH1 Value, MSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0x9A	TACH2 Value, LSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0x9B	TACH2 Value, MSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0x9C	TACH3 Value, LSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0x9D	TACH3 Value, MSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0x9E	TACH4 Value, LSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0x9F	TACH4 Value, MSBs	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA0	Unused	R	7	6	5	4	3	2	1	0	N/A	No	No
0xA1	Unused	R	7	6	5	4	3	2	1	0	N/A	No	No
0xA2	TACH5 Value, LSB	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA3	TACH5 MSB/ +12V1V	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA4	TACH6 Value, LSB	R	7	6	5	4	3	2	1	0	0xFF	No	No

Table 34. REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	SW Reset	Lock able
0xA5	TACH6 MSB/+12V 2 Voltage	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA6	TACH7 Value, LSB	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA7	TACH7 MSB/+5V Voltage	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA8	TACH8 Value, LSB	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xA9	TACH8 MSB/+12V 3 Voltage	R	7	6	5	4	3	2	1	0	0xFF	No	No
0xAA	PWM1 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0xAB	PWM2 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0xAC	PWM3 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0xC0	No	No
0xAD	PWM4 Duty Cycle	R/W	7	6	5	4	3	2	1	0	0x00	No	No
0xAE	$\overline{\text{THERM1}}$ %On−Time	R	7	6	5	4	3	2	1	0	0x00	No	No
0xAF	$\overline{\text{THERM2}}$ %On−Time	R	7	6	5	4	3	2	1	0	0x00	No	No
0xB8	Thermal Status 1, Host	R	R3D	R2D	R1D	R3	R2	R1	Local	Res	0x00	Yes	No
0xB9	Thermal Status 2, Host	R	VR2	VR1	T2S	T2A	T2%	T1S	T1A	T1%	0x00	Yes	No
0xBA	Thermal Status 3, Host	R	R3T2	R2T2	R1T2	LT2	R3T1	R2T1	R1T1	LT1	0x00	Yes	No
0xBB	Voltage Status 1, Host	R	Pin 23	+5V	Pin 19	Pin 15	+3.3V	+12V3	+12V2	+12V1	0x00	Yes	No
0xBC	Voltage Status 2, Host	R	+1.5V1 (ICH)	+1.5V2 (3GIO)	Pin 26	Pin 25	Pin 24	Res	Res	Res	0x00	Yes	No
0xBD	Fan Status, Host	R	Fan 8	Fan 7	Fan 6	Fan 5	Fan 4	Fan 3	Fan 2	Fan 1	0x00	Yes	No
0xBE	Digital Status, Host	R	CI	VID	SCSI2	SCSI1	$\overline{\text{FAN2MAX}}$	Res	Res	Res	0x00	Yes	No
0xBF	GPIO Status, Host	R/W	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	0x00	Yes	No
0xC0	Thermal Status 1, BMC	R	R3D	R2D	R1D	R3	R2	R1	Local	Res	0x00	Yes	No
0xC1	Thermal Status 2, BMC	R	VR2	VR1	T2S	T2A	T2%	T1S	T1A	T1%	0x00	Yes	No
0xC3	Voltage Status 1, BMC	R	Pin 23	+5V	Pin 19	Pin 15	+3.3V	+12V3	+12V2	+12V1	0x00	Yes	No
0xC4	Voltage Status 2, BMC	R	+1.5V1 (ICH)	+1.5V2 (3GIO)	Pin 26	Pin 25	Pin 24	Res	Res	Res	0x00	Yes	No
0xC5	Fan Status, BMC	R	Fan 8	Fan 7	Fan 6	Fan 5	Fan 4	Fan 3	Fan 2	Fan 1	0x00	Yes	No
0xC6	Digital Status, BMC	R	CI	VID	SCSI2	SCSI1	$\overline{\text{FAN2MAX}}$	Res	Res	Res	0x00	Yes	No

Table 35. REGISTER 0X00 − CONFIGURATION REGISTER 0 (Note 1)

Bit	Name	R/W	Description
[5:0]	#Bytes Block Read	R/W	These bits set the number of registers to be read in a block read. Default = 0x20.
6	VID Decoder	R/W	0 = VR10 Decoding Spec; 1 = VR11 Decoding Spec. Default = 0.
7	SW Reset	R/W	Setting this bit to 1 restores all unlocked registers to their default values. Self-clearing. Write 0x6D to register 0x7B before setting this bit to get a software reset. Default = 0.

1. POR = 0x20, Lock = Y, SW Reset = Y.

Table 36. REGISTER 0X01 − CONFIGURATION REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	Monitor	R/W	Setting this bit to 1 enables temperature and voltage measurements. When this bit is set to 0, temperature and voltage measurements are disabled. Default = 1.
1	Reserved	R/W	Reserved. Default = 0.
2	Reserved	R/W	Reserved. Default = 0.
3	$\overline{\text{ALERT}}$ Mode	R/W	This bit sets the $\overline{\text{ALERT}}$ mode in the ADT7462. 1 = comparator mode, 0 = $\overline{\text{SMBALERT}}$ mode (Default).
4	Disable Fast Spin-Up	R/W	Setting this bit to 1 disables the fast spin-up (for two TACH pulses) for the fans. Instead, the fans spin up for the programmed fan startup timeout. Default = 0.
5	Setup Complete	R/W	Setting this bit to 1 tells the ADT7462 that setup is complete and that monitoring of all selected channels should begin. Default = 0.
6	Lock	Write Once	Logic 1 locks all limit values at their current settings. When this bit is set, all lockable registers become read-only and cannot be modified until the ADT7462 is powered down and powered up again. This prevents rogue programs, such as viruses, from modifying critical system limit settings. Lockable.
7	RDY	R	This bit is set to 1 to indicate that the ADT7462 is fully powered up and ready to start monitoring.

1. POR = 0x81, Lock = Y, SW Reset = Y.

Table 37. REGISTER 0X02 − CONFIGURATION REGISTER 2 (Note 1)

Bit	Name	R/W	Description
0	FAST	R/W	In low frequency, PWM fan speed measurements are made once a second. Setting this bit to 1 increases the frequency of the fan speed measurements to 4 times a second. Default = 0.
1	Reserved	R/W	Reserved. Default = 0.
2	PWM Mode	R/W	This bit sets the PWM frequency mode. 0 = low frequency PWM; frequency programmable between 11 Hz and 88.2 Hz. Default = 35.3 Hz. 1 = high frequency mode, 22.5 kHz.
3	VRD1 Boost	R/W	Setting this bit to 0 causes the fans to go to full speed on assertion of VRD1. Default = 0. When this bit is set to 1, VRD1 assertions have no effect on the fan speed.
4	VRD2 Boost	R/W	Setting this bit to 0 causes the fans to go to full speed on assertion of VRD2. Default = 0. When this bit is set to 1, VRD2 assertions have no effect on the fan speed.
5	Fans Full Speed	R/W	Setting this bit to 1 drives the fans to full speed. Default = 0.
[7:6]	#TACH Pulses	R/W	In low frequency mode, the ADT7462 must pulse stretch to get an accurate fan speed measurement. The speed is always measured between the 2nd rising edge and one × TACH pulses later. This bit determines the last TACH pulse. Therefore, if the fan speed is to be measured between the second and fourth TACH pulse, 01 is written to these bits. x = 1 = 00 x = 2 = 01 x = 3 = 10 (Default) x = 4 = 11

1. POR = 0x80, Lock = Y, SW Reset = Y.

Table 38. REGISTER 0X03 − CONFIGURATION REGISTER 3 (Note 1)

Bit	Name	R/W	Description
0	GPIO_En	R/W	Setting this bit to 1 enables the GPIOs. Default = 0.
1	SCL_Timeout	R/W	1 = SCL timeout enabled. 0 = SCL timeout disabled = default.
2	SDA_Timeout	R/W	1 = SDA timeout enabled. 0 = SDA timeout disabled = default.
3	VID_Threshold	R/W	This bit sets the digital threshold for the VID digital inputs. 0 = default. 1 = low thresholds selected = 0.65 V.
4	$\overline{\text{THERM}}$_ Threshold	R/W	This bit sets the digital threshold for the $\overline{\text{THERM}}$ digital inputs. 0 = default. 1 = low thresholds selected = 2/3 V_{CCP1} (Pin 23).
5	CI Reset	R/W	Setting this bit to 1 resets the chassis intrusion circuit. This bit clears itself. Default = 0.
6	XOR Tree	R/W	Setting this bit to 1 enables the XOR tree test. Default = 0.
7	V_Core_Low	R/W	Setting this bit to 1 enables V_core_low. Default = 0.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 39. REGISTER 0X07 − TACH ENABLE REGISTER (Note 1)

Bit	Name	R/W	Description
0	TACH1	R/W	Setting this bit to 1 enables the TACH1 measurement. Default = 0.
1	TACH2	R/W	Setting this bit to 1 enables the TACH2 measurement. Default = 0.
2	TACH3	R/W	Setting this bit to 1 enables the TACH3 measurement. Default = 0.
3	TACH4	R/W	Setting this bit to 1 enables the TACH4 measurement. Default = 0.
4	TACH5	R/W	Setting this bit to 1 enables the TACH5 measurement. Default = 0.
5	TACH6	R/W	Setting this bit to 1 enables the TACH6 measurement. Default = 0.
6	TACH7	R/W	Setting this bit to 1 enables the TACH7 measurement. Default = 0.
7	TACH8	R/W	Setting this bit to 1 enables the TACH8 measurement. Default = 0.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 40. REGISTER 0X08 − TACH CONFIGURATION REGISTER (Note 1)

Bit	Name	R/W	Description
0	DC 1/5	R/W	Setting this bit to 1 enables continuous measurements on TACH1 and TACH5 in low frequency PWM mode. Continuous measurement means that pulse stretching is turned off and the PWM output and TACH inputs are no longer synchronized. Default = 1.
1	DC 2/6	R/W	Setting this bit to 1 enables continuous measurements on TACH2 and TACH6 in low frequency PWM mode. Continuous measurement means that pulse stretching is turned off and the PWM output and TACH inputs are no longer synchronized. Default = 1.
2	DC 3/7	R/W	Setting this bit to 1 enables continuous measurements on TACH3 and TACH7 in low frequency PWM mode. Continuous measurement means that pulse stretching is turned off and the PWM output and TACH inputs are no longer synchronized. Default = 1.
3	DC 4/8	R/W	Setting this bit to 1 enables continuous measurements on TACH4 and TACH8 in low frequency PWM mode. Continuous measurement means that pulse stretching is turned off and the PWM output and TACH inputs are no longer synchronized. Default = 1.
[7:4]	Reserved	R	Reserved for future use.

1. POR = 0x0F, Lock = Y, SW Reset = Y.

Table 41. REGISTER 0X09 − GPIO CONFIGURATION REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	GPIO1_P	R/W	This bit sets the polarity of GPIO1. 0 = Default = Active Low. 1= Active High.
1	GPIO1_D	R/W	This bit sets the direction of GPIO1. 0 = Default = Input. 1= Output.
2	GPIO2_P	R/W	This bit sets the polarity of GPIO2. 0 = Default = Active low. 1= Active High.
3	GPIO2_D	R/W	This bit sets the direction of GPIO2. 0 = Default = Input. 1= Output.
4	GPIO3_P	R/W	This bit sets the polarity of GPIO3. 0 = Default = Active Low. 1= Active High.
5	GPIO3_D	R/W	This bit sets the direction of GPIO3. 0 = Default = Input. 1= Output.
6	GPIO4_P	R/W	This bit sets the polarity of GPIO4. 0 = Default = Active Low. 1= Active High.
7	GPIO4_D	R/W	This bit sets the direction of GPIO4. 0 = Default = Input. 1= Output.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 42. REGISTER 0X0A − GPIO CONFIGURATION REGISTER 2 (Note 1)

Bit	Name	R/W	Description
0	GPIO5_P	R/W	This bit sets the polarity of GPIO5. 0 = Default = Active Low. 1= Active High.
1	GPIO5_D	R/W	This bit sets the direction of GPIO5. 0 = Default = Input. 1= Output.
2	GPIO6_P	R/W	This bit sets the polarity of GPIO6. 0 = Default = Active Low. 1= Active High.
3	GPIO6_D	R/W	This bit sets the direction of GPIO6. 0 = Default = Input. 1= Output.
4	GPIO7_P	R/W	This bit sets the polarity of GPIO7. 0 = Default = Active Low. 1= Active High.
5	GPIO7_D	R/W	This bit sets the direction of GPIO7. 0 = Default = Input. 1= Output.
6	GPIO8_P	R/W	This bit sets the polarity of GPIO8. 0 = Default = Active Low. 1= Active High.
7	GPIO8_D	R/W	This bit sets the direction of GPIO8. 0 = Default = Input. 1= Output.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 43. REGISTER 0X0B − DYNAMIC T_{MIN} CONTROL REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	Remote 1 En	R/W	Setting this bit to 1 enables dynamic T_{MIN} control for the Remote 1 channel. Default = 0.
1	Remote 2 En	R/W	Setting this bit to 1 enables dynamic T_{MIN} control for the Remote 2 channel. Default = 0.
2	P1R1	R/W	P1R1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register if $\overline{\text{THERM1}}$ is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which $\overline{\text{THERM1}}$ is asserted. P1R1 = 0 (Default) ignores any $\overline{\text{THERM1}}$ assertions on the $\overline{\text{THERM1}}$ pin. The Remote 1 operating point register reflects its programmed value.
3	P1R2	R/W	P1R2 = 1 copies the Remote 2 current temperature to the Remote 2 operating point register if $\overline{\text{THERM1}}$ is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which $\overline{\text{THERM1}}$ is asserted. P1R2 = 0 (Default) ignores any $\overline{\text{THERM1}}$ assertions on the $\overline{\text{THERM1}}$ pin. The Remote 2 operating point register reflects its programmed value.
4	P2R1	R/W	P2R1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register if $\overline{\text{THERM2}}$ is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which $\overline{\text{THERM2}}$ is asserted. P2R1 = 0 (Default) ignores any $\overline{\text{THERM2}}$ assertions on the $\overline{\text{THERM2}}$ pin. The Remote 1 operating point register reflects its programmed value.
5	P2R2	R/W	P2R2 = 1 copies the Remote 2 current temperature to the Remote 2 operating point register if $\overline{\text{THERM2}}$ is asserted externally. This happens only if the current temperature is less than the value in the operating point register. The operating point contains the temperature at which $\overline{\text{THERM2}}$ is asserted. P2R2 = 0 (Default) ignores any $\overline{\text{THERM2}}$ assertions on the $\overline{\text{THERM2}}$ pin. The Remote 2 operating point register reflects its programmed value.
[7:6]	Reserved	R/W	Reserved for future use.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 44. REGISTER 0X0C − DYNAMIC T_{MIN} CONTROL REGISTER 2 (Note 1)

Bit	Name	R/W	Description		
[2:0]	CYR1	R/W	Three-bit Remote 1 cycle value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 1 temperature channel, in terms of number of monitoring cycles. The system has associated thermal time constants that must be found to optimize the response of fans and the control loop.		
			Bits	**Decrease cycle**	**Increase cycle**
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
[5:3]	CYR2	R/W	Three-bit Remote 2 cycle value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 2 temperature channel, in terms of number of monitoring cycles. The system has associated thermal time constants that must be found to optimize the response of fans and the control loop.		
			Bits	**Decrease cycle**	**Increase Cycle**
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
6	Control Loop Select	R/W	This bit allows the user to select between two control loops. 0 makes the control loop backwards compatible with the ADT7463 and ADT7468. 1 = ADT7462 control loop (Default).		
7	Reserved	R	Reserved for future use.		

1. POR = 0x40, Lock = Y, SW Reset = Y.

Table 45. REGISTER 0X0D − $\overline{\text{THERM}}$ CONFIGURATION REGISTER (Note 1)

Bit	Name	R/W	Description
0	Boost 1	R/W	Setting this bit to 0 causes the fans to go to maximum PWM on assertion of $\overline{\text{THERM1}}$ as an output. Setting this bit to 1 means that the fan speed is not affected when the $\overline{\text{THERM1}}$ temperature limit is exceeded. Default = 0.
1	Boost 2	R/W	Setting this bit to 0 causes the fans to go to maximum PWM on assertion of $\overline{\text{THERM2}}$ as an output. Setting this bit to 1 means that the fan speed is not affected when the $\overline{\text{THERM2}}$ temperature limit is exceeded. Default = 0.
[4:2]	$\overline{\text{THERM1}}$ Timer Window	R/W	These bits set the timer window for measuring $\overline{\text{THERM1}}$ assertions. 000 = 0.25 sec 001 = 0.5 sec 010 = 1 sec 011 = 2 sec 100 = 4 sec 101 = 8 sec 110 = 8 sec 111 = 8 sec
[7:5]	$\overline{\text{THERM2}}$ Timer Window	R/W	These bits set the timer window for measuring $\overline{\text{THERM2}}$ assertions. 000 = 0.25 sec 001 = 0.5 sec 010 = 1 sec 011 = 2 sec 100 = 4 sec 101 = 8 sec 110 = 8 sec 111 = 8 sec

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 46. REGISTER 0X0E − $\overline{\text{THERM1}}$ CONFIGURATION REGISTER (Note 1)

Bit	Name	R/W	Description
0	$\overline{\text{THERM1}}$ Timer Enable	R/W	Enables the $\overline{\text{THERM1}}$ timer circuit. Default = 0.
1	$\overline{\text{THERM1}}$_Local	R/W	Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the local temperature exceeds the local $\overline{\text{THERM1}}$ temperature limit. Default = 0.
2	$\overline{\text{THERM1}}$_ Remote 1	R/W	Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the Remote 1 temperature exceeds the Remote 1 $\overline{\text{THERM1}}$ temperature limit. Default = 0.
3	$\overline{\text{THERM1}}$_ Remote 2	R/W	Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the Remote 2 temperature exceeds the Remote 2 $\overline{\text{THERM1}}$ temperature limit. Default = 0.
4	$\overline{\text{THERM1}}$_ Remote 3	R/W	Setting the bit to 1 means that the $\overline{\text{THERM1}}$ pin is asserted low as an output whenever the Remote 3 temperature exceeds the Remote 3 $\overline{\text{THERM1}}$ temperature limit. Default = 0.
[7:5]	Reserved	R	Reserved for future use.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 47. REGISTER 0X0F − $\overline{\text{THERM2}}$ CONFIGURATION REGISTER (Note 1)

Bit	Name	R/W	Description
0	$\overline{\text{THERM2}}$ Timer Enable	R/W	Enables the $\overline{\text{THERM2}}$ timer circuit. Default = 0.
1	$\overline{\text{THERM2}}$_Local	R/W	Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the local temperature exceeds the local $\overline{\text{THERM2}}$ temperature limit. Default = 0.
2	$\overline{\text{THERM2}}$_ Remote 1	R/W	Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the Remote 1 temperature exceeds the Remote 1 $\overline{\text{THERM2}}$ temperature limit. Default = 0.
3	$\overline{\text{THERM2}}$_ Remote 2	R/W	Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the Remote 2 temperature exceeds the Remote 2 $\overline{\text{THERM2}}$ temperature limit. Default = 0.
4	$\overline{\text{THERM2}}$_ Remote 3	R/W	Setting the bit to 1 means that the $\overline{\text{THERM2}}$ pin is asserted low as an output whenever the Remote 3 temperature exceeds the Remote 3 $\overline{\text{THERM2}}$ temperature limit. Default = 0.
[7:5]	Reserved	R	Reserved for future use.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 48. REGISTER 0X10 − PIN CONFIGURATION REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	Pin 7	R/W	0 = +12V1; 1 = TACH5 Input. Default = 1.
1	Pin 4	R/W	0 = GPIO4; 1= TACH4 Input (that is, if the VIDs are not selected). Default = 1.
2	Pin 3	R/W	0 = GPIO3; 1= TACH3 Input (that is, if the VIDs are not selected). Default = 1.
3	Pin 2	R/W	0 = GPIO2; 1= TACH2 Input (that is, if the VIDs are not selected). Default = 1.
4	Pin 1	R/W	0 = GPIO1; 1= TACH1 Input (that is, if the VIDs are not selected). Default = 1.
5	Diode 3	R/W	1 enables the D3+ and D3− inputs on Pin 19 and Pin 20. 0 enables the voltage measurement input and SCSI_TERM2 input. Default = 1.
6	Diode 1	R/W	1 enables the D1+ and D1− inputs on Pin 15 and Pin 16. 0 enables the voltage measurement input and SCSI_TERM1 input. Default = 1.
7	VIDs	R/W	Setting this bit to 1 enables the VIDs on Pin 1 to Pin 4, Pin 28, Pin 31, and Pin 32. Default = 0.

1. POR = 0x7F, Lock = Y, SW Reset = Y.

Table 49. REGISTER 0X11 − PIN CONFIGURATION REGISTER 2 (Note 1)

Bit	Name	R/W	Description
[1:0]	Pin 23	R/W	00 = V_{CCP1} Selected. 01 = +2.5V. 10 = +1.8V (Default). 11 = +1.5V.
2	Pin 22	R/W	0 = +12V3; 1 = TACH8. Default = 1.
3	Pin 21	R/W	0 = +5V; 1 = TACH7. Default = 1.
4	Pin 19	R/W	0 = +1.25V; 1 = +0.9V (that is, if RT3 Is Not Selected). Default = 0.
5	Pin 15	R/W	0 = +2.5V, 1 = +1.8V (that is, if RT1 Is Not Selected). Default = 0.
6	Pin 13	R/W	0 = +3.3V; 1 = PWM4. Default = 1.
7	Pin 8	R/W	0 = +12V2; 1 = TACH6. Default = 1.

1. POR = 0xCE, Lock = Y, SW Reset = Y.

Table 50. REGISTER 0X12 − PIN CONFIGURATION REGISTER 3 (Note 1)

Bit	Name	R/W	Description
0	Reserved	R	Reserved for future use.
1	Pin 27	R/W	0 = $\overline{\text{FAN2MAX}}$; 1 = Chassis Intrusion (Default).
[3:2]	Pin 26	R/W	00 = V_{BATT} Selected (Default). 01 = +1.2V2 (FSB_V_{TT}). 10 = VR_HOT2. 11 = VR_HOT2.
[5:4]	Pin 25	R/W	00 = +3.3V Selected (Default). 01 = +1.2V1 (G_{BIT}). 10 = VR_HOT1. 11 = VR_HOT1.
[7:6]	Pin 24	R/W	00 = V_{CCP2} Selected. 01 = +2.5V (Default). 10 = +1.8V. 11 = +1.5V.

1. POR = 0x42, Lock = Y, SW Reset = Y.

Table 51. REGISTER 0X13 − PIN CONFIGURATION REGISTER 4 (Note 1)

Bit	Name	R/W	Description
[1:0]	Reserved	R	Reserved.
2	Pin 32	R/W	0 = GPIO6; 1 = PWM2 (Pin 32 Is VID5 if VIDs Are Selected). Default = 1.
3	Pin 31	R/W	0 = GPIO5; 1 = PWM1 (Pin 31 Is VID4 if VIDs Are Selected). Default = 1.
[5:4]	Pin 29 (Pin 28, +1.5V Monitoring) (Note 2)	R/W	00 = GPIO8. 01 = +1.5V (Measured on Pin 28). 10 = $\overline{\text{THERM2}}$. 11 = $\overline{\text{THERM2}}$ (Default).(Pin 28 Is VID6 if VIDs Are Selected.)
[7:6]	Pin 28 (Pin 29, +1.5V Monitoring) (Note 3)	R/W	00 = GPIO7. 01 = +1.5V (Measured on Pin 29). 10 = $\overline{\text{THERM1}}$. 11 = $\overline{\text{THERM1}}$ (Default).

1. POR = 0xFC, Lock = Y, SW Reset = Y.
2. +1.5V can be monitored on Pin 28 and 29 only when both are configured as +1.5V inputs. This means that +1.5V is measured on both pins or on neither. +1.5V monitoring cannot be combined with another function on the other pin. For example, if Pin 29 is configured as +1.5V, then $\overline{\text{THERM1}}$ cannot be selected on Pin 28, because they share the same selection bits.

Table 52. REGISTER 0X14 − EASY CONFIGURATION OPTIONS (Note 1)

Bit	Name	R/W	Description
0	Easy Option 1 Select	R/W	Setting this bit to 1 enables Easy Option 1.
1	Easy Option 2 Select	R/W	Setting this bit to 1 enables Easy Option 2.
2	Easy Option 3 Select	R/W	Setting this bit to 1 enables Easy Option 3.
3	Easy Option 4 Select	R/W	Setting this bit to 1 enables Easy Option 4.
4	Easy Option 5 Select	R/W	Setting this bit to 1 enables Easy Option 5.
[7:5]	Reserved	R	Reserved for future use.

1. POR = 0x01, Lock = Y, SW Reset = Y.

Table 53. REGISTER 0X16 − EDO/SINGLE CHANNEL ENABLE (Note 1)

Bit	Name	R/W	Description
0	EDO_En1	R/W	Enable EDO on GPIO5. Default = 0.
1	EDO_En2	R/W	Enable EDO on GPIO6. Default = 0.
2	Single−Channel Mode Select	R/W	Setting this bit to 1 places the ADT7462 in single-channel mode. This means that it converts on one channel only. The channel it converts on is set using the channel select bits in this register. Default = 0.
[7:3]	Channel Select	R/W	These bits are used to set the single channel that the ADT7462 measures in single-channel mode. 0000 0 = Pin 26 (Default) 0001 0 = Remote 2 Temperature 0010 0 = Local Temperature 0011 0 = +12V2 0100 0 = +3.3V 0101 0 = Pin 19 Voltage 0110 0 = Pin 23 Voltage 0111 0 = Pin 25 Voltage 1000 1 = +1.5V2 (3GIO) Voltage 0000 1 = Remote 1 Temperature 0001 1 = Remote 3 Temperature 0010 1 = +12V1 0011 1 = +12V3 0100 1 = Pin 15 Voltage 0101 1 = +5V 0110 1 = Pin 24 Voltage 1000 0 = +1.5V1 (ICH) Voltage

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 54. REGISTER 0X18 − VOLTAGE ATTENUATOR CONFIGURATION 1 (Note 1)

Bit	Name	R/W	Description
0	Reserved	R	Reserved for future use.
1	Attenuator Pin 7	R/W	Setting this bit to 0 removes the attenuators for Pin 7. Default = 1 = Attenuators Enabled.
2	Attenuator Pin 8	R/W	Setting this bit to 0 removes the attenuators for Pin 8. Default = 1 = Attenuators Enabled.
3	Attenuator Pin 13	R/W	Setting this bit to 0 removes the attenuators for Pin 13. Default = 1 = Attenuators Enabled.
4	Attenuator Pin 15	R/W	Setting this bit to 0 removes the attenuators for Pin 15. Default = 1 = Attenuators Enabled.
5	Attenuator Pin 19	R/W	Setting this bit to 0 removes the attenuators for Pin 19. Default = 1 = Attenuators Enabled.
6	Attenuator Pin 21	R/W	Setting this bit to 0 removes the attenuators for Pin 21. Default = 1 = Attenuators Enabled.
7	Attenuator Pin 22	R/W	Setting this bit to 0 removes the attenuators for Pin 22. Default = 1 = Attenuators Enabled.

1. POR = 0xFF, Lock = Y, SW Reset = Y.

Table 55. REGISTER 0X19 − VOLTAGE ATTENUATOR CONFIGURATION 2 (Note 1)

Bit	Name	R/W	Description
0	Attenuator Pin 23	R/W	Setting this bit to 0 removes the attenuators for Pin 23. Default = 1 = Attenuators Enabled.
1	Attenuator Pin 24	R/W	Setting this bit to 0 removes the attenuators for Pin 24. Default = 1 = Attenuators Enabled.
2	Attenuator Pin 25	R/W	Setting this bit to 0 removes the attenuators for Pin 25. Default = 1 = Attenuators Enabled.
3	Reserved	R/W	Reserved for future use. Default = 0.
4	Attenuator Pin 28	R/W	Setting this bit to 0 removes the attenuators for Pin 28. Default = 1 = Attenuators Enabled.
5	Attenuator Pin 29	R/W	Setting this bit to 0 removes the attenuators for Pin 29. Default = 1 = Attenuators Enabled.
[7:6]	Reserved	R/W	Reserved for future use. Default = 00.

1. POR = 0x37, Lock = Y, SW Reset = Y.

Table 56. REGISTER 0X1A − ENHANCED ACOUSTICS REGISTER 1

Bit	Mnemonic	R/W	Description
0	En1	R/W	Setting this bit to 1 enables the enhanced acoustics mode for PWM1; 0 disables it. Default = 0.
1	En2	R/W	Setting this bit to 1 enables the enhanced acoustics mode for PWM2; 0 disables it. Default = 0.
[4:2]	Ramp Rate 1	R/W	These bits set the ramp rate for the enhanced acoustics mode for PWM1. Default = 000. **Time Slot Increase** / **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7.0 sec 100 = 8 — 4.4 sec 101 = 12 — 3.0 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
[7:5]	Ramp Rate 2	R/W	These bits set the ramp rate for the enhanced acoustics mode for PWM2. Default = 000. **Time Slot Increase** / **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7.0 sec 100 = 8 — 4.4 sec 101 = 12 — 3.0 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 57. REGISTER 0X1B − ENHANCED ACOUSTICS REGISTER 2

Bit	Mnemonic	R/W	Description
0	En3	R/W	Setting this bit to 1 enables the enhanced acoustics mode for PWM3; 0 disables it. Default = 0.
1	En4	R/W	Setting this bit to 1 enables the enhanced acoustics mode for PWM4; 0 disables it. Default = 0.
[4:2]	Ramp Rate 3	R/W	These bits set the ramp rate for the enhanced acoustics mode for PWM3. Default = 000. **Time Slot Increase** / **Time for 33% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 5 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
[7:5]	Ramp Rate 4	R/W	These bits set the ramp rate for the enhanced acoustics mode for PWM4. Default = 000. **Time Slot Increase** / **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7.0 sec 100 = 8 — 4.4 sec 101 = 12 — 3.0 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 58. REGISTER 0X1C − FAN FREEWHEELING TEST (Note 1)

Bit	Name	R/W	Description
0	Test Fan 1	R/W	Fan freewheeling test bit for Fan 1. This bit self-clears when the test is complete.
1	Test Fan 2	R/W	Fan freewheeling test bit for Fan 2. This bit self-clears when the test is complete.
2	Test Fan 3	R/W	Fan freewheeling test bit for Fan 3. This bit self-clears when the test is complete.
3	Test Fan 4	R/W	Fan freewheeling test bit for Fan 4. This bit self-clears when the test is complete.
4	Test Fan 5	R/W	Fan freewheeling test bit for Fan 5. This bit self-clears when the test is complete.
5	Test Fan 6	R/W	Fan freewheeling test bit for Fan 6. This bit self-clears when the test is complete.
6	Test Fan 7	R/W	Fan freewheeling test bit for Fan 7. This bit self-clears when the test is complete.
7	Test Fan 8	R/W	Fan freewheeling test bit for Fan 8. This bit self-clears when the test is complete.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 59. REGISTER 0X1D − FANS PRESENT (Note 1)

Bit	Name	R/W	Description
0	Fan 1 Present	R/W	Set this bit to 1 when Fan 1 is present.
1	Fan 2 Present	R/W	Set this bit to 1 when Fan 2 is present.
2	Fan 3 Present	R/W	Set this bit to 1 when Fan 3 is present.
3	Fan 4 Present	R/W	Set this bit to 1 when Fan 4 is present.
4	Fan 5 Present	R/W	Set this bit to 1 when Fan 5 is present.
5	Fan 6 Present	R/W	Set this bit to 1 when Fan 6 is present.
6	Fan 7 Present	R/W	Set this bit to 1 when Fan 7 is present.
7	Fan 8 Present	R/W	Set this bit to 1 when Fan 8 is present.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 60. REGISTER 0X1E − FAN FREEWHEELING TEST ENABLE (Note 1)

Bit	Name	R/W	Description
0	Test Fan 1	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 1.
1	Test Fan 2	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 2.
2	Test Fan 3	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 3.
3	Test Fan 4	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 4.
4	Test Fan 5	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 5.
5	Test Fan 6	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 6.
6	Test Fan 7	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 7.
7	Test Fan 8	R/W	Setting this bit to 1 enables the fan freewheeling test for Fan 8.

1. POR = 0x00, Lock = Y, SW Reset = Y.

Table 61. PWM CONFIGURATION REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x21	R/W	PWM1 Configuration Register	0x11
0x22	R/W	PWM2 Configuration Register	0x31
0x23	R/W	PWM3 Configuration Register	0x51
0x24	R/W	PWM4 Configuration Register	0x71

1. Lock = Y, SW Reset = Y.

Table 62. REGISTER 0X21, REGISTER 0X22, REGISTER 0X23, REGISTER 0X24 − PWM1, PWM2, PWM3 AND PWM4 CONFIGURATION REGISTERS

Bit	Name	R/W	Description
[2:0]	Spin-Up Timeout	R/W	These bits set the duration of the fan startup timeout and the timeout for the fan freewheeling test. 000 = No Startup Timeout 001 = 100 ms 010 = 250 ms 011 = 400 ms 100 = 667 ms 101 = 1 sec 110 = 2 sec 111 = 32 sec
3	SLOW	R/W	Setting this bit to 1 makes the ramp rate of the enhance acoustics mode four times longer.
4	INV	R/W	Setting this bit to 0, the PWM outputs are active low. Setting this bit to 1, the PWM outputs are active high (Default).
[7:5]	BHVR	R/W	These bits determine which temperature channel controls the fans in the automatic fan speed control loop. 000 = Local Temperature 001 = Remote 1 Temperature 010 = Remote 2 Temperature 011 = Remote 3 Temperature 100 = Off 101 = Maximum Fan Speed Calculated by the Local and Remote 3 Temperature Channels 110 = Maximum Fan Speed Calculated by All Four Channels 111 = Manual Mode

Table 63. REGISTER 0X25 − PWM1, PWM2 FREQUENCY (Note 1)

Bit	Name	R/W	Description
0	Min 1	R/W	When the ADT7462 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at minimum PWM1 duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T_{MIN} − hysteresis (Default); 1 = minimum PWM1 duty cycle below T_{MIN} − hysteresis.
1	Min 2	R/W	When the ADT7462 is in automatic fan control mode, this bit defines whether PWM2 is off (0% duty cycle) or at minimum PWM2 duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T_{MIN} − hysteresis (Default); 1 = minimum PWM2 duty cycle below T_{MIN} − hysteresis.
[4:2]	Low Freq 1	R/W	These bits set the frequency of PWM1 when configured in low frequency mode. 000 = 11 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
[7:5]	Low Freq 2	R/W	These bits set the frequency of PWM2 when configured in low frequency mode. 000 = 11 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz

1. POR = 0x90, Lock = Y, SW Reset = Y.

Table 64. REGISTER 0X26 − PWM3, PWM4 FREQUENCY (Note 1)

Bit	Name	R/W	Description
0	Min 3	R/W	When the ADT7462 is in automatic fan control mode, this bit defines whether PWM3 is off (0% duty cycle) or at minimum PWM3 duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T_{MIN} − hysteresis (default); 1 = minimum PWM3 duty cycle below T_{MIN} − hysteresis.
1	Min 4	R/W	When the ADT7462 is in automatic fan control mode, this bit defines whether PWM4 is off (0% duty cycle) or at minimum PWM4 duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T_{MIN} − hysteresis (default); 1 = minimum PWM4 duty cycle below T_{MIN} − hysteresis.
[4:2]	Low Freq 3	R/W	These bits set the frequency of PWM3 when configured in low frequency mode. 000 = 11 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
[7:5]	Low Freq 4	R/W	These bits set the frequency of PWM4 when configured in low frequency mode. 000 = 11 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz

1. POR = 0x90, Lock = Y, SW Reset = Y.

Table 65. MINIMUM PWMX DUTY CYCLE (Note 1)

Register Address	R/W	Description	POR Default
0x28	R/W	Minimum PWM1 duty cycle	0x80
0x29	R/W	Minimum PWM2 duty cycle	0x80
0x2A	R/W	Minimum PWM3 duty cycle	0x80
0x2B	R/W	Minimum PWM4 duty cycle	0x80

1. Lock = Y, SW Reset = Y.

Table 66. REGISTER 0X2C − MAXIMUM PWM DUTY CYCLE (Note 1)

Bit	Name	R/W	Description
[7:0]	Maximum PWM Duty Cycle	R/W	This register sets the maximum % duty cycle output in automatic fan speed control mode for all four PWM outputs.

1. POR = 0xC0, Lock = Y, SW Reset = Y.

Table 67. REGISTER 0X30 − THERMAL MASK REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	Reserved	R/W	Reserved for future use.
1	Local Temp	R/W	1 masks $\overline{\text{ALERT}}$s for an out-of-limit condition on the local temperature channel.
2	Remote 1 Temp	R/W	1 masks $\overline{\text{ALERT}}$s for an out-of-limit condition on the Remote 1 temperature channel.
3	Remote 2 Temp	R/W	1 masks $\overline{\text{ALERT}}$s for an out-of-limit condition on the Remote 2 temperature channel.
4	Remote 3 Temp	R/W	1 masks $\overline{\text{ALERT}}$s for an out-of-limit condition on the Remote 3 temperature channel.
5	Diode 1 Error	R/W	1 masks $\overline{\text{ALERT}}$s for an open or short condition on the Remote 1 channel.
6	Diode 2 Error	R/W	1 masks $\overline{\text{ALERT}}$s for an open or short condition on the Remote 2 channel.
7	Diode 3 Error	R/W	1 masks $\overline{\text{ALERT}}$s for an open or short condition on the Remote 3 channel.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 68. REGISTER 0X31 − THERMAL MASK REGISTER 2 (Note 1)

Bit	Name	R/W	Description
0	$\overline{\text{THERM1}}$ %	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.
1	$\overline{\text{THERM1}}$ Assert	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.
2	$\overline{\text{THERM1}}$ State	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.
3	$\overline{\text{THERM2}}$ %	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.
4	$\overline{\text{THERM2}}$ Assert	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.
5	$\overline{\text{THERM2}}$ State	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.
6	VRD1_Assert	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1.
7	VRD2_Assert	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1.

1. POR = 0xC0, Lock = N, SW Reset = Y.

Table 69. REGISTER 0X32 − VOLTAGE MASK REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	+12V1	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
1	+12V2	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
2	+12V3	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
3	+3.3V	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
4	Pin 15 Voltage	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
5	Pin 19 Voltage	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
6	+5V	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
7	Pin 23 Voltage	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 70. REGISTER 0X33 − VOLTAGE MASK REGISTER 2 (Note 1)

Bit	Name	R/W	Description
[2:0]	Reserved	R/W	Reserved for future use.
3	Pin 24 Voltage	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
4	Pin 25 Voltage	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
5	Pin 26 Voltage	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
6	+1.5V2 (3GIO)	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
7	+1.5V1 (ICH)	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 71. REGISTER 0X34 − FAN MASK REGISTER (Note 1)

Bit	Name	R/W	Description
0	Fan 1 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
1	Fan 2 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
2	Fan 3 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
3	Fan 4 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
4	Fan 5 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
5	Fan 6 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
6	Fan 7 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
7	Fan 8 Fault	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 72. REGISTER 0X35 − DIGITAL MASK REGISTER (Note 1)

Bit	Name	R/W	Description
[2:0]	Reserved	R	Reserved for future use.
3	$\overline{\text{FAN2MAX}}$	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1.
4	SCSI1	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1.
5	SCSI2	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 1.
6	VID Comparison	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.
7	Chassis Intrusion	R/W	1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit. Default = 0.

1. POR = 0x38, Lock = N, SW Reset = Y.

Table 73. REGISTER 0X36 − GPIO MASK REGISTER (Note 1)

Bit	Name	R/W	Description
0	GPIO1	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
1	GPIO2	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
2	GPIO3	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
3	GPIO4	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
4	GPIO5	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
5	GPIO6	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
6	GPIO7	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.
7	GPIO8	R/W	A 1 masks $\overline{\text{ALERT}}$s for the corresponding interrupt status bit.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 74. REGISTER 0X37 − EDO 1 MASK REGISTER (Note 1)

Bit	Name	R/W	Description
0	GPIO1	R/W	A 1 masks GPIO1 from causing an EDO1 assertion.
1	GPIO2	R/W	A 1 masks GPIO2 from causing an EDO1 assertion.
2	GPIO3	R/W	A 1 masks GPIO3 from causing an EDO1 assertion.
3	GPIO4	R/W	A 1 masks GPIO4 from causing an EDO1 assertion.
4	Reserved	R/W	Unused.
5	Fan	R/W	A 1 masks a fan-fail condition from causing an EDO1 assertion.
6	Temp	R/W	A 1 masks a $\overline{\text{THERM}}$ condition from causing an EDO1 assertion.
7	Volt	R/W	A 1 masks a voltage exceed limit condition from causing an EDO1 assertion.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 75. REGISTER 0X38 − EDO 2 MASK REGISTER (Note 1)

Bit	Name	R/W	Description
0	GPIO1	R/W	A 1 masks GPIO1 from causing an EDO2 assertion.
1	GPIO2	R/W	A 1 masks GPIO2 from causing an EDO2 assertion.
2	GPIO3	R/W	A 1 masks GPIO3 from causing an EDO2 assertion.
3	GPIO4	R/W	A 1 masks GPIO4 from causing an EDO2 assertion.
4	Reserved	R/W	Unused.
5	Fan	R/W	A 1 masks a fan-fail condition from causing an EDO2 assertion.
6	Temp	R/W	A 1 masks a $\overline{\text{THERM}}$ condition from causing an EDO2 assertion.
7	Volt	R/W	A 1 masks a voltage exceed limit condition from causing an EDO2 assertion.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 76. REGISTER 0X3D − DEVICE ID REGISTER (Note 1)

Bit	Name	R/W	Description
[7:0]	Device ID	R	This register contains the device ID (0x62) for the ADT7462.

1. POR = 0x62, SW Reset = N.

Table 77. REGISTER 0X3E − COMPANY ID REGISTER (Note 1)

Bit	Name	R/W	Description
[7:0]	Company ID	R	This register contains the company ID (0x41) for the ADT7462.

1. POR = 0x41, SW Reset = N.

Table 78. REGISTER 0X3F − REVISION REGISTER (Note 1)

Bit	Name	R/W	Description
[7:0]	Revision ID	R	This register contains the revision ID (0x04) for the ADT7462.

1. POR = 0x04, SW Reset = N.

Table 79. TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	Lockable	POR Default
0x44	R/W	Local low temperature limit.	No	0x40
0x45	R/W	Remote 1 low temperature/Pin 15 voltage low limit.	No	0x40
0x46	R/W	Remote 2 low temperature limit.	No	0x40
0x47	R/W	Remote 3 low temperature/Pin 19 voltage low limit.	No	0x40
0x48	R/W	Local high temperature limit.	No	0x95
0x49	R/W	Remote 1 high temperature/Pin 15 voltage high limit.	No	0x95
0x4A	R/W	Remote 2 high temperature limit.	No	0x95
0x4B	R/W	Remote 3 high temperature/Pin 19 voltage high limit.	No	0x95
0x4C	R/W	Local $\overline{\text{THERM1}}$ temperature limit/+1.5V2 (3GIO) voltage high limit.	Yes	0xA4
0x4D	R/W	Remote 1 $\overline{\text{THERM1}}$ temperature limit.	Yes	0xA4
0x4E	R/W	Remote 2 $\overline{\text{THERM1}}$ temperature limit.	Yes	0xA4
0x4F	R/W	Remote 3 $\overline{\text{THERM1}}$ temperature limit.	Yes	0xA4
0x50	R/W	Local $\overline{\text{THERM2}}$ temperature limit/+1.5V1 (ICH) voltage high limit.	Yes	0xA4
0x51	R/W	Remote 1 $\overline{\text{THERM2}}$ temperature limit.	Yes	0xA4
0x52	R/W	Remote 2 $\overline{\text{THERM2}}$ temperature limit.	Yes	0xA4
0x53	R/W	Remote 3 $\overline{\text{THERM2}}$ temperature limit.	Yes	0xA4

1. SW Reset = N.

Table 80. REGISTER 0X54 − LOCAL/REMOTE 1 TEMPERATURE HYSTERESIS (Note 1)

Bit	Name	R/W	Description
[3:0]	Remote 1 Hysteresis	R/W	These four bits set the Remote 1 $\overline{\text{THERM}}$ hysteresis value, 1 LSB = 1°C.
[7:4]	Local Hysteresis	R/W	These four bits set the local $\overline{\text{THERM}}$ hysteresis value, 1 LSB = 1°C. 0000 = 0°C 0001 = 1°C 0010 = 2°C 0011 = 3°C 0100 = 4°C (Default) 0101 = 5°C 0110 = 6°C 0111 = 7°C 1000 = 8°C 1001 = 9°C 1010 = 10°C 1011 = 11°C 1100 = 12°C 1101 = 13°C 1110 = 14°C 1111 = 15°C

1. POR = 0x44, Lock = Y, SW Reset = N.

Table 81. REGISTER 0X55 − REMOTE 2/REMOTE 3 TEMPERATURE HYSTERESIS (Note 1)

Bit	Name	R/W	Description
[3:0]	Remote 3 Hysteresis	R/W	These four bits set the Remote 3 $\overline{\text{THERM}}$ hysteresis value, 1 LSB = 1°C.
[7:4]	Remote 2 Hysteresis	R/W	These four bits set the Remote 2 $\overline{\text{THERM}}$ hysteresis value, 1 LSB = 1°C. 0000 = 0°C 0001 = 1°C 0010 = 2°C 0011 = 3°C 0100 = 4°C (Default) 0101 = 5°C 0110 = 6°C 0111 = 7°C 1000 = 8°C 1001 = 9°C 1010 = 10°C 1011 = 11°C 1100 = 12°C 1101 = 13°C 1110 = 14°C 1111 = 15°C

1. POR = 0x44, Lock = Y, SW Reset = N.

Table 82. OFFSET REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x56	R/W	Local offset, resolution = 0.5°C.	0x00
0x57	R/W	Remote 1 offset, resolution = 0.5°C.	0x00
0x58	R/W	Remote 2 offset, resolution = 0.5°C.	0x00
0x59	R/W	Remote 3 offset, resolution = 0.5°C.	0x00

1. Lock = Y, SW Reset = N.

Table 83. OPERATING POINT REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x5A	R/W	Remote 1 operating point.	0xA4
0x5B	R/W	Remote 2 operating point.	0xA4

1. Lock = Y, SW Reset = Y.

Table 84. TIMING REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x5C	R/W	Local temperature T_{MIN}.	0x9A
0x5D	R/W	Remote 1 temperature T_{MIN}.	0x9A
0x5E	R/W	Remote 2 temperature T_{MIN}.	0x9A
0x5F	R/W	Remote 3 temperature T_{MIN}.	0x9A

1. Lock = Y, SW Reset = Y.

Table 85. T_{RANGE}/HYSTERESIS REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x60	R/W	Local T_{RANGE}/Hysteresis	0xC4
0x61	R/W	Remote 1 T_{RANGE}/Hysteresis	0xC4
0x62	R/W	Remote 2 T_{RANGE}/Hysteresis	0xC4
0x63	R/W	Remote 3 T_{RANGE}/Hysteresis	0xC4

1. Lock = Y, SW Reset = Y.

Table 86. REGISTER 0X60, REGISTER 61, REGISTER 62, REGISTER 63 − LOCAL, REMOTE 1, REMOTE 2, AND REMOTE 3 T_{RANGE}/HYSTERESIS

Bit	Name	R/W	Description
[3:0]	Hysteresis	R/W	These four bits set the hysteresis in the automatic fan speed control loop and in the dynamic T_{MIN} control loop, 1 LSB = 1°C. 0000 = 0°C 0001 = 1°C 0010 = 2°C 0011 = 3°C 0100 = 4°C (Default) 0101 = 5°C 0110 = 6°C 0111 = 7°C 1000 = 8°C 1001 = 9°C 1010 = 10°C 1011 = 11°C 1100 = 12°C 1101 = 13°C 1110 = 14°C 1111 = 15°C
[7:4]	Range	R/W	These four bits set the T_{RANGE} value, that is, the slope or rate of change of fan speed with respect to temperature in the automatic fan speed control loop. 0000 = 2°C 0001 = 2.5°C 0010 = 3.3°C 0011 = 4°C 0100 = 5°C 0101 = 6.7°C 0110 = 8°C 0111 = 10°C 1000 = 13.3°C 1001 = 16°C 1010 = 20°C 1011 = 26.7°C 1100 = 32°C (Default) 1101 = 40°C 1110 = 53.3°C 1111 = 80°C

Table 87. REGISTER 0X64 − OPERATING POINT HYSTERESIS (Note 1)

Bit	Name	R/W	Description
[3:0]	Reserved	R	Reserved for future use.
[7:4]	Operating Point Hysteresis	R/W	These four bits set the operating point hysteresis for the dynamic T_{MIN} control loop, 1 LSB = 1°C. 0000 = 0°C 0001 = 1°C 0010 = 2°C 0011 = 3°C 0100 = 4°C (Default) 0101 = 5°C 0110 = 6°C 0111 = 7°C 1000 = 8°C 1001 = 9°C 1010 = 10°C 1011 = 11°C 1100 = 12°C 1101 = 13°C 1110 = 14°C 1111 = 15°C

1. POR = 0x40, Lock = Y, SW Reset = Y.

Table 88. VOLTAGE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x68	R/W	+3.3V high limit.	0xFF
0x69	R/W	Pin 23 voltage high limit.	0xFF
0x6A	R/W	Pin 24 voltage high limit.	0xFF
0x6B	R/W	Pin 25 voltage high limit.	0xFF
0x6C	R/W	Pin 26 voltage high limit.	0xFF
0x6D	R/W	+12V1 voltage low limit.	0x00
0x6E	R/W	+12V2 voltage low limit.	0x00
0x6F	R/W	+12V3 voltage low limit.	0x00
0x70	R/W	+3.3V low limit.	0x00
0x71	R/W	+5V low limit.	0x00
0x72	R/W	Pin 23 voltage low limit.	0x20
0x73	R/W	Pin 24 voltage low limit.	0x00
0x74	R/W	Pin 25 voltage low limit.	0x00
0x75	R/W	Pin 26 voltage low limit.	0x80
0x76	R/W	+1.5V2 (3GIO) voltage low limit.	0x00
0x77	R/W	+1.5V1 (ICH) voltage low limit.	0x00

1. Lock = N, SW Reset = N.

Table 89. TACH LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x78	R/W	TACH1 limit/VID limit.	0xFF
0x79	R/W	TACH2 limit.	0xFF
0x7A	R/W	TACH3 limit.	0xFF
0x7B	R/W	TACH4 limit.	0xFF
0x7C	R/W	TACH5 limit/+12V1 voltage high limit.	0xFF
0x7D	R/W	TACH6 limit/+12V2 voltage high limit.	0xFF
0x7E	R/W	TACH7 limit/+5V voltage high limit.	0xFF
0x7F	R/W	TACH8 limit/+12V3 voltage high limit.	0xFF

1. Lock = Y, SW Reset = N.

Table 90. $\overline{\text{THERM}}$ TIMER LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x80	R/W	$\overline{\text{THERM1}}$ Timer Limit.	0xFF
0x81	R/W	$\overline{\text{THERM2}}$ Timer Limit.	0xFF

1. Lock = Y, SW Reset = N.

Table 91. TEMPERATURE VALUE REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x88	R	Bits [7:6] Local temperature value, LSBs.	0x00
0x89	R	Local temperature value, MSBs.	0x00
0x8A	R	Bits [7:6] Remote 1 temperature value, LSBs.	0x00
0x8B	R	Remote 1 temperature value, MSBs/Pin 15 voltage.	0x00
0x8C	R	Bits [7:6] Remote 2 temperature value, LSBs.	0x00
0x8D	R	Remote 2 temperature value, MSBs.	0x00
0x8E	R	Bits [7:6] Remote 3 temperature value, LSBs.	0x00
0x8F	R	Remote 3 temperature value, MSBs/Pin 19 voltage.	0x00

1. Lock = N, SW Reset = N.

Table 92. VOLTAGE VALUE REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x90	R	Pin 23 voltage value.	0x00
0x91	R	Pin 24 voltage value.	0x00
0x92	R	Pin 25 voltage value.	0x00
0x93	R	Pin 26 voltage value.	0x00
0x94	R	+1.5V1 (ICH) voltage value.	0x00
0x95	R	+1.5V2 (3GIO) voltage value.	0x00
0x96	R	+3.3V voltage value.	0x00

1. Lock = N, SW Reset = N.

Table 93. VID VALUE REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x97	R	This register reports the state of the seven VID inputs.	0x00

1. Lock = N, SW Reset = N.

Table 94. TACH VALUE REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0x98	R	TACH1, LSB.	0xFF
0x99	R	TACH1, MSB.	0xFF
0x9A	R	TACH2, LSB.	0xFF
0x9B	R	TACH2, MSB.	0xFF
0x9C	R	TACH3, LSB.	0xFF
0x9D	R	TACH3, MSB.	0xFF
0x9E	R	TACH4, LSB.	0xFF
0x9F	R	TACH4, MSB.	0xFF
0xA2	R	TACH5, LSB.	0xFF
0xA3	R	TACH5, MSB/+12V1 voltage value register.	0xFF
0xA4	R	TACH6, LSB.	0xFF
0xA5	R	TACH6, MSB/+12V2 voltage value register.	0xFF
0xA6	R	TACH7, LSB.	0xFF
0xA7	R	TACH7, MSB/+5V voltage value register.	0xFF
0xA8	R	TACH8, LSB.	0xFF
0xA9	R	TACH8, MSB/+12V3 voltage value register.	0xFF

1. Lock = N, SW Reset = N.

Table 95. PWM CURRENT DUTY CYCLE REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0xAA	R/W	PWM1 current duty cycle.	0x00
0xAB	R/W	PWM2 current duty cycle.	0x00
0xAC	R/W	PWM3 current duty cycle.	0xC0
0xAD	R/W	PWM4 current duty cycle.	0x00

1. Lock = N, SW Reset = N.

Table 96. $\overline{\text{THERM}}$ TIMER VALUE REGISTERS (Note 1)

Register Address	R/W	Description	POR Default
0xAE	R	$\overline{\text{THERM1}}$ timer % on-time value.	0x00
0xAF	R	$\overline{\text{THERM2}}$ timer % on-time value.	0x00

1. Lock = N, SW Reset = N.

Table 97. REGISTER 0XB8 − HOST THERMAL STATUS REGISTER 1 (Note 1)**;**
REGISTER 0XC0 − BMC THERMAL STATUS REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	Reserved	R	Reserved for future use.
1	Local Temp	R	A 1 indicates that a local temperature limit has been tripped.
2	Remote 1 Temp	R	A 1 indicates that a Remote 1 temperature limit has been tripped.
3	Remote 2 Temp	R	A 1 indicates that a Remote 2 temperature limit has been tripped.
4	Remote 3 Temp	R	A 1 indicates that a Remote 3 temperature limit has been tripped.
5	Diode 1 Error	R	A 1 indicates that a Remote 1 diode error, either an open or a short, has occurred.
6	Diode 2 Error	R	A 1 indicates that a Remote 2 diode error, either an open or a short, has occurred.
7	Diode 3 Error	R	A 1 indicates that a Remote 3 diode error, either an open or a short, has occurred.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 98. REGISTER 0XB9 − HOST THERMAL STATUS REGISTER 2 (Note 1)**;**
REGISTER 0XC1 − BMC THERMAL STATUS REGISTER 2 (Note 1)

Bit	Name	R/W	Description
0	$\overline{\text{THERM1}}$ %	R	A 1 indicates that $\overline{\text{THERM1}}$ has been asserted for longer than the programmed $\overline{\text{THERM1}}$ timer limit.
1	$\overline{\text{THERM1}}$ Assert	R	A 1 indicates that $\overline{\text{THERM1}}$ is asserted.
2	$\overline{\text{THERM1}}$ State	R	A 1 indicates that a transition from high to low has taken place on the $\overline{\text{THERM1}}$ pin.
3	$\overline{\text{THERM2}}$ %	R	A 1 indicates that $\overline{\text{THERM2}}$ has been asserted for longer than the programmed $\overline{\text{THERM2}}$ timer limit.
4	$\overline{\text{THERM2}}$ Assert	R	A 1 indicates that $\overline{\text{THERM2}}$ is asserted.
5	$\overline{\text{THERM2}}$ State	R	A 1 indicates that a transition from high to low has taken place on the $\overline{\text{THERM2}}$ pin.
6	VRD1_Assert	R	A 1 indicates that VRD1 is asserted.
7	VRD2_Assert	R	A 1 indicates that VRD2 is asserted.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 99. REGISTER 0XBA − HOST THERMAL STATUS REGISTER 3 (Note 1)

Bit	Name	R/W	Description
0	Local $\overline{\text{THERM1}}$	R	A 1 indicates that the local $\overline{\text{THERM1}}$ limit has been exceeded.
1	Remote 1 $\overline{\text{THERM1}}$	R	A 1 indicates that the Remote 1 $\overline{\text{THERM1}}$ limit has been exceeded.
2	Remote 2 $\overline{\text{THERM1}}$	R	A 1 indicates that the Remote 2 $\overline{\text{THERM1}}$ limit has been exceeded.
3	Remote 3 $\overline{\text{THERM1}}$	R	A 1 indicates that the Remote 3 $\overline{\text{THERM1}}$ limit has been exceeded.
4	Local $\overline{\text{THERM2}}$	R	A 1 indicates that the Local $\overline{\text{THERM2}}$ limit has been exceeded.
5	Remote 1 $\overline{\text{THERM2}}$	R	A 1 indicates that the Remote 1 $\overline{\text{THERM2}}$ limit has been exceeded.
6	Remote 2 $\overline{\text{THERM2}}$	R	A 1 indicates that the Remote 2 $\overline{\text{THERM2}}$ limit has been exceeded.
7	Remote 3 $\overline{\text{THERM2}}$	R	A 1 indicates that the Remote 3 $\overline{\text{THERM2}}$ limit has been exceeded.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 100. REGISTER 0XBB − HOST VOLTAGE STATUS REGISTER 1 (Note 1)**;**
REGISTER 0XC3 − BMC VOLTAGE REGISTER 1 (Note 1)

Bit	Name	R/W	Description
0	+12V1	R	A 1 indicates that a +12V1 voltage limit has been tripped.
1	+12V2	R	A 1 indicates that a +12V2 voltage limit has been tripped.
2	+12V3	R	A 1 indicates that a +12V3 voltage limit has been tripped.
3	+3.3V	R	A 1 indicates that a +3.3V voltage limit has been tripped.
4	Pin 15 Voltage	R	A 1 indicates that a Pin 15 voltage limit has been tripped.
5	Pin 19 Voltage	R	A 1 indicates that a Pin 19 voltage limit has been tripped.
6	+5V	R	A 1 indicates that a +5V voltage limit has been tripped.
7	Pin 23 Voltage	R	A 1 indicates that a Pin 23 voltage limit has been tripped.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 101. REGISTER 0XBC − HOST VOLTAGE STATUS REGISTER 2 (Note 1)**;**
REGISTER 0XC4 − BMC VOLTAGE STATUS REGISTER 2 (Note 1)

Bit	Name	R/W	Description
[2:0]	Reserved	R	Reserved for future use.
3	Pin 24 Voltage	R	A 1 indicates that a Pin 24 voltage limit has been tripped.
4	Pin 25 Voltage	R	A 1 indicates that a Pin 25 voltage limit has been tripped.
5	Pin 26 Voltage	R	A 1 indicates that a Pin 26 voltage limit has been tripped.
6	+1.5V2 (3GIO)	R	A 1 indicates that a +1.5V2 (3GIO) voltage limit has been tripped.
7	+1.5V1 (ICH)	R	A 1 indicates that a +1.5V1 (ICH) voltage limit has been tripped.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 102. REGISTER 0XBD − HOST FAN STATUS REGISTER (Note 1)**;**
REGISTER 0XC5 − BMC FAN STATUS REGISTER (Note 1)

Bit	Name	R/W	Description
0	Fan 1 Fault	R	A 1 indicates a Fan 1 fault.
1	Fan 2 Fault	R	A 1 indicates a Fan 2 fault.
2	Fan 3 Fault	R	A 1 indicates a Fan 3 fault.
3	Fan 4 Fault	R	A 1 indicates a Fan 4 fault.
4	Fan 5 Fault	R	A 1 indicates a Fan 5 fault.
5	Fan 6 Fault	R	A 1 indicates a Fan 6 fault.
6	Fan 7 Fault	R	A 1 indicates a Fan 7 fault.
7	Fan 8 Fault	R	A 1 indicates a Fan 8 fault.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 103. REGISTER 0XBE − HOST DIGITAL STATUS REGISTER (Note 1)**;**
REGISTER 0XC6 − BMC DIGITAL STATUS REGISTER (Note 1)

Bit	Name	R/W	Description
[2:0]	Reserved	R	Reserved for future use.
3	$\overline{\text{FAN2MAX}}$	R	A 1 indicates that the $\overline{\text{FAN2MAX}}$ has been asserted as an input.
4	SCSI1	R	A 1 indicates that the SCSI_TERM1 digital input has been asserted.
5	SCSI2	R	A 1 indicates that the SCSI_TERM2 digital input has been asserted.
6	VID Comparison	R	A 1 indicates a VID comparison fault.
7	Chassis Intrusion	R	A 1 indicates that the chassis intrusion digital input has been asserted.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 104. REGISTER 0XBF − HOST GPIO STATUS REGISTER (Note 1)

Bit	Name	R/W	Description
0	GPIO1	R/W	A 1 indicates that GPIO1 is asserted.
1	GPIO2	R/W	A 1 indicates that GPIO2 is asserted.
2	GPIO3	R/W	A 1 indicates that GPIO3 is asserted.
3	GPIO4	R/W	A 1 indicates that GPIO4 is asserted.
4	GPIO5	R/W	A 1 indicates that GPIO5 is asserted.
5	GPIO6	R/W	A 1 indicates that GPIO6 is asserted.
6	GPIO7	R/W	A 1 indicates that GPIO7 is asserted.
7	GPIO8	R/W	A 1 indicates that GPIO8 is asserted.

1. POR = 0x00, Lock = N, SW Reset = Y.

Table 105. ORDERING INFORMATION

Device Number*	Temperature Range	Package Type	Package Option	Shipping†
ADT7462ACPZ−REEL	−40°C to +125°C	32-lead LFCSP_VQ	CP−32−2	5,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The “Z” suffix indicates Pb−Free part.

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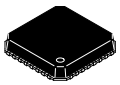
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

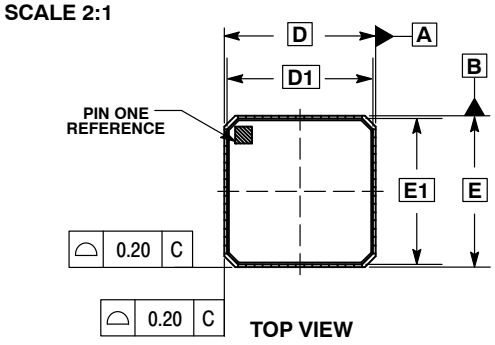
ON Semiconductor®

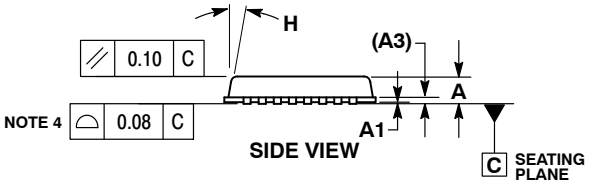
LFCSP32 5x5, 0.5P
CASE 932AE−01
ISSUE A

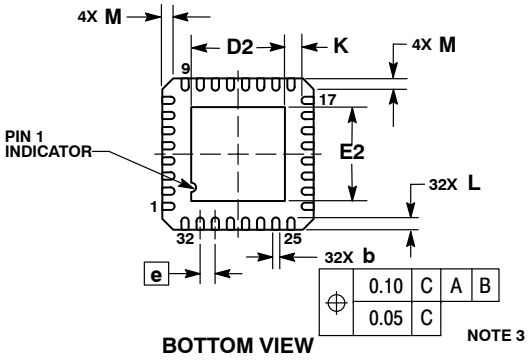
DATE 27 JAN 2009



SCALE 2:1



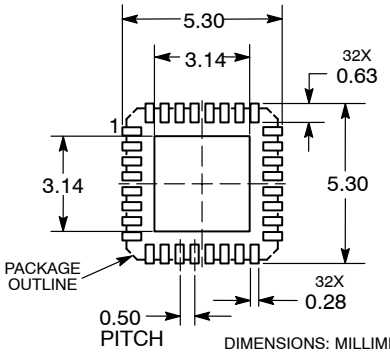




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D1	4.75 BSC	
D2	2.95	3.25
E	5.00 BSC	
E1	4.75 BSC	
E2	2.95	3.25
e	0.50 BSC	
H	---	12°
K	0.20	---
L	0.30	0.50
M	---	0.60

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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