

# 8-Bit Dual Supply Configurable Voltage Interface Transceiver

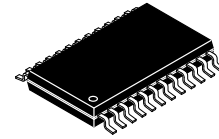
with 3-STATE Outputs

## 74LVXC3245

The LVXC3245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The  $V_{CCA}$  pin accepts a 3 V supply level. The A Port is a dedicated 3 V port. The  $V_{CCB}$  pin accepts a 3 V-to-5 V supply level. The B Port is configured to track the  $V_{CCB}$  supply level respectively. A 5 V level on the  $V_{CC}$  pin will configure the I/O pins at a 5 V level and a 3 V  $V_{CC}$  will configure the I/O pins at a 3 V level. The A Port should interface with a 3 V host system and the B Port to the card slots. This device will allow the  $V_{CCB}$  voltage source pin and I/O pins on the B Port to float when  $\overline{OE}$  is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

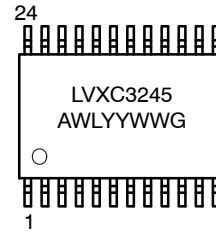
### Features

- Bidirectional Interface Between 3.0 V and 3 V-to-5 V Buses
- Control Inputs Compatible with TTL Level
- Outputs Source/Sink Up to 24 mA
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Implements Proprietary EMI Reduction Circuitry
- Flexible  $V_{CCB}$  Operating Range
- Allows B Port and  $V_{CCB}$  to Float Simultaneously When  $\overline{OE}$  is HIGH
- Functionally Compatible With the 74 Series 245
- These Devices are Pb-Free and are RoHS Compliant



TSSOP24  
CASE 948AR

### MARKING DIAGRAMS



LVXC3245 = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 Y = Year  
 WW, W = Work Week  
 G = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# 74LVXC3245

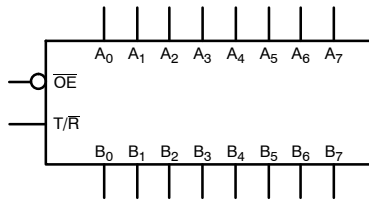


Figure 1. Logic Symbol/s

## PIN DESCRIPTIONS

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/R	Transmit / Receive Input
A <sub>0</sub> – A <sub>7</sub>	Side A Inputs or 3-STATE Outputs
B <sub>0</sub> – B <sub>7</sub>	Side B Inputs or 3-STATE Outputs

## TRUTH TABLE/s

Inputs		Outputs
$\overline{OE}$	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

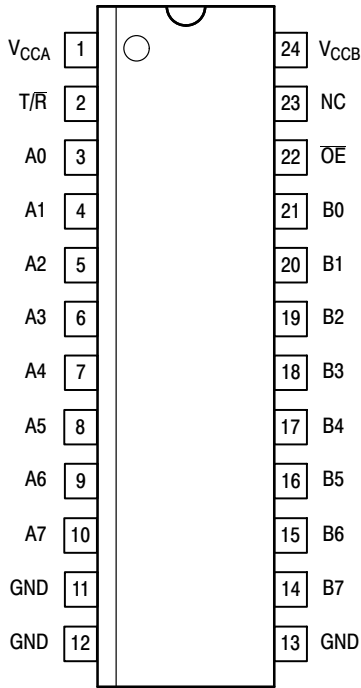


Figure 2. Connection Diagram/s

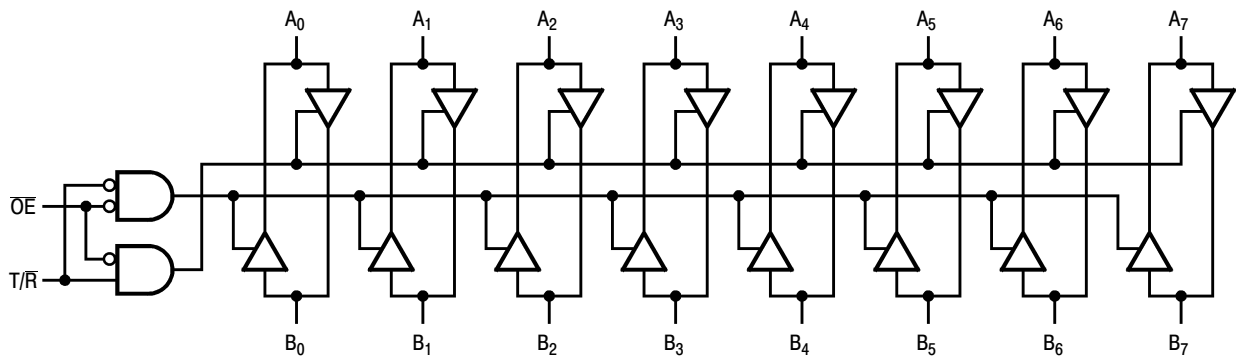


Figure 3. Logic Diagram

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## ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Condition	Unit
$V_{CCA}, V_{CCB}$	Supply Voltage	-0.5 to +6.5		V
$V_I$	DC Input Voltage $\overline{OE}, T/R$	-0.5 to $V_{CCA} + 0.5$		V
$V_{I/O}$	DC Input/Output Voltage An	-0.5 to $V_{CCA} + 0.5$		V
		Bn	-0.5 to $V_{CCB} + 0.5$	V
$I_{IK}$	DC Input Diode Current $\overline{OE}, T/R$	$\pm 20$		mA
$I_{OK}$	DC Output Diode Current	$\pm 50$		mA
$I_O$	DC Output Source or Sink Current	$\pm 50$		mA
$I_{CC}, I_{GND}$	DC $V_{CC}$ or Ground Current Per Output Pin Max Current	$\pm 50$ $\pm 200$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		$^{\circ}C$
	DC Latch-Up Source or Sink Current	$\pm 100$		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Min	Max	Unit
$V_{CCA}, V_{CCB}$	Supply Voltage $V_{CCA}$ $V_{CCB}$	2.7	3.6	V
		3.0	5.5	
$V_I$	Input Voltage $\overline{OE}, T/R$	0	$V_{CCA}$	V
$V_{I/O}$	Input/Output Voltage An Bn	0	$V_{CCA}$	V
		0	$V_{CCB}$	
$T_A$	Free-Air Operating Temperature	-40	+85	$^{\circ}C$
$\Delta t/\Delta V$	Minimum Input Edge Rate $V_{IN}$ from 30% to 70% of $V_{CC}$ ; $V_{CC}$ at 3.0 V, 4.5 V, 5.5 V	0	8	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
- The A Port unused pins (inputs or I/Os) must be held HIGH or LOW. They may not float.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25 °C		T <sub>A</sub> = -40 to +85 °C		Unit	
						Typ	Guaranteed Limits				
V <sub>IHA</sub>	Minimum HIGH Level Input Voltage	An OE T/R	V <sub>OUT</sub> ≤ 0.1 V or ≥ V <sub>CC</sub> - 0.1 V	2.7	3.0		2.0	2.0	V		
					3.0	3.6		2.0		2.0	
V <sub>IHB</sub>		Bn		2.7	3.0		2.00	2.00	V		
				3.0	3.6		2.00	2.00			
				3.6	5.5		3.85	3.85			
V <sub>ILA</sub>	Maximum LOW Level Input Voltage	An OE T/R	V <sub>OUT</sub> ≤ 0.1 V or ≥ V <sub>CC</sub> - 0.1 V	2.7	3.0		0.8	0.8	V		
						3.0	3.6			0.8	0.8
V <sub>ILB</sub>		Bn		2.7	3.0		0.80	0.80	V		
				3.0	3.6		0.80	0.80			
				3.6	5.5		1.65	1.65			
V <sub>OHA</sub>	Minimum HIGH Level Output Voltage		I <sub>OUT</sub> = -100 μA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA	3.0	3.0	2.99	2.90	2.90	V		
						3.0	3.0	2.85		2.56	2.46
						3.0	3.0	2.65		2.35	2.25
						2.7	3.0	2.50		2.30	2.20
						2.7	4.5	2.30		2.10	2.00
						3.0	4.5	2.30		2.10	2.00
V <sub>OHB</sub>			I <sub>OUT</sub> = -100 μA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA	3.0	3.0	2.99	2.90	2.90	V		
				3.0	3.0	2.85	2.56	2.46			
				3.0	3.0	2.65	2.35	2.25			
				3.0	3.0	2.65	2.35	2.25			
				3.0	4.5	4.25	3.86	3.76			
				3.0	4.5	4.25	3.86	3.76			
V <sub>OLA</sub>	Maximum LOW Level Output Voltage		I <sub>OUT</sub> = 100 μA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 24 mA	3.0	3.0	0.002	0.10	0.10	V		
						3.0	3.0	0.21		0.36	0.44
						2.7	3.0	0.11		0.36	0.44
						2.7	4.5	0.22		0.42	0.50
						3.0	4.5	0.22		0.42	0.50
V <sub>OLB</sub>			I <sub>OUT</sub> = 100 μA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA	3.0	3.0	0.002	0.10	0.10	V		
				3.0	3.0	0.21	0.36	0.44			
				3.0	3.0	0.21	0.36	0.44			
				3.0	4.5	0.18	0.36	0.44			
				3.0	4.5	0.18	0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	OE, T/R	V <sub>I</sub> = V <sub>CCA</sub> , GND	3.6	3.6		±0.1	±1.0	μA		
				3.6	5.5		±0.1	±1.0			
I <sub>OZA</sub>	Maximum 3-State Output Leakage	An	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> OE = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCA</sub> , GND	3.6	3.6		±0.5	±5.0	μA		
				3.6	5.5		±0.5	±5.0			
I <sub>OZB</sub>	Maximum 3-State Output Leakage	Bn	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> OE = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCB</sub> , GND	3.6	3.6		±0.5	±5.0	μA		
				3.6	5.5		±0.5	±5.0			
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	Bn	V <sub>I</sub> = V <sub>CCB</sub> - 2.1 V	3.6	5.5	1.0	1.35	1.5	mA		
		All Inputs	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V	3.6	3.6		0.35	0.5	mA		
I <sub>CCA1</sub>	Quiescent V <sub>CCA</sub> Supply Current as B Port Floats		An = V <sub>CCA</sub> or GND Bn = Open, OE = V <sub>CCA</sub> , T/R = V <sub>CCA</sub> , V <sub>CCB</sub> = Open	3.6	Open		5	50	μA		
I <sub>CCA2</sub>	Quiescent V <sub>CCA</sub> Supply Current		An = V <sub>CCA</sub> or GND Bn = V <sub>CCB</sub> or GND, OE = GND, T/R = GND	3.6	3.6		5	50	μA		
				3.6	5.5		5	50			
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current		An = V <sub>CCA</sub> or GND Bn = V <sub>CCB</sub> or GND, OE = GND, T/R = V <sub>CCA</sub>	3.6	3.6		5	50	μA		
				3.6	5.5		8	80			

## NOISE CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25 °C		Unit
					Typ	Limit	
V <sub>OLPA</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	(Note 3), (Note 4)	3.3	3.3		0.8	V
			3.3	5.0		0.8	
V <sub>OLPB</sub>		(Note 3), (Note 4)	3.3	3.3		0.8	V
			3.3	5.0		1.5	
V <sub>OLVA</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	(Note 3), (Note 4)	3.3	3.3		-0.8	V
			3.3	5.0		-0.8	
V <sub>OLVB</sub>		(Note 3), (Note 4)	3.3	3.3		-0.8	V
			3.3	5.0		-1.2	
V <sub>IHDA</sub>	Minimum HIGH Level Dynamic Input Voltage	(Note 3), (Note 5)	3.3	3.3		2.0	V
			3.3	5.0		2.0	
V <sub>IHDB</sub>		(Note 3), (Note 5)	3.3	3.3		2.0	V
			3.3	5.0		3.5	
V <sub>ILDA</sub>	Maximum LOW Level Dynamic Input Voltage	(Note 3), (Note 5)	3.3	3.3		0.8	V
			3.3	5.0		0.8	
V <sub>ILDB</sub>		(Note 3), (Note 5)	3.3	3.3		0.8	V
			3.3	5.0		1.5	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Worst case package.

4. Max number of outputs defined as (n). Data inputs are driven 0 V to V<sub>CC</sub> level; one output at GND.

5. Max number of data inputs (n) switching. (n-1) inputs switching 0 V to V<sub>CC</sub> level. Input under test switching: V<sub>CC</sub> level to threshold (V<sub>IHD</sub>), 0 V to threshold (V<sub>ILD</sub>), f = 1 MHz.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T <sub>A</sub> = +25 °C; C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7-3.6 V V <sub>CCB</sub> = 4.5-5.5 V			T <sub>A</sub> = -40 °C to +85 °C; C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7-3.6 V V <sub>CCB</sub> = 4.5-5.5 V		T <sub>A</sub> = +25 °C; C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7-3.6 V V <sub>CCB</sub> = 3.0-3.6 V			T <sub>A</sub> = -40 °C to +85 °C; C <sub>L</sub> = 50 pF V <sub>CCA</sub> = 2.7-3.6 V V <sub>CCB</sub> = 3.0-3.6 V		Unit
		Min	Typ (Note 6)	Max	Min	Max	Min	Typ (Note 7)	Max	Min	Max	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay A to B	1.0 1.0	4.8 3.9	8.0 6.5	1.0 1.0	8.5 7.0	1.0 1.0	5.5 5.2	8.5 8.0	1.0 1.0	9.0 8.5	ns
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay B to A	1.0 1.0	3.8 4.3	6.5 7.5	1.0 1.0	7.0 8.0	1.0 1.0	4.4 5.1	7.0 7.5	1.0 1.0	7.5 8.0	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to B	1.0 1.0	4.7 4.8	8.0 8.5	1.0 1.0	8.5 9.0	1.0 1.0	6.0 6.1	9.0 9.5	1.0 1.0	9.5 10.0	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time $\overline{OE}$ to A	1.0 1.0	5.9 5.4	9.5 9.0	1.0 1.0	10.0 9.5	1.0 1.0	6.4 5.8	10.0 9.0	1.0 1.0	10.5 9.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to B	1.0 1.0	4.0 3.8	8.0 7.5	1.0 1.0	8.5 8.0	1.0 1.0	6.3 4.5	9.5 8.5	1.0 1.0	10.0 8.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to A	1.0 1.0	4.6 3.1	9.5 6.5	1.0 1.0	10.0 7.0	1.0 1.0	5.2 3.4	9.5 6.5	1.0 1.0	10.0 7.0	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew, (Note 8) Data to Output		1.0	1.5		1.5		1.0	1.5		1.5	ns

6. Typical values at V<sub>CCA</sub> = 3.3 V, V<sub>CCB</sub> = 5.0 V at 25 °C.

7. Typical values at V<sub>CCA</sub> = 3.3 V, V<sub>CCB</sub> = 3.3 V at 25 °C.

8. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

## CAPACITANCE

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}$	4.5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CCA} = 3.3 \text{ V}; V_{CCB} = 5.0 \text{ V}$	10	pF
$C_{PD}$	Power Dissipation Capacitance (Measured at 10 MHz)	A→B B→A $V_{CCB} = 5.0 \text{ V}$ $V_{CCA} = 3.3 \text{ V}$	50 40	pF

## Power Up Considerations

To insure the system does not experience unnecessary  $I_{CC}$  current draw, bus contention, or oscillations during power up, the following guidelines should be adhered to (refer to Table 1):

- Power up the control side of the device first. This is the  $V_{CCA}$  side.
- $\overline{OE}$  should ramp with or ahead of  $V_{CCA}$ . This will help guard against bus contention.
- The Transmit/Receive control pin ( $T/\overline{R}$ ) should ramp with  $V_{CCA}$ , this will ensure that the A Port data pins are

configured as inputs. With  $V_{CCA}$  receiving power first, the A I/O Port should be configured as inputs to help guard against bus contention and oscillations.

- A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

Table 1. Low Voltage Translator Power Up Sequencing Table

Device Type	$V_{CCA}$	$V_{CCB}$	$T/\overline{R}$	$\overline{OE}$	A Side I/O	B Side I/O	Floatable Pin Allowed
74LVXC3245	3 V (power up 1st)	3 V to 5.5 V configurable	ramp with $V_{CCA}$	ramp with $V_{CCA}$	logic 0 V or $V_{CCA}$	outputs	yes, $V_{CCB}$ and B I/O's w/ $\overline{OE}$ HIGH

Please reference Application Note [AN-5001](#) for more detailed information on using onsemi's LVX Low Voltage Dual Supply CMOS Translating Transceivers.



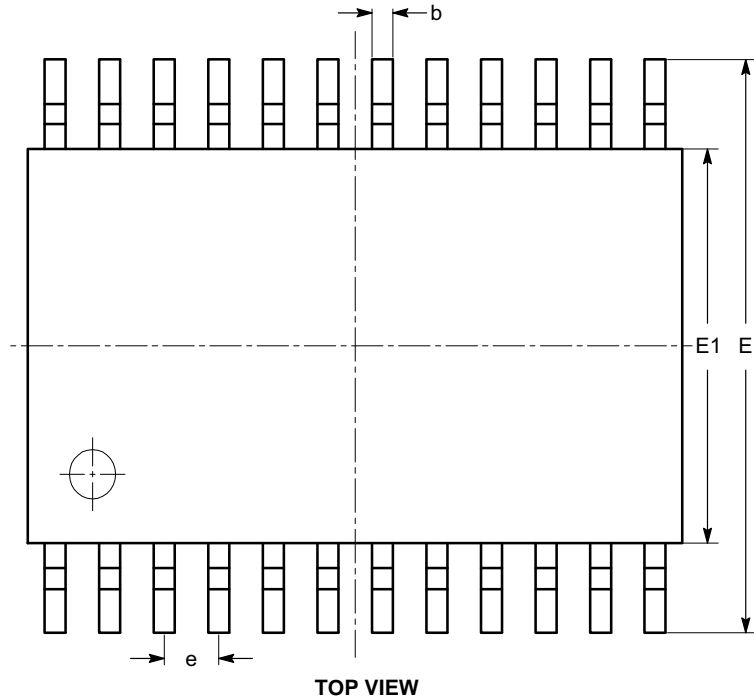
**REVISION HISTORY**

Revision	Description of Changes	Date
2	Converted the Data Sheet to <b>onsemi</b> format.	9/16/2025

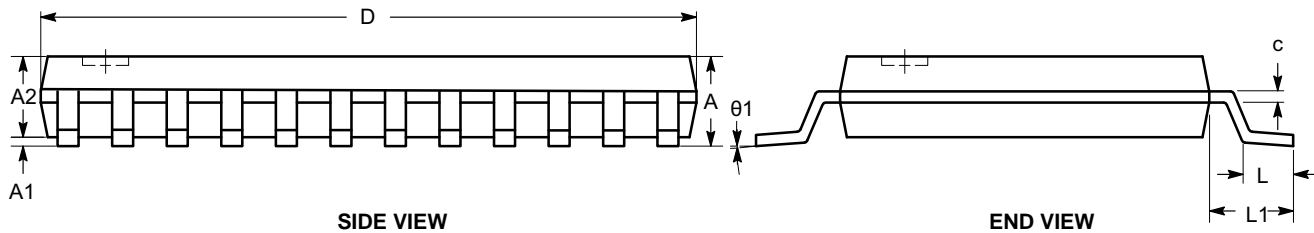
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

**TSSOP24, 4.4x7.8**  
CASE 948AR  
ISSUE A

DATE 17 MAR 2009



SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.50	0.60	0.70
L1	1.00 REF		
$\theta$	0°		8°



**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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