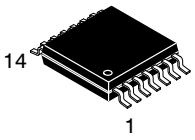
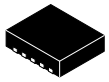
Low Voltage Quad Buffer with 5 V Tolerant Inputs and Outputs

74LCX126



TSSOP-14 WB
CASE 948G



QFN14, 3.0X2.5, 0.5P
CASE 510CB

General Description

The LCX126 contains four independent non-inverting buffers with 3-STATE outputs. Each output is disabled when the associated output-enable (OE) input is LOW. The inputs tolerate voltages up to 7 V allowing the interface of 5 V systems to 3 V systems.

The 74LCX126 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5 V Tolerant Inputs and Outputs
- 2.3 V – 3.6 V V_{CC} Specifications Provided
- 5.5 ns t_{PD} max (V_{CC} = 3.3 V), 10 μA I_{CC} max.
- Power Down High Impedance Inputs and Outputs
- Supports Live Insertion / Withdrawal*
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Proprietary Noise / EMI Reduction Circuitry
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >100 V
- Leadless DQFN Package
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

* To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

MARKING DIAGRAM

LCX126	= Specific Device Code
L	= Wafer Lot
Y	= Year
WW	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

CONNECTION DIAGRAMS

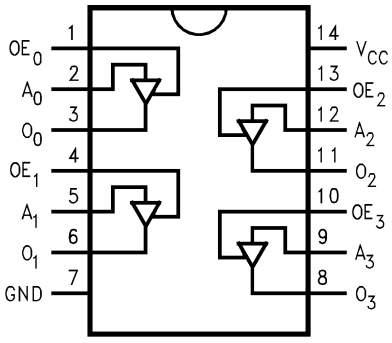
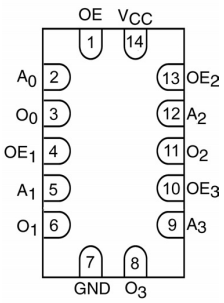
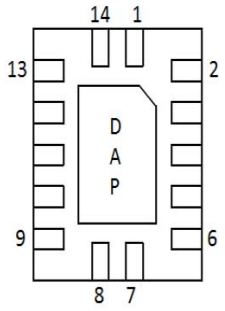


Figure 1. Pin Assignments for SOIC, SOP and TSSOP



(Top Through View)



(Bottom View)

Figure 2. Pad Assignments for DQFN

TRUTH TABLE

Inputs		Output
OE_n	**A_n**	**O_n**
H	L	L
H	H	H
L	X	Z

NOTES:
H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

LOGIC SYMBOL

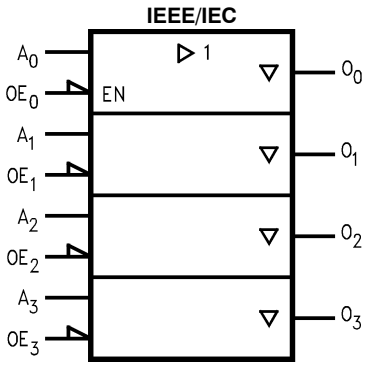


Figure 3. IEEE/IEC

PIN DESCRIPTION

Pin Names	Description
A_n	Inputs
OE_n	Output Enable Inputs
O_n	Outputs
DAP	No Connect

NOTE: DAP (Die Attach Pad)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)		−0.5 to +6.5	V
V_O	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} +6.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC-14 QFN14 TSSOP-14	116 130 150	°C/W
P_D	Power Dissipation in Still Air at 125 °C	SOIC-14 QFN14 TSSOP-14	1077 962 833	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	4000 2000	V
$I_{\_latchup}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS (Note 5)

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH} / I_{OL}	Out put Current	V_{CC} = 3.0 V – 3.6 V		±24	mA
		V_{CC} = 2.7 V – 3.0 V		±12	
		V_{CC} = 2.3 V – 2.7 V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8 V –2.0 V, V_{CC} = 3.0 V		0	10	ns / V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = −40 °C to +85 °C		Unit
				Min	Max	
V_{IH}	HIGH Level Input Voltage	2.3 – 2.7		1.7		V
		2.7 – 3.6		2.0		
V_{IL}	LOW Level Input Voltage	2.3 – 2.7			0.7	V
		2.7 – 3.6			0.8	
V_{OH}	HIGH Level Output Voltage	2.3 – 3.6	I_{OH} = −100 μA	V_{CC} −0.2		V
		2.3	I_{OH} = −8 mA	1.8		
		2.7	I_{OH} = −12 mA	2.2		
		3.0	I_{OH} = −18 mA	2.4		
			I_{OH} = −24 mA	2.2		
V_{OL}	LOW Level Output Voltage	2.3 – 3.6	I_{OL} = 100 μA		0.2	V
		2.3	I_{OL} = 8 mA		0.6	
		2.7	I_{OL} = 12 mA		0.4	
		3.0	I_{OL} = 16 mA		0.4	
			I_{OL} = 24 mA		0.55	
I_I	Input Leakage Current	2.3 – 3.6	0 ≤ V_I ≤ 5.5 V		±5.0	μA
I_{OZ}	3-STATE Output Leakage	2.3 – 3.6	0 ≤ V_I ≤ 5.5 V, V_I = V_{IH} or V_{IL}		±5.0	μA
I_{OFF}	Power−-Off Leakage Current	0	V_I or V_O = 5.5 V		10	μA
I_{CC}	Quiescent Supply Current	2.3 – 3.6	V_I = V_{CC} or GND		10	
			3.6 V ≤ V_I, V_O ≤ 5.5 V (Note 5)		±10	
ΔI_{CC}	Increase in I_{CC} per Input	2.3 – 3.6	V_{IH} = V_{CC} − 0.6 V		500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Outputs disabled or 3-STATE only.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = −40 °C to +85 °C, R_L = 500 Ω						Unit
		V_{CC} = 3.3 V ±0.3 V, C_L = 50 pF		V_{CC} = 2.7 V, C_L = 50 pF		V_{CC} = 2.5 V ±0.2 V, C_L = 30 pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay	1.5	5.5	1.5	6.0	1.5	6.6	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.5	6.0	1.5	7.0	1.5	7.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.5	5.5	1.5	6.5	1.5	6.6	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 7)		1.0					ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25 °C Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	0.6	
V_{OLV}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	−0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	−0.6	

CAPACITANCE

Symbol	Parameter	Conditions	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25.0	pF

AC LOADING AND WAVEFORMS (Generic for LCX Family)

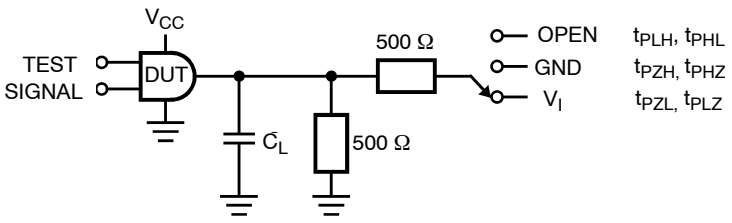
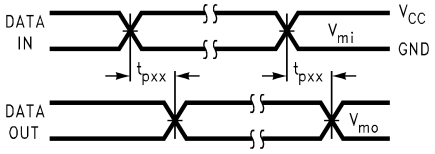


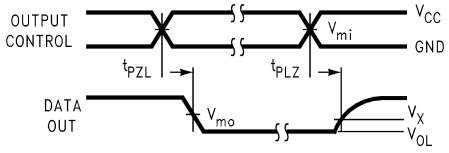
Table 1. TEST CIRCUIT TABLE

Test	Switch Position
t_{PLH} ,t_{PHL}	Open
t_{PZL} ,t_{PLZ}	6 V at V_{CC} = 3.3 ±0.3 V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2 V
t_{PZH} / t_{PHZ}	GND

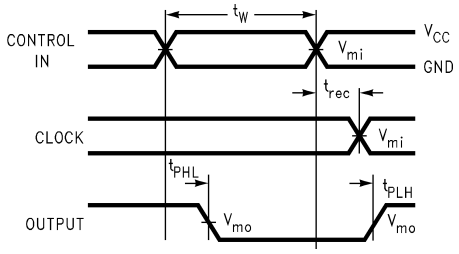
Figure 4. Test Circuit (C_L Includes Probe and Jig Capacitance)



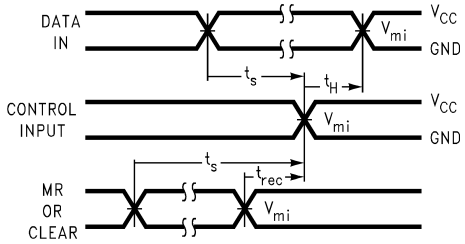
WAVEFORM FOR INVERTING AND NON-INVERTING FUNCTIONS



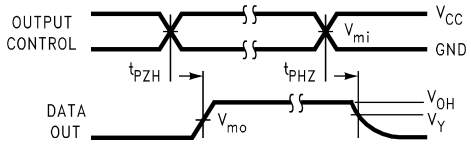
3-STATE OUTPUT HIGH ENABLE AND DISABLE TIMES FOR LOGIC



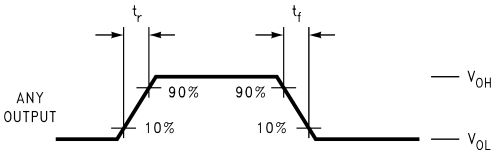
PROPAGATION DELAY. PULSE WIDTH AND t_{rec} WAVEFORMS



SETUP TIME, HOLD TIME AND RECOVERY TIME FOR LOGIC



3-STATE OUTPUT LOW ENABLE AND DISABLE TIMES FOR LOGIC



T_{rise} AND T_{fall}

Figure 5. Waveforms (Input Characteristics; f =1 MHz, t_r = t_f = 3 ns)

Table 2. SWITCHING WAVEFORMS TABLE

Symbol	V_{CC}		
	3.3 V ±0.3 V	2.7 V	2.5 V ±0.2 V
V_{mi}	1.5 V	1.5 V	V_{CC}/2
V_{mo}	1.5 V	1.5 V	V_{CC}/2
V_x	V_{OL} +0.3 V	V_{OL} +0.3 V	V_{OL} +0.15 V
V_y	V_{OH} −0.3 V	V_{OH} −0.3 V	V_{OH} −0.15 V

SCHEMATIC DIAGRAM (Generic for LCX Family)

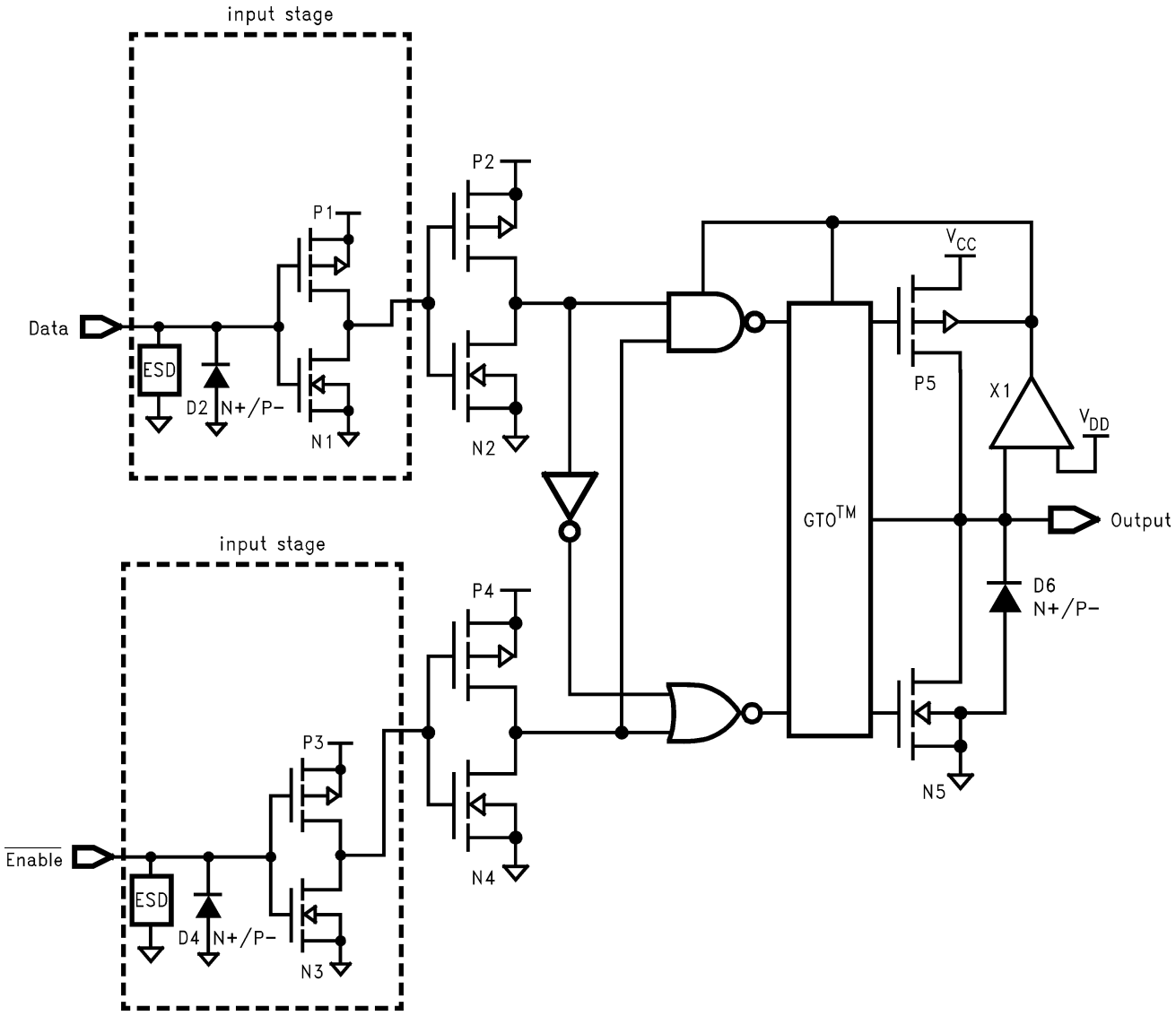


Figure 6. Schematic Diagram

ORDERING INFORMATION

Product Number	Package	Marking	Shipping†
74LCX126BQX	QFN-14 (Pb-Free/Halide Free)	LCX126	3000 / Tape and Reel
74LCX126MTCX	TSSOP-14 (Pb-Free/Halide Free)	LCX 126	2500 / Tape and Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* DQFN package available in Tape and Reel only.
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number

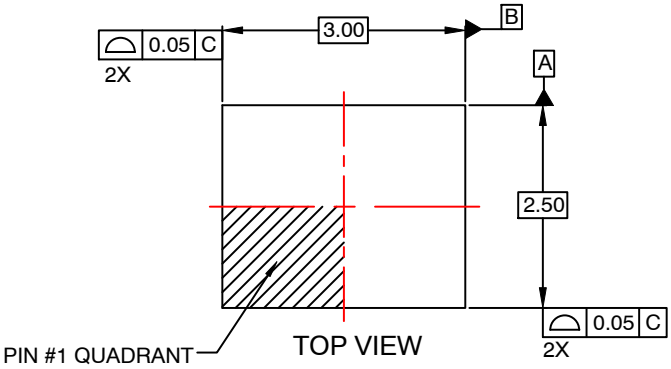
REVISION HISTORY

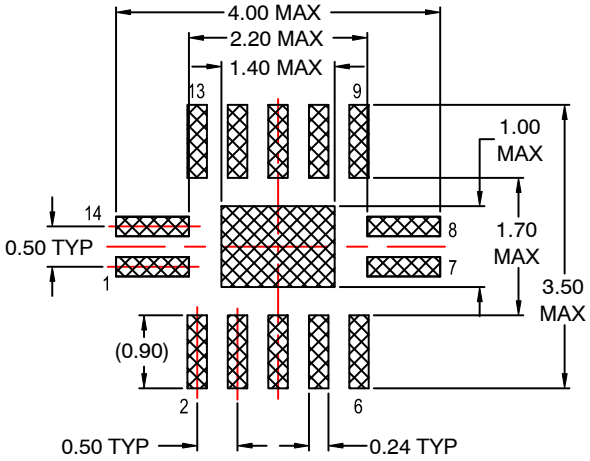
Revision	Description of Changes	Date
2	Converted the Data Sheet to **onsemi** format.	5/12/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

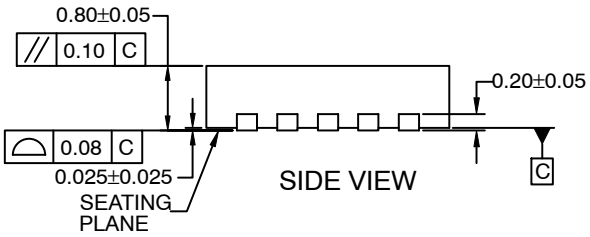
QFN14 3.0x2.5, 0.5P
CASE 510CB
ISSUE O

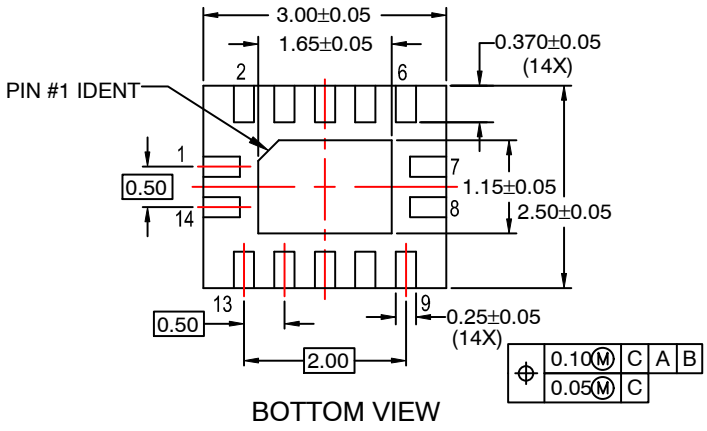
DATE 31 AUG 2016





RECOMMENDED LAND PATTERN





NOTES:

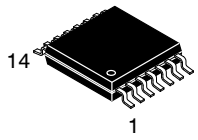
A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

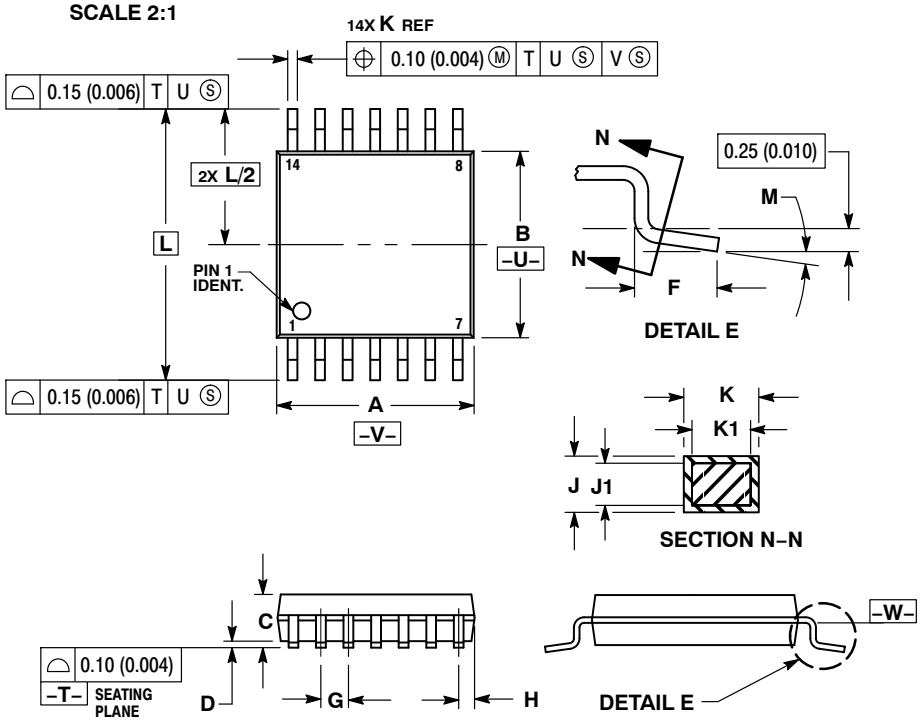
DOCUMENT NUMBER:	**98AON13643G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**QFN14 3.0X2.5, 0.5P**	**PAGE 1 OF 1**



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

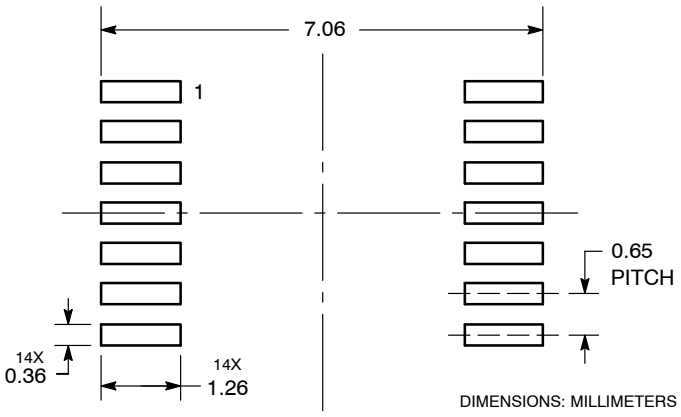
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

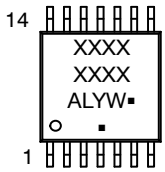
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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onsemi Website: www.onsemi.com

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