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Enable Pin Operation and Functions of eFuses

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APPLICATION NOTE

Introduction

ON Semiconductor electronic fuses (eFuses) are analog integrated circuits that are used to protect circuits operating from 3.3, 5, or 12 V DC supplies. They have numerous protection functionalities such as overvoltage clamping, current limiting, thermal shutdown, and a controlled output voltage slew rate. They are available in thermal latching or thermal auto-retry configurations.

A key feature of the eFuse family is the enable pin. This application note describes the features of the enable pin and provides guidance to ensure its proper use. The enable pin of any eFuse may be left floating if the application does not require that it be controlled and does not require thermal fault notification. For a basic explanation of the operation of an eFuse, please refer to the datasheets for the NIS5112, NIS5135, NIS5132, and NIS5232.

The operation and functionality of the enable pin depends on the particular eFuse being considered. Table 1 provides information regarding the key differences between the devices in the ON Semiconductor eFuse family.

Table 1. THE KEY DIFFERENCES BETWEEN THE FUNCTIONALITY OF THE ENABLE PIN FOR ON SEMICONDUCTOR eFUSES

| Device	Startup Blanking	Timer Capability	Logic Levels
NIS5112	No	Yes	Low or High
NIS5135, NIS5132, NIS5232	Yes*	No	Low, Mid, or High

*The NIS5132MN3 does not have a startup blanking circuit.

NIS5112 Enable/Timer Pin

The enable pin of the NIS5112 may be in either a high or a low state. Figure 1 provides a simplified schematic of the enable circuit. The voltage at the enable pin is compared with a nominal 2.5 V internal reference voltage. If the voltage at the enable pin is greater than this reference voltage, the eFuse output is enabled. To force the enable pin voltage low, it is recommended that a transistor is connected as shown in Figure 1. An internal current source of about 80 μA serves as the pull-up device.

The NIS5112 has a typical thermal shutdown temperature of 135°C. After a thermal shutdown, a thermal auto-retry NIS5112 returns power to the load after its internal temperature drops below 95°C (typical). By contrast, a thermal latching NIS5112 remains in a disabled state with its enable pin high after thermal shutdown. Resetting may be done by cycling the power to the eFuse or by forcing the enable pin into the low state and then releasing the pin.
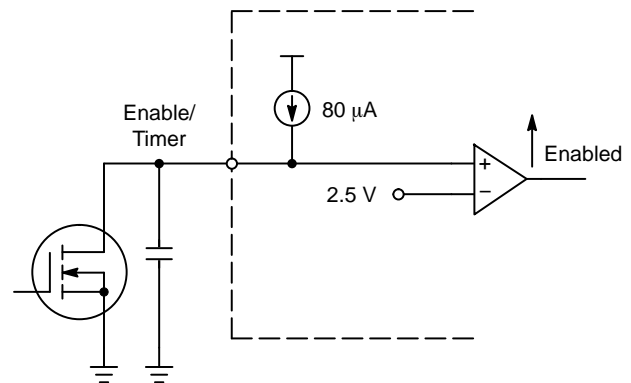
Figure 1. Simplified Schematic of the Enable Circuitry for the NIS5112. It Shows a Transistor and a Timing Capacitor Connected

The NIS5112 enable pin may also be used as a timer pin by adding a capacitor between it and ground as shown in Figure 1. Such a capacitor provides a delay after power is applied to the eFuse or after a transistor on the enable pin transitions from on to off. The timer circuit uses the internal 80 μA current source shown in Figure 1 to charge the capacitor. The eFuse does not turn on until the current source charges the capacitor to the high state of the enable pin. The added delay is given by:

$$\text{Delay} = \frac{(V_{High})\,(C)}{I_{Source}} \qquad \text{(eq. 1)}$$

Where V_{High} is the voltage to enter the high state on the enable pin, C is the value of the capacitor between the enable pin and ground in farads, and I_{Source} is the eFuse's internal current source on the enable pin. Values for the enable voltage and charging current for different conditions are provided in the NIS5112 datasheet. For example, at 25°C, V_{High} has a minimum value of 2.5 V and I_{Source} has a typical value of 83 μA. Therefore, to achieve a 25 ms delay, the following calculation may be made:

$$25 \times 10^{-3} = \frac{(2.5)\,(C)}{83 \times 10^{-6}}$$

$$C = 0.83\ \mu F \qquad \text{(eq. 2)}$$

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NIS5135, NIS5132 and NIS5232 Enable/Fault Pin

The enable pin of the NIS5135, NIS5132, and NIS5232 has three different logic levels. Table 2 provides a summary of these logic levels. In contrast to traditional input/output buffers, there is no circuitry which isolates the input and output circuits from each other and the enable pin's input and output functions operate simultaneously.

Table 2. TRI-STATE LEVELS OF THE ENABLE PIN OF THE NIS5135, NIS5132 AND NIS5232

Level	How Enable Pin is Placed in Logic State	State of eFuse
Low	Held low by startup blanking circuit for fixed time after power has been applied to V_{CC}*	Output disabled, thermal latch circuitry reset
	Held low by external circuit	Output disabled, thermal latch circuitry reset
Mid	Forced to level by internal circuitry due to a thermal fault condition	Output disabled, thermal shutdown
	Held in state by the enable pin of another eFuse	Output disabled
High	Pulled high by internal circuitry	Output enabled

*The NIS5132MN3 does not have startup blanking circuitry.

A simplified schematic of the enable circuit is shown in Figure 2. The output of the enable circuit is the enable shutdown (SD) signal. A high enable SD forces the eFuse to shut down, removing power from the load. A low enable SD allows normal operation. The enable SD comparator generates the enable SD signal based on an internally generated nominal 2.64 V internal reference and the enable voltage as shown in Figure 2. Under normal conditions and with no external input, the enable pin is held high by a 12 μA internal current source and the enable SD signal is low.


(*MN1 and MN2 Versions)
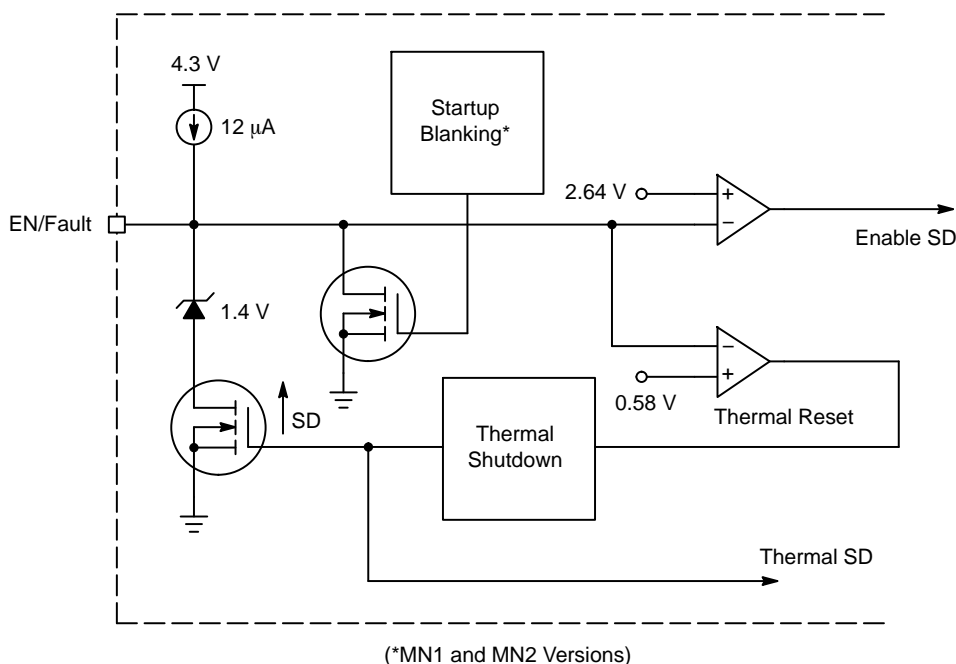
Figure 2. Simplified Schematic of the Enable Circuitry for the NIS5135, NIS5132 and NIS5232

An enable SD high is generated by the enable SD comparator any time the enable voltage goes below the nominal 2.64 V threshold for a high state. As shown in Table 2, there are four basic ways the enable pin can be forced or held below the high state. These are the startup blanking circuit, an external transistor connected to the enable pin, the internal thermal shutdown circuit, and the enable pin of another eFuse.

When power is first applied to the eFuse, a startup blanking circuit holds the enable pin to ground for a fixed time (typically much less than 100 μs) by turning on the startup blanking transistor in Figure 2. After the startup time, the startup blanking transistor is turned off and the enable pin voltage is pulled to a high state.

The enable pin may be forced to the low or mid state with an external circuit to disable the eFuse. A low state may be forced by connecting a transistor as shown in Figure 3. The enable pin should not be forced high. For example, it should not be connected to V_{CC} or directly to standard logic circuits with active circuitry. Furthermore, it is not recommended to connect a capacitor from the enable pin to ground for timing purposes.
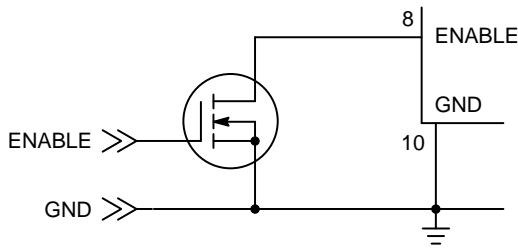
Figure 3. Circuit for Forcing a Low State on the Enable Pin

Activation of the thermal shutdown circuit provides a high signal to the internal thermal shutdown transistor to pull the enable pin out of the high state. A 1.4 V diode drop element in series with the internal thermal shutdown transistor

results in the enable pin being pulled to the intermediate or mid state. Since the mid state is below the trip point for the enable SD comparator, a high enable SD is generated and the eFuse output is disabled.

An alternate method of controlling the state of the enable pin is to tie the enable pins of multiple eFuses together. The maximum fanout (the total number of eFuses that can be connected to the pin for simultaneous shutdown) is three. A common application is a system with 5 and 12 V rails using the NIS5135 and the NIS5232 with the enable pins connected to each other as shown in Figure 4. With multiple enable pins tied together a thermal fault on one eFuse forces a mid level on all of the eFuses. This ensures full shutdown of a system under a thermal fault condition on any of the eFuses.
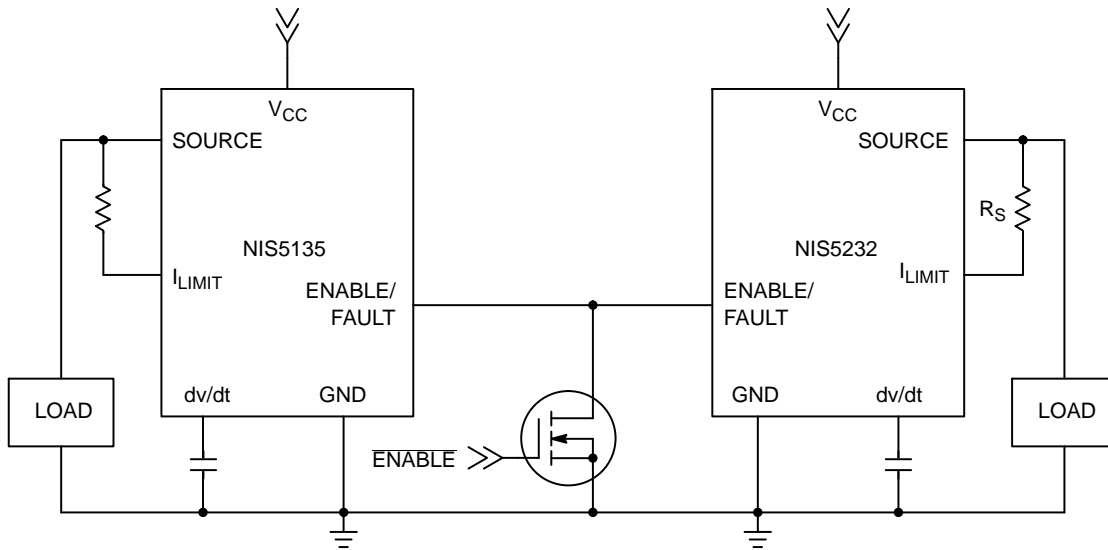
Figure 4. Example of Two eFuses with their Enable Pins Connected together for a Common Thermal Shutdown. The Transistor Connected to the Enable Pin may be used to Hold the Enable Pin Low or to Reset the eFuses after Thermal Latching

The functional distinction between the mid and low levels is only significant for thermal latching eFuses. After a thermal shutdown, an auto-retry NIS5135 or NIS5132 returns power to the load after the internal temperature of the eFuse drops below 130°C (typical). The enable pin of the thermal latching versions is brought to the mid state after thermal shutdown. The eFuse may be reset by cycling the

power to the V_{CC} pin or alternatively by forcing the enable pin into the low state and then releasing the pin. The function of the reset circuit may be seen in Figure 2. If the logic level on the enable pin is changed from the mid level to the low level, the output of the thermal reset comparator goes from low to high, signaling the thermal shutdown circuit to reset.

Summary

The enable pin of ON Semiconductor eFuses provides a number of features. With all eFuses, a transistor may be used to force the pin low to disable the output. In addition, it may be left floating if no control of the enable pin is required. With thermal latching eFuses, it may be brought low and then allowed to go high to reset the device.

The enable pin of the NIS5135, NIS5132, and NIS5232 has a middle logic state and their enable pins may be connected to allow a common thermal shutdown. A capacitor may be connected on the NIS5112 to serve as a startup timer, while the NIS5135, NIS5132MN1, NIS5132MN2, and NIS5232 have an internal startup blanking circuit and should not have a capacitor connected from the enable pin to ground.