Preconfigured DSP System for Hearing Aids

RHYTHM SB3230

Description

The RHYTHM™ SB3230 hybrid from ON Semiconductor is a trimmer−configurable DSP system based on a four−channel compression circuit featuring adaptive feedback cancellation and adaptive noise reduction.

Based on a phase cancellation method, SB3230's adaptive feedback reduction algorithm provides added stable gain to enable extra gain and user comfort. It features rapid adjustment for dynamic feedback situations and resistance to tonal inputs.

The SB3230's Adaptive Noise Reduction monitors noise levels independently in 64 individual bands and employs advanced psychoacoustic models to provide user comfort.

In addition to these adaptive algorithms, SB3230 also supports the following features: up to four channel WDRC, low−distortion compression limiting, cross fading between audio paths for click−free memory changes, eight−band graphic equalizer, eight configurable generic biquad filters, programming speed enhancements, in−channel squelch to attenuate microphone and circuit noise in quiet environments, optional peak clipping, flexible compression adjustments, volume control, rocker switch, noise generation for Tinnitus treatment, and industry−leading security features to avoid cloning and software piracy.

A trimmer interface supports manual circuit configuration. It continuously monitors trimmer positions and translates them into the hearing−aid parameters of choice. A Serial Data or I^2C Interface provides full programmability at the factory and in the field.

SB3230 hybrid contains a 256 kbit EEPROM intended for programmable and trimmer based devices.

Features

- Adaptive Noise Reduction
- Adaptive Feedback Cancellation
- WDRC Compression with Choice of 1, 2 or 4 Channels of Compression
- Auto Telecoil with Programmable Delay
- EVOKE Acoustic Indicators
- Noise Generator for Tinnitus Treatment or In−situ Audiometry
- Frequency Response Shaping with Graphic EQ
- Trimmer Compatibility – Four Three−Terminal Trimmers with Configurable Assignments of Control Parameters
- I^2C and SDA Programming
- Rocker Switch Support for Memory Change and/or Volume Control Adjustment
- Analog or Digital Volume Control with Programmable Range

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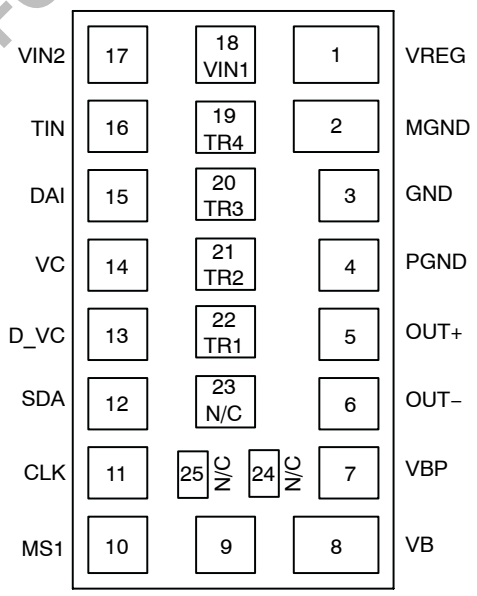
25 PAD HYBRID CASE 127DN

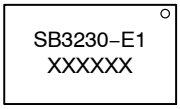
PAD CONNECTION



MS2

(Bottom View)

MARKING DIAGRAM



SB3230 = Specific Device Code
E1 = RoHS Compliant Hybrid
XXXXXX = Work Order Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

- High Quality 20−bit Audio Processing
- High Power/High Gain Capability
- SOUNDFIT Fitting Software
- Configurable Low Battery Indicator
- Eight Biquadratic Filters
- 16 kHz or 8 kHz Bandwidth
- Four Fully Configurable Memories with Audible Memory Change Indicator
- 96 dB Input Dynamic Range with Headroom Extension
- 128−bit Fingerprint Security System and Other Security Features to Protect against Device Cloning and Software Piracy
- High Fidelity Audio CODEC
- Soft Acoustic Fade between Memory Changes
- Drives Zero−Bias Two−Terminal Receivers
- E1 RoHS−compliant Hybrid
- Hybrid Typical Dimensions: 0.220 x 0.125 x 0.060 in (5.59 x 3.18 x 1.52 mm)

BLOCK DIAGRAM

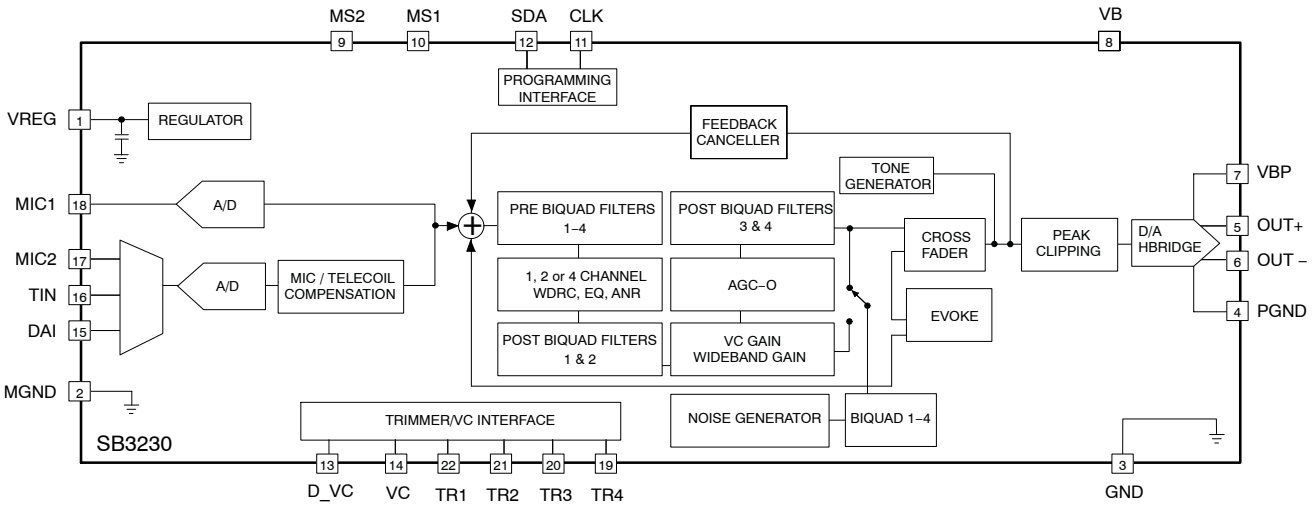


Figure 1. Hybrid Block Diagram

SPECIFICATIONS

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Operating Temperature Range	0 to +40	°C
Storage Temperature Range	−20 to +70	°C
Absolute Maximum Power Dissipation	25	mW
Maximum Operating Supply Voltage	1.65	VDC
Absolute Maximum Supply Voltage	1.8	VDC

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

WARNING: Electrostatic Sensitive Device − Do not open packages or handle except at a static−free workstation.

WARNING: Moisture Sensitive Device − RoHS Compliant; Level 3 MSL. Do not open packages except under controlled conditions.

Table 2. ELECTRICAL CHARACTERISTICS (Supply Voltage V_B = 1.25 V; Temperature = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Hybrid Current	I_{AMP}	All Functions, 32 kHz Sampling Rate	−	660	−	μA
		All Functions, 16 kHz Sampling Rate	−	490	−	
Minimum Operating Supply Voltage	V_{BOFF}	Ramp Down, Audio Path	0.93	0.95	0.97	V
		Ramp Down, Control Logic	0.77	0.80	0.83	
Supply Voltage Turn On Threshold	V_{BON}	Ramp Up	1.06	1.10	1.16	V
EEPROM Burn Cycles	−	−	100 k	−	−	cycles
Low Frequency System Limit	−	−	−	125	−	Hz
High Frequency System Limit	−	−	−	16	−	kHz
Total Harmonic Distortion	THD	V_{IN} = −40 dBV	−	−	1	%
THD at Maximum Input	THD_M	V_{IN} = −15 dBV, Headroom Extension − ON	−	−	3	%
Clock Frequency	f_{CLK}	−	3.973	4.096	4.218	MHz
Audio Path Latency	−	8 kHz Bandwidth	−	4.2	−	ms
	−	16 kHz Bandwidth	−	4.0	−	
System Power On Time (Note 1)	−	SB3230	−	1600	−	ms
REGULATOR						
Regulator Voltage	V_{REG}	−	0.87	0.90	0.93	V
System PSRR	$PSRR_{SYS}$	1 kHz, Input Referred, Headroom Extension Enabled	−	70	−	dB
INPUT						
Input Referred Noise	IRN	Bandwidth 100 Hz − 8 kHz, Headroom Extension on	−	−108	−106	dBV
Input Impedance	Z_{IN}	1 kHz	−	3	−	MΩ
Anti−aliasing Filter Rejection	−	$f = f_{CLK/2}$ − 8 kHz, V_{IN} = −40 dBV	−	80	−	dB
Crosstalk	−	Between both A/D and Mux	−	60	−	dB
Maximum Input Level	−	−	−15	−13	−	dBV
Analogue Input Voltage Range	V_{AN_IN}	V_{IN1}, V_{IN2}, AI	0	−	800	mV
	V_{AN_TIN}	T_{IN}	−100	−	800	
Input Dynamic Range	−	Headroom Extension − ON Bandwidth 100 Hz − 8 kHz	−	95	96	dB

Table 2. ELECTRICAL CHARACTERISTICS (Supply Voltage V_B = 1.25 V; Temperature = 25°C) (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT						
D/A Dynamic Range	–	100 Hz – 8 kHz	–	88	–	dB
Output Impedance	Z_{OUT}	–	–	10	13	Ω
CONTROL A/D						
Resolution (Monotonic)	–	–	7	–	–	bits
Zero Scale Level	–	–	–	0	–	V
Full Scale Level	–	–	–	V_{REG}	–	V
VOLUME CONTROL						
Volume Control Resistance	R_{VC}	Three−terminal Connection	100	–	360	kΩ
Volume Control Range	–	–	–	–	42	dB
PC_SDA INPUT						
Logic 0 Voltage	–	–	0	–	0.3	V
Logic 1 Voltage	–	–	1	–	1.25	V
PC_SDA OUTPUT						
Stand−by Pull Up Current	–	Creftrim = 6	3	5	6.5	μA
Sync Pull Up Current	–	Creftrim = 6	748	880	1020	μA
Max Sync Pull Up Current	–	Creftrim = 15	–	1380	–	μA
Min Sync Pull Up Current	–	Creftrim = 0	–	550	–	μA
Logic 0 Current (Pull Down)	–	Creftrim = 6	374	440	506	μA
Logic 1 Current (Pull Up)	–	Creftrim = 6	374	440	506	μA
Synchronization Time (Synchronization Pulse Width)	T_{SYNC}	Baud = 0	237	250	263	μs
		Baud = 1	118	125	132	
		Baud = 2	59	62.5	66	
		Baud = 3	29.76	31.25	32.81	
		Baud = 4	14.88	15.63	16.41	
		Baud = 5	7.44	7.81	8.20	
		Baud = 6	3.72	3.91	4.10	
		Baud = 7	1.86	1.95	2.05	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

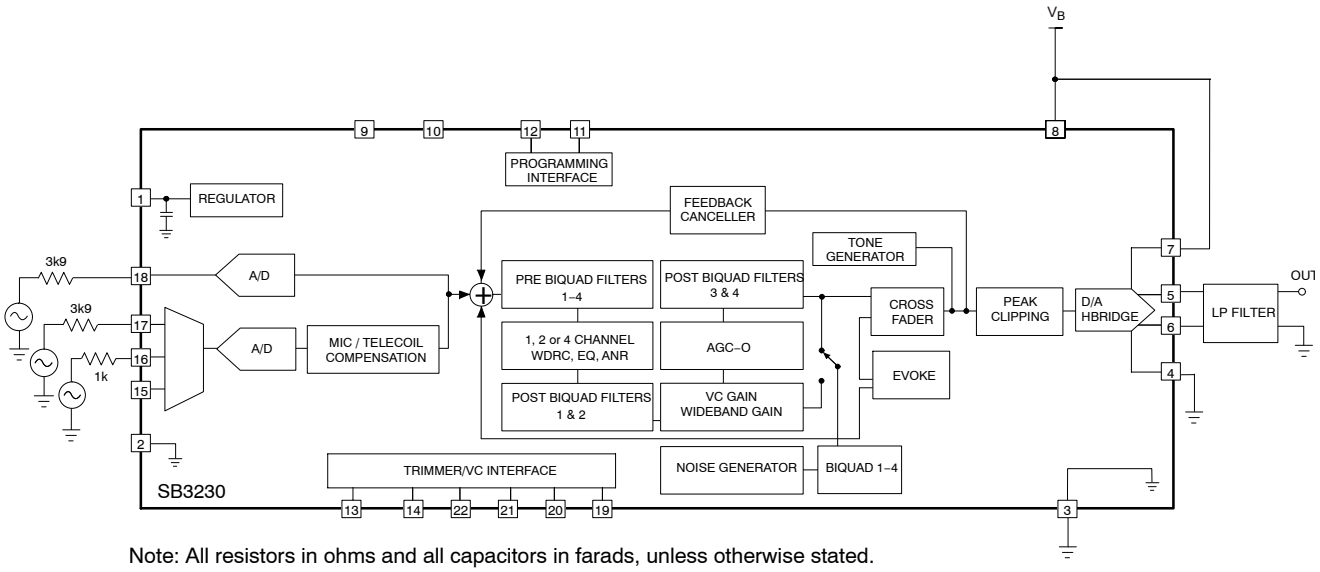
1. Times do not include additional programmable startup delay.

Table 3. I²C TIMING

Parameter	Symbol	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
Clock Frequency	f_{PC_CLK}	0	100	0	400	kHz
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated.	$t_{HD;STA}$	4.0	–	0.6	–	μsec
LOW Period of the PC_CLK Clock	t_{LOW}	4.7	–	–	–	μsec
HIGH Period of the PC_CLK Clock	t_{HIGH}	4.0	–	–	–	μsec
Set−up Time for a Repeated START Condition	$t_{SU;STA}$	4.7	–	–	–	μsec
Data Hold Time: for CBUS Compatible Masters for I²C−bus Devices	$t_{HD;DAT}$	 5.0 0 (Note 1)	 – 3.45 (Note 2)	 – 0 (Note 1)	 – 0.9 (Note 2)	μsec
Data Set−up Time	$t_{SU;DAT}$	250	–	100	–	nsec
Rise Time of Both PC_SDA and PC_CLK Signals	t_r	–	1000	20 + 0.1 C_b (Note 4)	300	nsec
Fall Time of Both PC_SDA and PC_CLK Signals	t_f	–	300	20 + 0.1 C_b (Note 4)	300	nsec
Set−up Time for STOP Condition	$t_{SU;STO}$	4.0	–	0.6	–	nsec
Bus Free Time between a STOP and START Condition	t_{BUF}	4.7	–	1.3	–	μsec
Output Fall Time from V_{IHmin} to V_{ILmax} with a Bus Capacitance from 10 pF to 400 pF	t_{of}	–	250	20 + 0.1 C_b (Note 4)	250	nsec
Pulse Width of Spikes which Must Be Suppressed by the Input Filter	t_{SP}	n/a	n/a	0	50	nsec
Capacitive Load for Each Bus Line	C_b	–	400	–	400	pF

1. A device must internally provide a hold time of at least 300 ns for the PC_SDA signal to bridge the undefined region of the falling edge of PC_CLK.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the PC_CLK signal.
3. A Fast−mode I²C−bus device can be used in a Standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ P250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the PC_CLK signal. If such a device does stretch the LOW period of the PC_CLK signal, it must output the next data bit to the PC_SDA line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I²C−bus specification) before the PC_CLK line is released.
4. C_b = total capacitance of one bus line in pF.

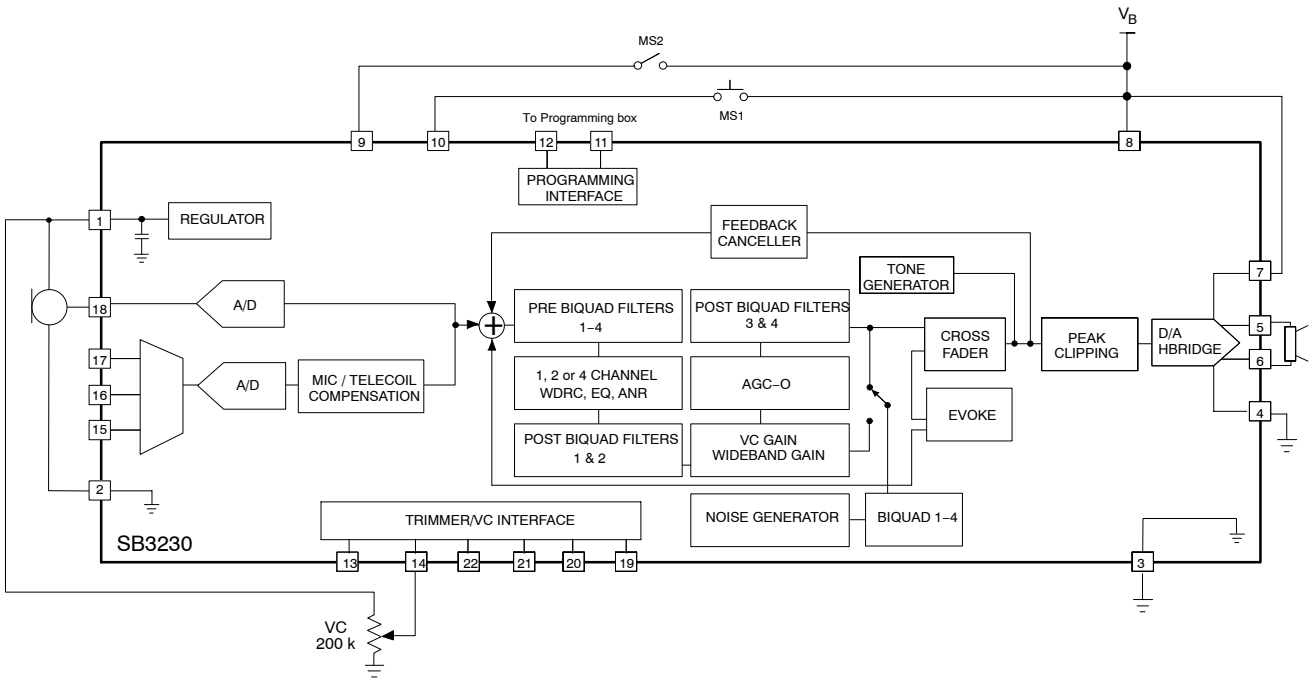
TYPICAL APPLICATIONS



Note: All resistors in ohms and all capacitors in farads, unless otherwise stated.

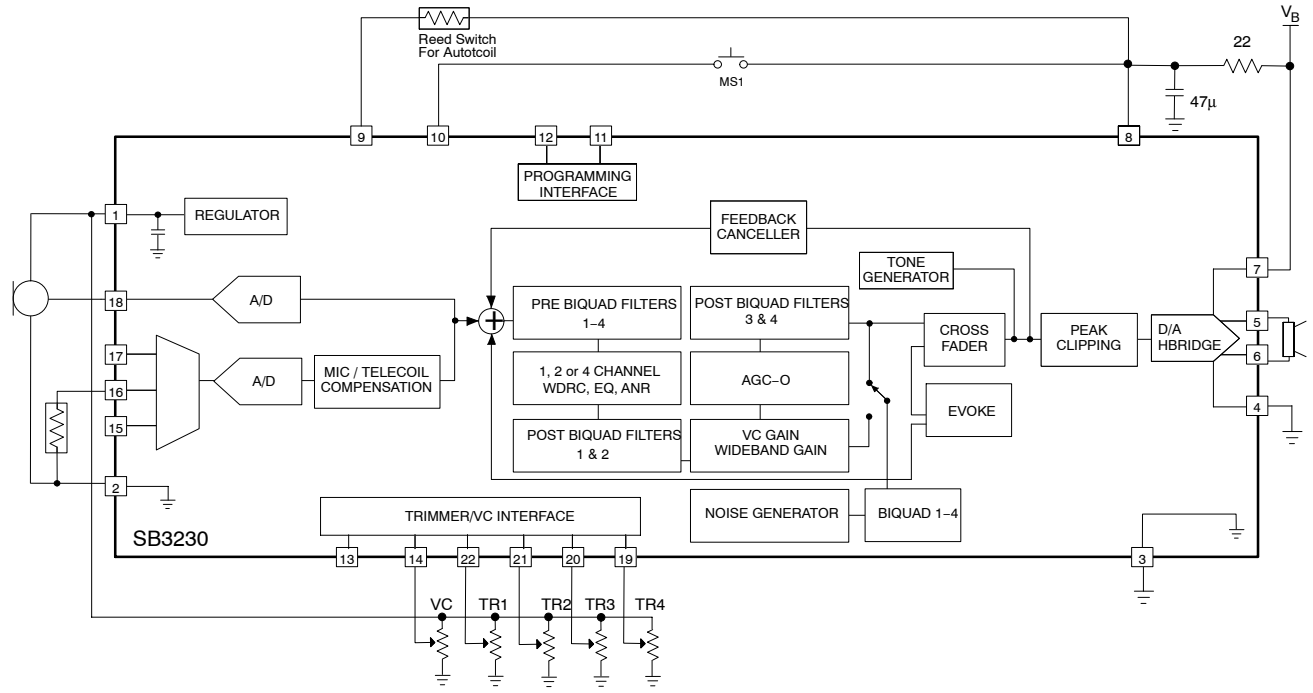
Figure 2. Test Circuit

TYPICAL APPLICATIONS (continued)



Note: All resistors in ohms and all capacitors in farads, unless otherwise stated.

Figure 3. Typical Programmable Application Circuit



Note: All resistors in ohms and all capacitors in farads, unless otherwise stated.

Figure 4. Typical Trimmer Application Circuit

SB3230 OVERVIEW

SB3230 is a DSP system implemented on ON Semiconductor's Wolverine hardware platform. Wolverine is the hearing industry's first 90 nm Silicon−on−Chip platform enabling design of highly−efficient and flexible hearing aid solutions. The device is packaged for easy integration into a wide range of applications from CIC to BTE. SB3230 can be used as a programmable or trimmer adjustable device. It may be configured as one, two or four channels with linear or WDRC processing. Configuration data stored in non−volatile memory defines hearing−aid parameters. SB3230 can be programmed via the SDA or I^2C programming interfaces.

The DSP core implements Adaptive Feedback Cancellation, Adaptive Noise Reduction, compression, wideband gain, and volume control. The Adaptive Feedback Canceller reduces acoustic feedback while offering robust performance against pure tones.

During trimmer mode operation, a low−speed A/D circuit monitors the positions of up to four manual trimmers and a VC potentiometer. Trimmer position changes are immediately interpreted and translated into new circuit parameter values, which are then used to update the signal path.

FUNCTIONAL BLOCK DESCRIPTION

A/D and D/A Converter

The system's A/D converter is a 2nd−order sigma−delta modulator operating at a 2.048 MHz sample rate.

The system's input is pre−conditioned with anti−alias filtering and a programmable gain pre−amplifier. The analog output is oversampled and modulated to produce a 1−bit pulse density modulated (PDM) data stream. The digital PDM data is then decimated down to pulse−code modulated (PCM) digital words at the system's sampling rate of 32 kHz.

The D/A is comprised of a digital 3rd−order sigma−delta modulator and an H−bridge. The modulator accepts PCM audio data from the DSP path and converts it into a 64−times oversampled, 1−bit PDM data stream, which is then supplied to the H−bridge. The H−bridge is a specialized CMOS output driver used to convert the 1−bit data stream into a low−impedance, differential output voltage waveform suitable for driving zero−biased hearing aid receivers.

Analog Inputs

SB3230 provides for up to four analog inputs, Microphone 1 (MIC1), Microphone 2 (MIC2), Telecoil (TCOIL) and Direct Audio Input (DAI) with the following configurable front end modes:

- 1 Mic Omni
- 1 Mic Omni (Rear channel only)
- DAI
- TCOIL
- 1 Mic Omni + TCOIL
- 1 Mic Omni + DAI

Attenuation can be applied to the input when mixing with either TCOIL or DAI inputs.

Channel Processing

Figure 5 represents the I/O characteristic of independent AGC channel processing. The I/O curve can be divided into four main regions:

- Low input level expansion (squelch) region
- Low input level linear region
- Compression region
- High input level linear region (return to linear)

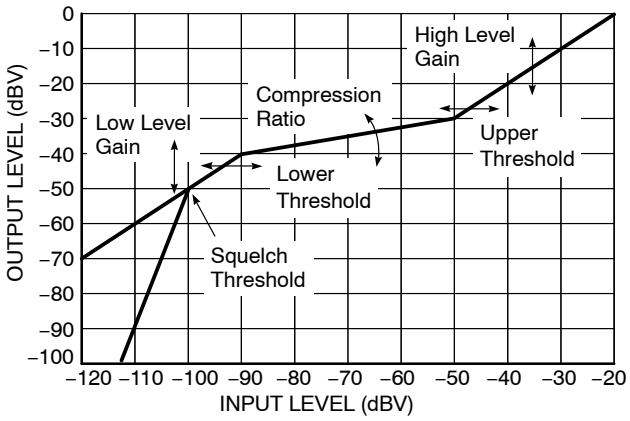


Figure 5. Independent Channel I/O Curve Flexibility

Channel I/O processing is specified by the Squelch threshold (SQUELCHTH) and any four of the following five parameters (only four of the five properties are independent):

- Low level gain (LLGAIN)
- Lower threshold (LTH)
- High level gain (HLGAIN)
- Upper threshold (UTH)
- Compression ratio (CR)

During the Parameter Map creation, constraints are applied to the compression parameters to ensure that the I/O characteristics are continuous. Parameter adjustments support two popular styles of compression ratio adjustment:

- The compression region of the I/O curve pivots about the upper threshold. As the compression ratio trimmer is adjusted, high−level gain remains constant while the low−level gain changes.

- The compression region of the I/O curve pivots about the lower threshold. Low−level gain remains constant as the compression ratio trimmer is adjusted.

The squelch region within each channel implements a low level noise reduction scheme (1:3 expansion) for listener comfort. This scheme operates in quiet listening environments (programmable threshold) to reduce the gain at very low levels.

Automatic Telecoil

The automatic telecoil feature in SB3230 is to be used with memory D programmed with the telecoil or MIC + TCOIL front end configuration. The feature enables the part to transition to memory D upon the closing of a switch connected to MS2. With the feature enabled and a reed switch connected to MS2, the static magnetic field of a telephone handset will close the switch whenever the handset is brought close to the device, causing the hybrid to change to memory D. The part will transition back to the initial memory once the switch is deemed opened after proper debouncing.

A debounce algorithm with a programmable debounce period is used to prevent needless switching in and out of memory D due to physical switch bounces when MS2 is configured for automatic telecoil. Upon detecting a close to open switch transition, the debounce algorithm monitors the switch status. The debounce algorithm switches the device out of memory D only once the switch signal has been continuously sampled open over the specified debounce period.

Adaptive Feedback Canceller

The Adaptive Feedback Canceller (AFC) reduces acoustic feedback by forming an estimate of the hearing aid feedback signal and then subtracting this estimate from the hearing aid input. The forward path of the hearing aid is not affected. Unlike adaptive notch filter approaches, SB3230's AFC does not reduce the hearing aid's gain. The AFC is based on a time−domain model of the feedback path.

The third−generation AFC (see Figure 6) allows for an increase in the stable gain (Note 1) of the hearing instrument while minimizing artefacts for music and tonal input signals. As with previous products, the feedback canceller provides completely automatic operation.

1. Added stable gain will vary based on hearing aid style and acoustic setup. Please refer to the Adaptive Feedback Cancellation Information note for more details.

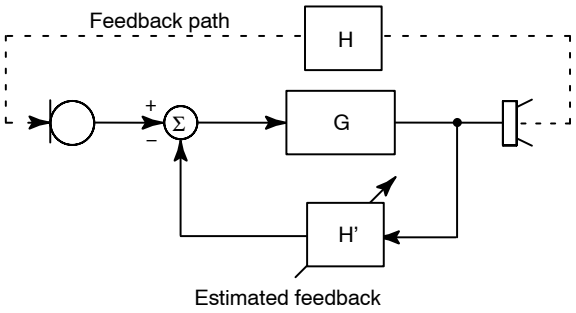


Figure 6. Adaptive Feedback Canceller (AFC) Block Diagram

Feedback Path Measurement Tool

The feedback path measurement tool uses the onboard feedback cancellation algorithm and noise generator to measure the acoustic feedback path of the device. The noise generator is used to create an acoustic output signal from the hearing aid, some of which leaks back to the microphone via the feedback path. The feedback canceller algorithm automatically calculates the feedback path impulse response by analyzing the input and output signals. Following a suitable adaptation period, the feedback canceller coefficients can be read out of the device and used as an estimate of the feedback−path impulse response.

Adaptive Noise Reduction

The noise reduction algorithm is built upon a high resolution 64−band filter bank (32 bands at 16 kHz sampling) enabling precise removal of noise. The algorithm monitors the signal and noise activities in these bands, and imposes a carefully calculated attenuation gain independently in each of the 64 bands.

The noise reduction gain applied to a given band is determined by a combination of three factors:

- Signal−to−Noise Ratio (SNR)
- Masking threshold
- Dynamics of the SNR per band

The SNR in each band determines the maximum amount of attenuation to be applied to the band − the poorer the SNR, the greater the amount of attenuation. Simultaneously, in each band, the masking threshold variations resulting from the energy in other adjacent bands is taken into account. Finally, the noise reduction gain is also adjusted to take advantage of the natural masking of 'noisy' bands by speech bands over time.

Based on this approach, only enough attenuation is applied to bring the energy in each ‘noisy’ band to just below the masking threshold. This prevents excessive amounts of attenuation from being applied and thereby reduces unwanted artifacts and audio distortion. The Noise Reduction algorithm efficiently removes a wide variety of types of noise, while retaining natural speech quality and level. The level of noise reduction (aggressiveness) is configurable to 3, 6, 9 and 12 dB of reduction.

Volume Control, Trimmers and Switches

External Volume Control

The volume of the device can either be set statically via software or controlled externally via a physical interface.

SB3230 supports both analog and digital volume control functionality, although only one can be enabled at a time. Digital control is supported with either a momentary switch or a rocker switch. In the latter case, the rocker switch can also be used to control memory selects.

Analog Volume Control

Both the external (analog) volume control and trimmers work with a three−terminal 100 kΩ – 360 kΩ variable resistor. The volume control can have either a log or linear taper, which is selectable via software. It is possible to use a VC with up to 1 MΩ of resistance, but this could result in a slight decrease in the resolution of the taper.

Trimmers

The trimmer interface provides the ability to control up to 19 hearing aid parameters through up to four trimmers. A single trimmer parameter can have up to 16 values and a single trimmer can control multiple parameters (e.g., Trimmer 1 can control compression ratio in all four channels simultaneously). The trimmer must be three−terminal 100 kΩ to 360 kΩ variable resistors and have a linear taper.

Parameters that can be assigned to trimmers include Noise Reduction, Low Cut, High Cut, Compression Ratio, Wideband Gain, Tinnitus Noise Level, Crossover Frequency, Lower Threshold, Upper Threshold, EQ Gain, Squelch Threshold, High Level Gain, Low Level Gain, AGC−O Threshold, Static Volume Control and Peak Clipper Threshold.

NOTE: There may be limitations to which parameters can be used together.

Digital Volume Control

The digital volume control makes use of two pins for volume control adjustment, VC and D_VC, with momentary switches connected to each. Closure of the switch to the VC pin indicates a gain increase while closure to the D_VC pin indicates a gain decrease. Figure 7 shows how to wire the digital volume control to SB3230.

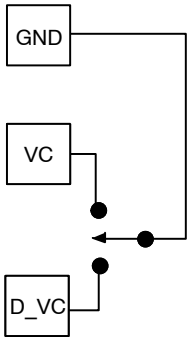


Figure 7. Wiring for Digital Volume Control

Memory Select Switches

Two Memory Select (MS) interfaces are available to support one or two 2−pole switches that can be used to switch between up to four memory profiles. The MS interface can be configured for the use of either momentary or static switches. The interface hardware can be configured to internally activate either a pull−up or pull−down resistor, depending on the physical wiring of the switch.

The audio path is temporarily faded−out and an acoustic indicator is optionally played out whenever the device transitions between memories. Each memory is assigned a unique acoustic indicator. See the Evoke Acoustic Indicators section for details on the acoustic indicators and related configurations.

NOTE: In situations where D−Only mode is activated, there is an option to disable the MS2 pin for products that may contain a reed switch, and you want to have it disabled.

Momentary Switch on MS1

This mode uses a single momentary switch on MS1 input to change memories. Using this mode causes the part to start in memory A, and whenever the button is pressed, the next valid memory is loaded. When the user is in the last valid memory, a button press causes memory A to be loaded. Thus, the possible selection sequences are:

If 4 valid memories: ABCDABCDA…
If 3 valid memories: ABCABCA…
If 2 valid memories: ABABA…
If 1 valid memory: AAA…

Momentary Switch on MS1, Static Switch on MS2 (D−only, Jump to Last Memory)

This mode uses a static switch on MS2 and a momentary switch on MS1 to change memories. It can be used to support the Automatic Telecoil feature, see section Automatic Telecoil. There are two possible configurations, depending on the setting of the pull−up/pull−down resistors.

Case 1. Pull−up/Pull−down Resistors set to Pull−down

If the static switch on MS2 is LOW, the part starts in memory A and is controlled by the momentary switch on MS1 as described in section Momentary Switch on MS1, with the exception that memory D is not used. If the static switch on MS2 is set to HIGH, the part automatically jumps to memory D (occurs on startup or during normal operation). In this setup, the state of the momentary switch on MS1 is ignored. When MS2 is set to LOW, the part loads in the memory that was active prior to jumping to memory D.

The possible memory selection sequences are:
If MS2 = LOW and there are four valid memories, MS1 selects: ABCABCA…
If MS2 = LOW and there are three valid memories, MS1 selects: ABABA…
If MS2 = LOW and there is one valid memory: A
If MS2 = HIGH: D

Case 2. Pull−up/Pull−down Resistors set to Pull−up

If the static switch on MS2 is HIGH, the part starts in memory A and is controlled by the momentary switch on MS1 as described in section Momentary Switch on MS1, with the exception that memory D is not used. If the static switch on MS2 is set to LOW, the part automatically jumps to memory D (occurs on startup or during normal operation). In this setup, the state of the momentary switch on MS1 is ignored. When MS2 is set to HIGH, the part loads in the memory that was active prior to jumping to memory D.

The possible memory selection sequences are:
If MS2 = HIGH and there are four valid memories, MS1 selects: ABCABCA...
If MS2 = HIGH and there are three valid memories, MS1 selects: ABABA...
If MS2 = HIGH and there is one valid memory: A
If MS2 = LOW: D

Static Switch on MS1, Static Switch on MS2 (D−Only, Jump to Last Memory)

This mode uses two static switches to change memories. Similar to the behaviour described in the Static Switch on MS1 and MS2 section, this mode will switch to memory D if the static switch on MS2 is HIGH (the state of the switch on MS1 is ignored). The mode, however, supports a maximum of three memories (even if four valid memories are programmed). This mode can be used to support the Automatic Telecoil feature (see the Automatic Telecoil section).

In this mode, it is possible to jump from any memory to any other memory by changing the state of both switches. If the two switches are changed one after the other, the part transitions to an intermediate memory before reaching the final memory.

The part starts in whatever memory the switches are selecting. If a memory is invalid, the part defaults to memory A.

Table 4. STATIC SWITCH TRUTH TABLE: D−ONLY ENABLED; INTERNAL RESISTORS SET TO PULL−DOWN (EXAMPLE WITH THREE−VALID MEMORIES)

Binary State (MS1/MS2)	Selected Memory
00	Memory A
10	Memory B
x1	Memory D

Table 5. STATIC SWITCH TRUTH TABLE: D−ONLY ENABLED; INTERNAL RESISTORS SET TO PULL−UP (EXAMPLE WITH THREE VALID MEMORIES)

Binary State (MS1/MS2)	Selected Memory
01	Memory A
11	Memory B
x0	Memory D

Static Switch on MS1 and MS2

This mode uses two static switches to change memories. In this mode, it is possible to jump from any memory to any other memory by changing the state of both switches. If the two switches are changed one after the other, the part transitions to an intermediate memory before reaching the final memory. The part starts in whatever memory the switches are selecting. If a memory is invalid, the part defaults to memory A.

Table 6. STATIC SWITCH TRUTH TABLE: D−ONLY DISABLED

Binary State (MS1/MS2)	Selected Memory
00	Memory A
10	Memory B
01	Memory C
11	Memory D

Rocker Switch Support

The device supports connection of a rocker switch to the digital volume control interface that can perform volume control (VC) adjustments and/or memory selection (MS).

There are three modes of operation:

- Digital Volume Control Mode
- Momentary Memory Select Mode
- Mixed Mode (VC and MS)

In Digital VC mode, the rocker switch provides the digital volume control functionality described in this section.

In Momentary Memory Select mode, the rocker switch allows cycling through the memory profiles in both directions. An “up” switch closure indicates a program advance to the next *higher* numbered memory and “down”

switch closures indicates a program retreat to the next *lower* numbered memory. In this mode, volume control is only available through software control.

In Mixed Mode, operation of the switch as a volume control or memory select is governed by the time duration of the switch closure: either short or long. The discrimination of short and long pulses is set by a programmable, time−threshold value, from 1 s to 5 s in 1 s increments. An additional programmable parameter determines whether the short pulses refer to volume−control operation or memory−select operation.

If long pulses control memory select operation, the memory change is initiated once the switch is held for the long pulse period without requiring the switch to be released. In Digital VC mode or Momentary Memory Select mode, the action takes place after the switch is released.

AGC−O

The AGC−O module is an output limiting circuit with a fixed compression ratio of ∞ : 1. The limiting level is programmable as a level measured in dB from full scale. The maximum output of the device is 0 dBFS.

The AGC−O module has its own level detector, with programmable attack and release time constants.

Graphic Equalizer

SB3230 has a 8−band graphic equalizer. Each band provides up to 31 dB of gain adjustment in 1 dB increments.

Biquadratic Filters

Additional frequency shaping can be achieved by configuring generic biquad filters. The transfer function for each of the biquad filters is as follows:

$$H(z) = \frac{b0 + b1 \times z^{-1} + b2 \times z^{-2}}{1 + a1 \times z^{-1} + a2 \times z^{-2}}$$

NOTE: The *a0* coefficient is hard−wired to always be '1'. The coefficients are each 16 bits in length and formatted as one sign bit, one integer bit and 14 fractional bits. This maps onto a decimal range of −2.0 to 2.0 before quantization (−32767 to 32767 after quantization).

Thus, before quantization, the floating−point coefficients must be in the range $-2.0 \le x < 2.0$ and quantized with the function:

$$\text{round}\left(x \times 2^{14}\right)$$

After designing a filter, the quantized coefficients can be entered into the PreBiquads or PostBiquads tab in the Interactive Data Sheet. The coefficients b0, b1, b2, a1, and a2 are as defined in the transfer function above. The parameters meta0 and meta1 do not have any effect on the signal processing, but can be used to store additional information related to the associated biquad.

The underlying code in the product components automatically checks all of the filters in the system for stability (i.e., the poles have to be within the unit circle) before updating the graphs on the screen or programming the coefficients into the hybrid. If the Interactive Data Sheet receives an exception from the underlying stability checking code, it automatically disables the biquad being modified and displays a warning message. When the filter is made stable again, it can be re−enabled.

Also note that in some configurations, some of these filters may be used by the product component for microphone/telecoil compensation, low−frequency EQ, etc. If this is the case, the coefficients entered by the user into IDS are ignored and the filter designed by the software is programmed instead. For more information on filter design refer to the Biquad Filters In PARAGON Digital Hybrid information note.

Tinnitus Treatment Noise

The Tinnitus Treatment noise is generated using white noise generator hardware and shaping the generated noise using four 2nd order biquadratic filters. The filter parameters are the same coefficients as those presented in the Biquadratic Filters section.

The Tinnitus Treatment noise can be added into the signal path at two possible locations: before the VC (before the AGC−O, but compensated for the Wideband Gain) or after the VC (between the last generic biquad and the Cross Fader).

If the noise is injected before the VC and the audio path is also enabled, the device can be set up to either have both the audio path and noise adjust via the VC, or to have only the noise adjust via the VC (see Table 7). If the noise is injected after the VC, it is not affected by VC changes.

Table 7. NOISE INSERTION MODES

Noise Insertion Modes	VC Controls	Noise Injected
Off	Audio	Off
Pre VC	Audio + Noise	Pre VC
Post VC	Audio	Post VC
Noise only Pre VC	Noise	Pre VC
Noise only Post VC	–	Post VC
Pre VC with Noise	Noise	Pre VC

EVOKE Acoustic Indicators

Ten Acoustic Indicators are available for indicating events. Each indicator is fixed to a particular event. Any event can have its assigned indicator enabled or disabled although not always independently. Individual enable/disable control is provided for the following event or group of events:

- Power on reset (POR)
- Four memory selects
- Volume Up and Volume Down
- Volume Max and Volume Min
- Low Battery

Each Acoustic Indicator is made up of up to four faded tones. A faded tone exhibits a nominal 32 ms fade−in and

fade−out transition time. The duration of an Acoustic Indicator is configurable, with a maximum value of 6.35 seconds.

EVOKE Acoustic Indicators can be programmed as output referred or input referred (prior to the filter bank).

Power Management

SB3230 has three user−selectable power management schemes to ensure the hearing aid turns off gracefully at the end of battery life. Shallow reset, Deep reset and Advanced Reset mode. It also contains a programmable power on reset delay function.

Power On Reset Delay

The programmable POR delay controls the amount of time between power being connected to the hybrid and the audio output being enabled. This gives the user time to properly insert the hearing aid before the audio starts, avoiding the temporary feedback that can occur while the device is being inserted. During the delay period, momentary button presses are ignored.

Power Management Functionality

As the voltage on the hearing aid battery decreases, an audible warning is given to the user indicating the battery life is low. In addition to this audible warning, the hearing aid takes other steps to ensure proper operation given the weak supply. The exact hearing aid behaviour in low supply conditions depends on the selected POR mode. The hearing aid has three POR modes:

- Shallow Reset Mode
- Deep Reset Mode
- Advanced Mode

Shallow Reset Mode

In Shallow Reset mode, the hearing aid will operate normally when the battery is above 0.95 V. Once the supply voltage drops below 0.95 V the audio will be muted and remain in that state until the supply voltage rises above 1.1 V. Once the supply voltage drops below the control logic ramp down voltage, the device will undergo a hardware reset. At this point, the device will remain off until the supply voltage returns to 1.1 V. When the supply voltage is below the control logic voltage, but above 0.6 V and rises above the 1.1 V turn on threshold, the device will activate its output and operate from the memory that was active prior to reset. If the supply voltage drops below 0.6 V, and rises above the 1.1 V turn on threshold, the device will reinitialize, activate its output and operate from memory A.

Deep Reset Mode

In Deep Reset mode, the hearing aid will operate normally when the battery is above 0.95 V. Once the supply voltage drops below 0.95 V the audio will be muted. The device remains in this state until the supply voltage drops below the hardware reset voltage of 0.6 V. When this occurs, the device will load memory A and operate normally after the supply voltage goes above 1.1 V.

Advanced Reset Mode

Advanced Reset Mode on SB3230 is a more sophisticated power management scheme than shallow and deep reset modes. This mode attempts to maximize the device's usable battery life by reducing the gain to stabilize the supply based on the instantaneous and average supply voltage levels. Instantaneous supply fluctuations below 0.95 V can trigger up to two 3 dB, instantaneous gain reductions. Average supply drops below 0.95 V can trigger up to eighteen, 1 dB average gain reductions.

While the average supply voltage is above 0.95 V, an instantaneous supply voltage fluctuation below 0.95 V will trigger an immediate 3 dB gain reduction. After the 3 dB gain reduction has been applied, the advanced reset model holds off checking the instantaneous voltage level for a monitoring period of 30 second in order to allow the voltage level to stabilize. If after the stabilization time the instantaneous voltage drops a second time below 0.95 V during the next monitoring period, the gain will be reduced an additional 3 dB for a 6 dB total reduction and a 30 second stabilization time is activated. The advanced reset mode continues to monitor the instantaneous voltage levels over 30 second monitoring periods. If the instantaneous voltage remains above 1.1 V during that monitoring period, the gain will be restored to the original setting regardless of whether one or two gain reductions are applied. If two gain reductions are applied and the instantaneous voltage level remains above 1.0 V for a monitoring period, the gain will be restored to a 3 dB reduction.

Should the average supply voltage drop below 0.95 V, the device will then reduce the gain by 1 dB every 10 seconds until either the average supply voltage rises above 0.95 V or a total of 18 average gain reductions have been applied, at which point the audio path will be muted. If the average supply voltage returns to a level above 1.1 V, the audio path will first be un−muted, if required. The gain will then be increased by 1 dB every 10 seconds until either the average supply voltage drops below 1.1 V, or all average gain reductions have been removed. No action is taken while the average supply voltage resides between 0.95 V and 1.1 V.

NOTE: Instantaneous and average gain reductions are adjusted independently.

When the instantaneous voltage falls below the hardware shutdown voltage, the device will undergo a hardware reset. When it turns back on because the voltage has risen above the turn−on threshold of 0.6 V, it will behave the same as it would in shallow reset mode.

Low Battery Notification

Notification of the low battery condition via an acoustic indicator is optionally performed when the battery voltage drops below a configurable low battery notification threshold. The low battery indicator is repeated every five minutes until the device shuts down.

SDA and I²C Communication

SB3230 can be programmed using the SDA or I²C protocol. During parameter changes, the main audio signal path of the hybrid is temporarily muted using the memory switch fader to avoid the generation of disturbing audio transients. Once the changes are complete, the main audio path is reactivated. Any changes made during programming are lost at power−off unless they are explicitly burned to EEPROM memory.

Improvements have been made to the ARK software, resulting in improved communication speed. Certain parameters in ARKonline can be selected to reduce the number of pages that need to be read out. In SDA mode, SB3230 is programmed via the SDA pin using industry standard programming boxes. I²C mode is a two−wire interface which uses the SDA pin for bidirectional data and CLK as the interface clock input. I²C programming support is available on the HiPro (serial or USB versions) and ON Semiconductor's DSP Programmer 3.0.

ORDERING INFORMATION

Device	Package	Shipping†
SA3230−E1−T	25 Pad Hybrid Case 127DN	250 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Hybrid Jig Ordering Information

To order a Hybrid Jig Evaluation Board for SB3230 contact your Sales Account Manager or FAE and use part number SA3405GEVB.

PAD LOCATIONS

Table 8. PAD POSITION AND DIMENSIONS

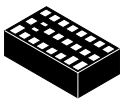
Pad No.	Pad Position		Pad Dimensions	
	X	Y	Xdim (mil)	Ydim (mil)
1	0	0	20	33
2	−27	0	20	33
3	−54	−5	20	23
4	−81	−5	20	23
5	−108	−5	20	23
6	−135	−5	20	23
7	−162	−5	20	23
8	−189	0	20	33
9	−189	42	20	23
10	−189	85	20	23
11	−162	85	20	23
12	−135	85	20	23
13	−108	85	20	23
14	−81	85	20	23
15	−54	85	20	23
16	−27	85	20	23
17	0	85	20	23
18	0	42	20	23
19	−27	42	20	23
20	−54	42	20	23
21	−81	42	20	23
22	−108	42	20	23
23	−135	42	20	23
24	−162	26.5	18	12
25	−162	53.5	18	12

Table 8. PAD POSITION AND DIMENSIONS

Pad No.	X	Y	Xdim (mm)	Ydim (mm)
1	0	0	0.508	0.838
2	−0.686	0	0.508	0.838
3	−1.372	−0.127	0.508	0.584
4	−2.057	−0.127	0.508	0.584
5	−2.743	−0.127	0.508	0.584
6	−3.429	−0.127	0.508	0.584
7	−4.115	−0.127	0.508	0.584
8	−4.801	0	0.508	0.838
9	−4.801	1.067	0.508	0.584
10	−4.801	2.159	0.508	0.584
11	−4.115	2.159	0.508	0.584
12	−3.429	2.159	0.508	0.584
13	−2.743	2.159	0.508	0.584
14	−2.057	2.159	0.508	0.584
15	−1.372	2.159	0.508	0.584
16	−0.686	2.159	0.508	0.584
17	0	2.159	0.508	0.584
18	0	1.067	0.508	0.584
19	−0.686	1.067	0.508	0.584
20	−1.372	1.067	0.508	0.584
21	−2.057	1.067	0.508	0.584
22	−2.743	1.067	0.508	0.584
23	−3.429	1.067	0.508	0.584
24	−4.115	0.673	0.457	0.305
25	−4.115	1.359	0.457	0.305

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

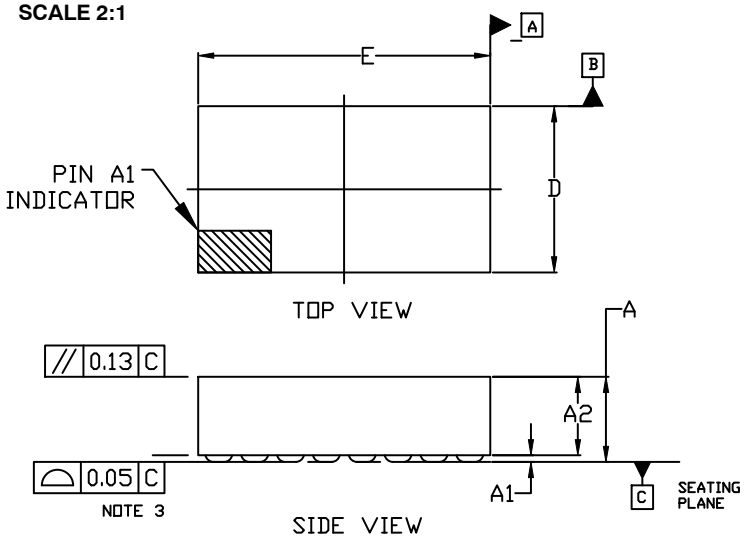
ON Semiconductor®

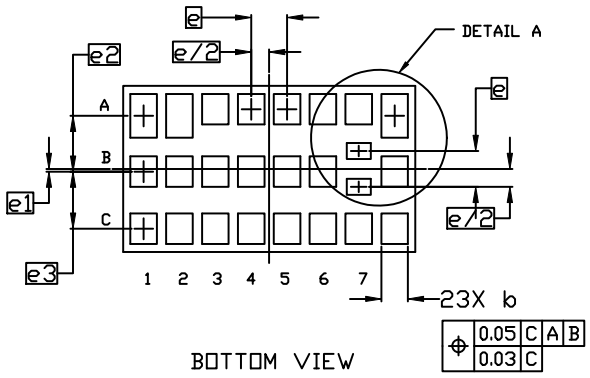


SCALE 2:1

SIP25, 5.59x3.18
CASE 127DN
ISSUE A

DATE 21 JUL 2020

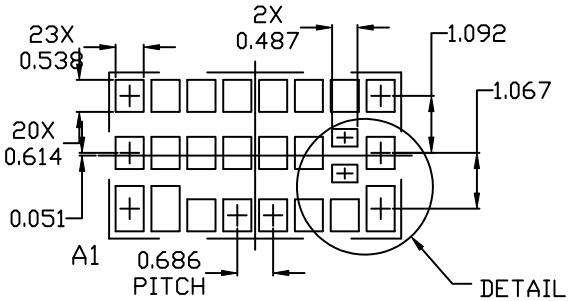




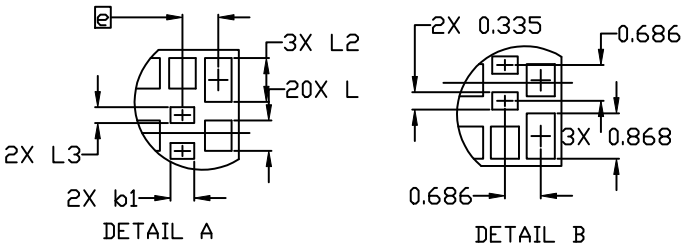
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE PADS.

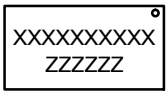
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.68
A1	0.08	0.13	0.18
A2	---	---	1.50
b	0.478	0.508	0.538
b1	0.427	0.457	0.487
D	3.05	3.18	3.31
E	5.46	5.59	5.72
e	0.686 BSC		
e1	0.051 BSC		
e2	1.067 BSC		
e3	1.092 BSC		
L	0.554	0.584	0.614
L2	0.808	0.838	0.868
L3	0.275	0.305	0.335



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



GENERIC MARKING DIAGRAM*



XX = Specific Device Code
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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