

Self-Protected Low Side Driver with Temperature and Current Limit

65 V, 7.0 A, Single N-Channel

NCV8406A, NCV8406B

NCV8406A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

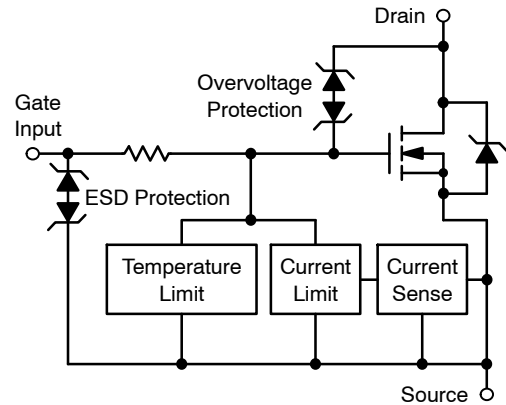
Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- These Devices are Faster than the Rest of the NCV Devices
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

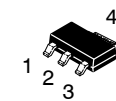
Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

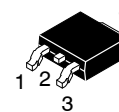
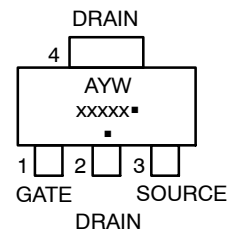
V _{DSS} (Clamped)	R _{DS(on)} TYP	I _D TYP (Limited)
65 V	210 mΩ	7.0 A



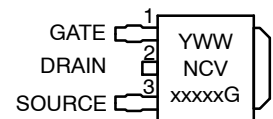
MARKING DIAGRAM



SOT-223
CASE 318E
STYLE 3



DPAK
CASE 369C



A = Assembly Location
Y = Year
W, WW = Work Week
xxxxx = 8406A or 8406B
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information page 10 of this data sheet.

NCV8406A, NCV8406B

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V _{DSS}	60	Vdc
Gate-to-Source Voltage	V _{GS}	± 14	Vdc
Drain Current	I _D	Internally Limited	
Total Power Dissipation – SOT-223 Version @ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2)	P _D	1.25 1.81	W
Total Power Dissipation – DPAK Version @ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2)	P _D	1.31 2.31	W
Thermal Resistance – SOT-223 Version Junction-to-Soldering Point Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	R _{θJS} R _{θJA} R _{θJA}	7.0 100 69	°C/W
Thermal Resistance – DPAK Version Junction-to-Soldering Point Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	R _{θJS} R _{θJA} R _{θJA}	1.0 95 54	°C/W
Single Pulse Inductive Load Switching Energy (Starting T _J = 25°C, V _{DD} = 50 Vdc, V _{GS} = 5.0 Vdc, I _L = 2.1 Apk, L = 50 mH, R _G = 25 Ω)	E _{AS}	110	mJ
Load Dump Voltage (V _{GS} = 0 and 10 V, R _I = 2 Ω, R _L = 7 Ω, t _d = 400 ms)	V _{LD}	75	V
Operating Junction Temperature Range	T _J	-40 to 150	°C
Storage Temperature Range	T _{stg}	-55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted onto minimum pad size (100 sq/mm) FR4 PCB, 1 oz cu.
2. Mounted onto 1" square pad size (700 sq/mm) FR4 PCB, 1 oz cu.

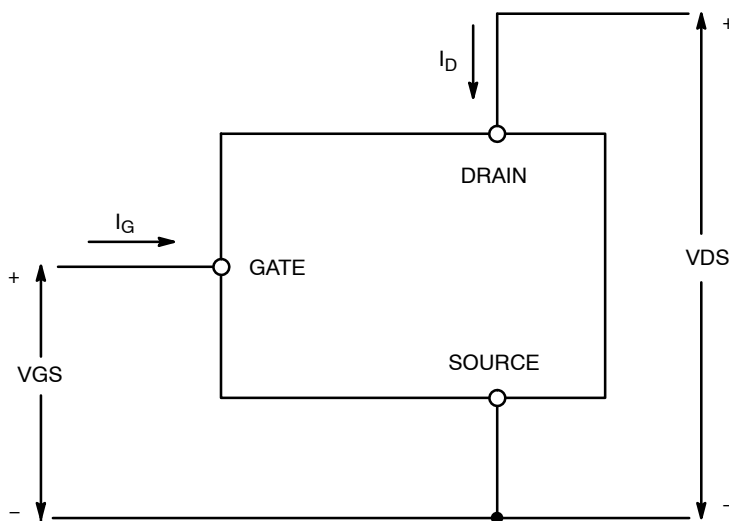


Figure 1. Voltage and Current Convention

NCV8406A, NCV8406B

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Clamped Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 2\text{ mA}$)	$V_{(BR)DSS}$	60	65	70	V
Zero Gate Voltage Drain Current ($V_{DS} = 52\text{ V}$, $V_{GS} = 0\text{ V}$)	I_{DSS}	-	22	100	μA
Gate Input Current ($V_{GS} = 5.0\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	-	30	100	μA

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 150\ \mu\text{A}$) Threshold Temperature Coefficient	$V_{GS(th)}$	1.2 -	1.66 4.0	2.0 -	V -mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 10\text{ V}$, $I_D = 2.0\text{ A}$, $T_J @ 25^\circ\text{C}$)	$R_{DS(on)}$	-	185	210	m Ω
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 5.0\text{ V}$, $I_D = 2.0\text{ A}$, $T_J @ 25^\circ\text{C}$) ($V_{GS} = 5.0\text{ V}$, $I_D = 2.0\text{ A}$, $T_J @ 150^\circ\text{C}$)	$R_{DS(on)}$	- -	210 445	240 520	m Ω
Source-Drain Forward On Voltage ($I_S = 7.0\text{ A}$, $V_{GS} = 0\text{ V}$)	V_{SD}	-	0.9	1.1	V

SWITCHING CHARACTERISTICS (Note 6)

Turn-on Delay Time	$R_L = 6.6\ \Omega$, $V_{in} = 0\text{ to }10\text{ V}$, $V_{DD} = 13.8\text{ V}$, $I_D = 2.0\text{ A}$, 10% V_{in} to 10% I_D	$t_{d(on)}$	-	127	-	ns
Turn-on Rise Time	$R_L = 6.6\ \Omega$, $V_{in} = 0\text{ to }10\text{ V}$, $V_{DD} = 13.8\text{ V}$, $I_D = 2.0\text{ A}$, 10% I_D to 90% I_D	t_{rise}	-	486	-	ns
Turn-off Delay Time	$R_L = 6.6\ \Omega$, $V_{in} = 0\text{ to }10\text{ V}$, $V_{DD} = 13.8\text{ V}$, $I_D = 2.0\text{ A}$, 90% V_{in} to 90% I_D	$t_{d(off)}$	-	1600	-	ns
Turn-off Fall Time	$R_L = 6.6\ \Omega$, $V_{in} = 0\text{ to }10\text{ V}$, $V_{DD} = 13.8\text{ V}$, $I_D = 2.0\text{ A}$, 90% I_D to 10% I_D	t_{fall}	-	692	-	ns
Slew Rate ON	$R_L = 6.6\ \Omega$, $V_{in} = 0\text{ to }10\text{ V}$, $V_{DD} = 13.8\text{ V}$, $I_D = 2.0\text{ A}$, 70% to 50% V_{DD}	dV_{DS}/dT_{on}	-	79	-	V/ μs
Slew Rate OFF	$R_L = 6.6\ \Omega$, $V_{in} = 0\text{ to }10\text{ V}$, $V_{DD} = 13.8\text{ V}$, $I_D = 2.0\text{ A}$, 50% to 70% V_{DD}	dV_{DS}/dT_{off}	-	27	-	V/ μs

SELF PROTECTION CHARACTERISTICS (Note 4)

Current Limit	$V_{DS} = 10\text{ V}$, $V_{GS} = 5.0\text{ V}$, $T_J = 25^\circ\text{C}$ (Notes 5, 7) $V_{DS} = 10\text{ V}$, $V_{GS} = 5.0\text{ V}$, $T_J = 150^\circ\text{C}$ (Notes 5, 6, 7) $V_{DS} = 10\text{ V}$, $V_{GS} = 10\text{ V}$, $T_J = 25^\circ\text{C}$ (Notes 5, 7)	I_{LIM}	5.0 3.5 6.5	7.0 4.5 8.5	9.5 6.0 10.5	A
Temperature Limit (Turn-off)	$V_{GS} = 5.0\text{ V}$ (Notes 6, 7)	$T_{LIM(off)}$	150	180	200	$^\circ\text{C}$
Thermal Hysteresis	$V_{GS} = 5.0\text{ V}$	$\Delta T_{LIM(on)}$	-	10	-	$^\circ\text{C}$
Temperature Limit (Turn-off)	$V_{GS} = 10\text{ V}$ (Notes 6, 7)	$T_{LIM(off)}$	150	180	200	$^\circ\text{C}$
Thermal Hysteresis	$V_{GS} = 10\text{ V}$	$\Delta T_{LIM(on)}$	-	20	-	$^\circ\text{C}$
Input Current during Thermal Fault	$V_{DS} = 0\text{ V}$, $V_{GS} = 5.0\text{ V}$, $T_J = T_J > T_{(fault)}$ (Note 6) $V_{DS} = 0\text{ V}$, $V_{GS} = 10\text{ V}$, $T_J = T_J > T_{(fault)}$ (Note 6)	$I_{g(fault)}$	- -	5.9 12.3	-	mA

ESD ELECTRICAL CHARACTERISTICS

Electro-Static Discharge Capability Human Body Model (HBM) Machine Model (MM)	ESD	6000 500	- -	- -	V
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Current limit measured at $380\ \mu\text{s}$ after gate pulse.
6. Not subject to production test.
7. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

TYPICAL PERFORMANCE CURVES

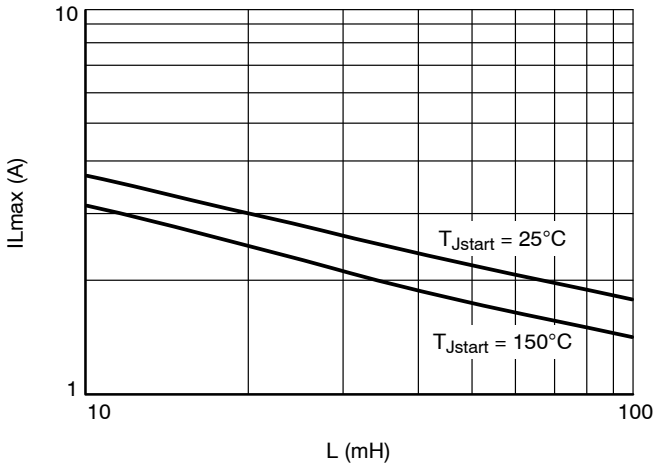


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

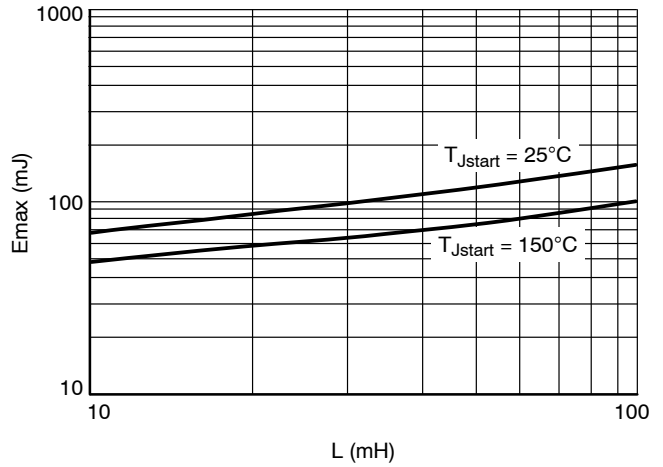


Figure 3. Single-Pulse Maximum Switching Energy vs. Load Inductance

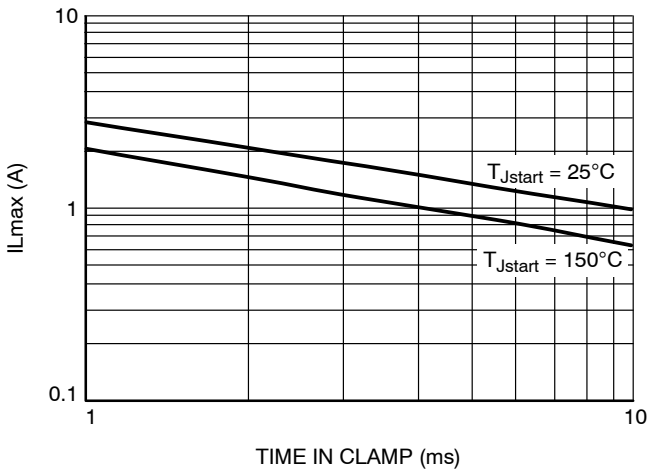


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

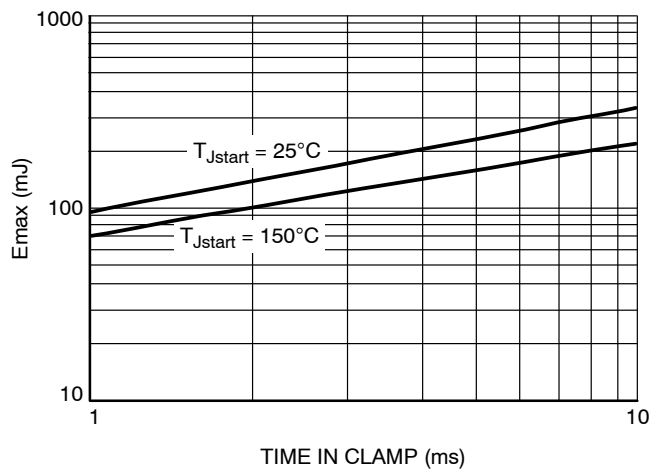


Figure 5. Single-Pulse Maximum Inductive Switching Energy vs. Time in Clamp

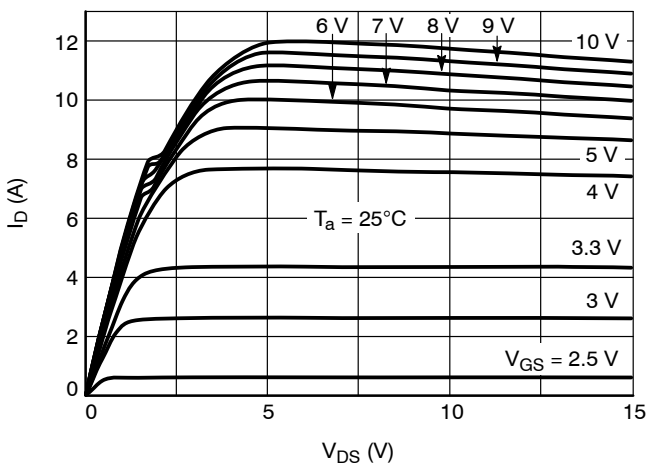


Figure 6. On-state Output Characteristics

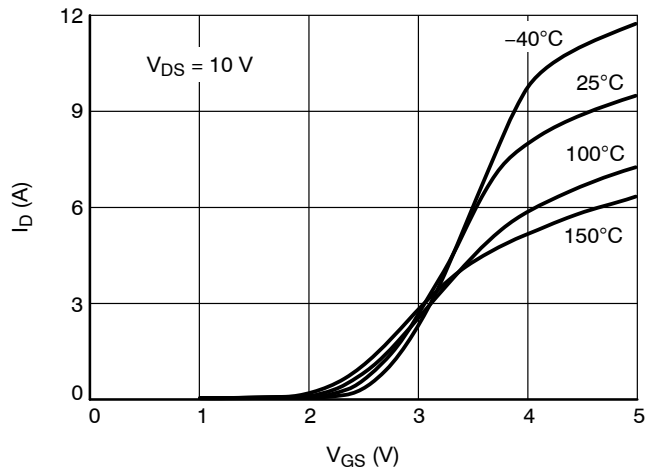


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

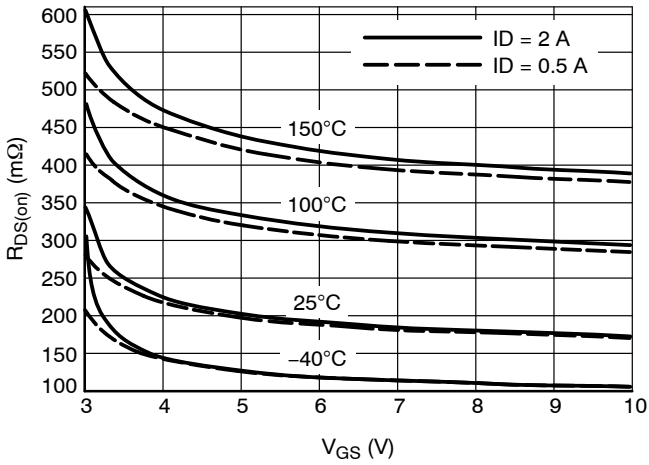


Figure 8. $R_{DS(on)}$ vs. Gate-Source Voltage

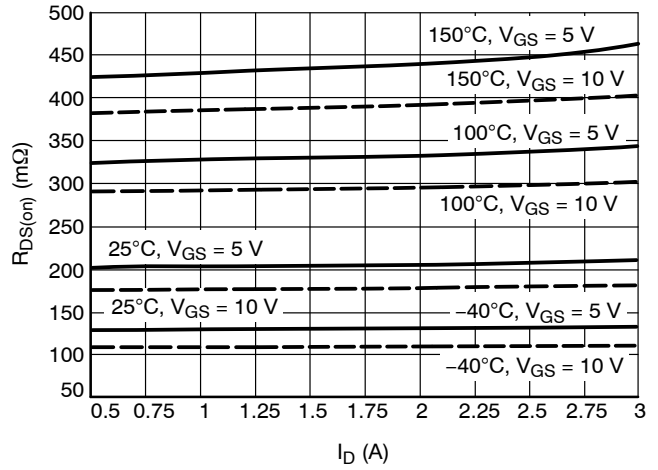


Figure 9. $R_{DS(on)}$ vs. Drain Current

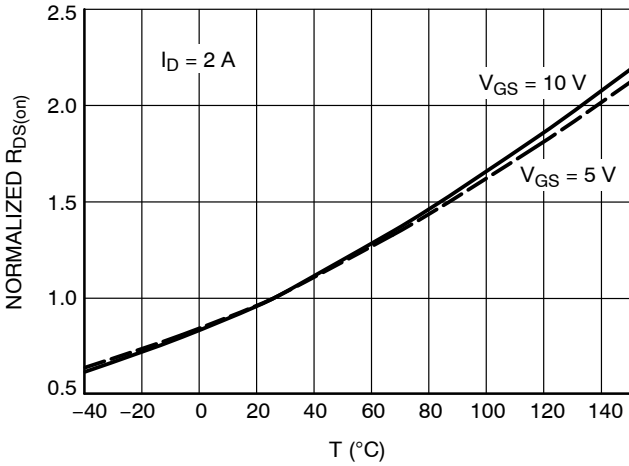


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

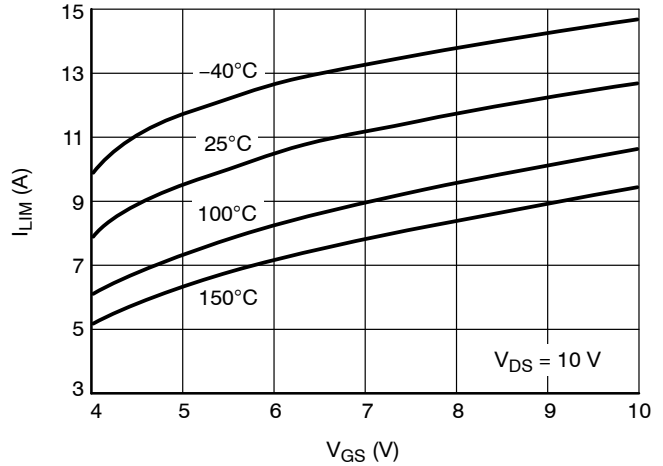


Figure 11. Current Limit vs. Gate-Source Voltage

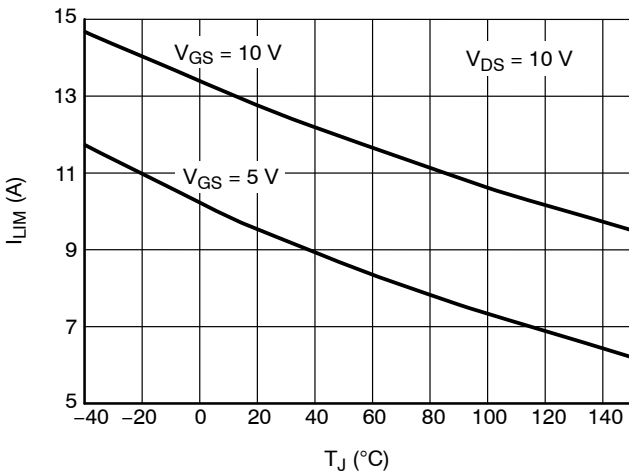


Figure 12. Current Limit vs. Junction Temperature

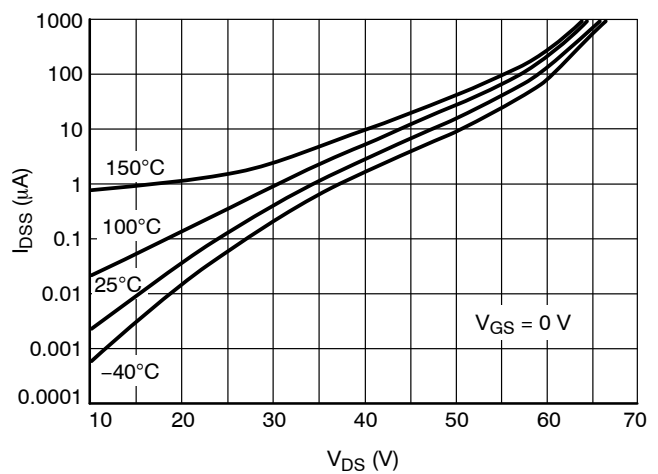


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

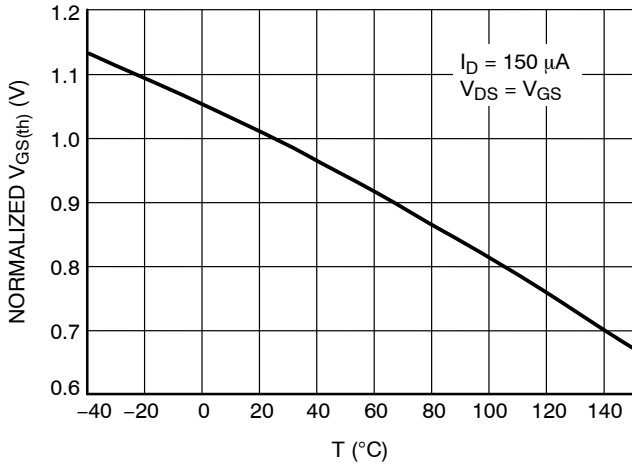


Figure 14. Normalized Threshold Voltage vs. Temperature

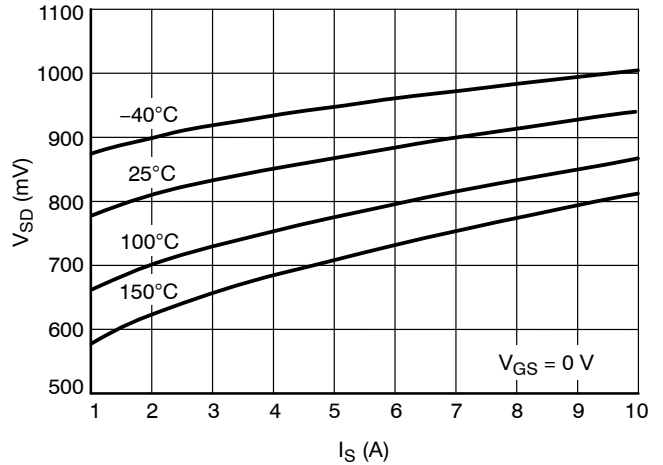


Figure 15. Source-Drain Diode Forward Characteristics

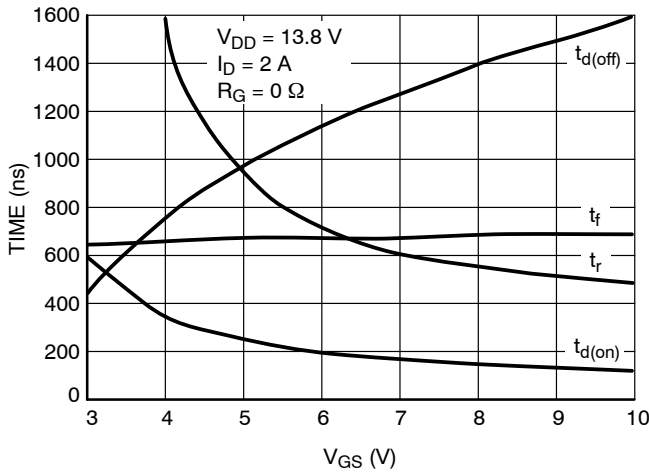


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

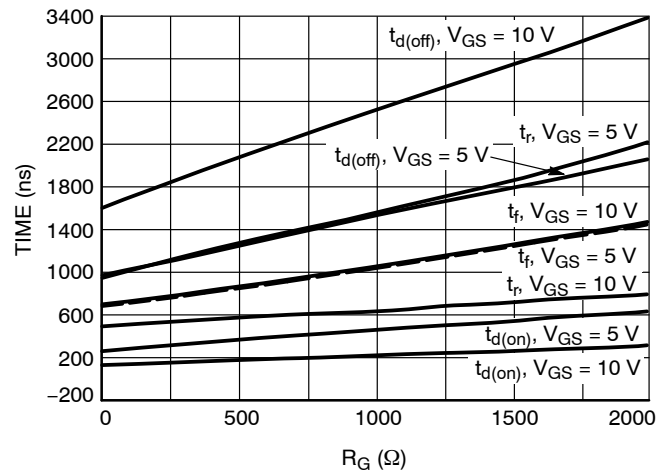


Figure 17. Resistive Load Switching Time vs. Gate Resistance

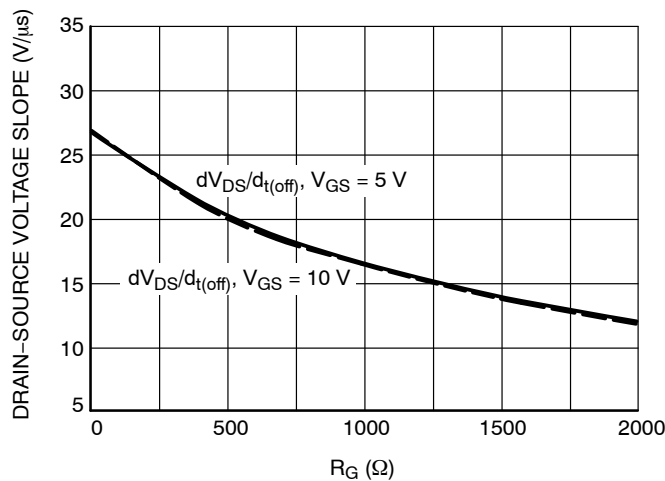


Figure 18. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

TYPICAL PERFORMANCE CURVES

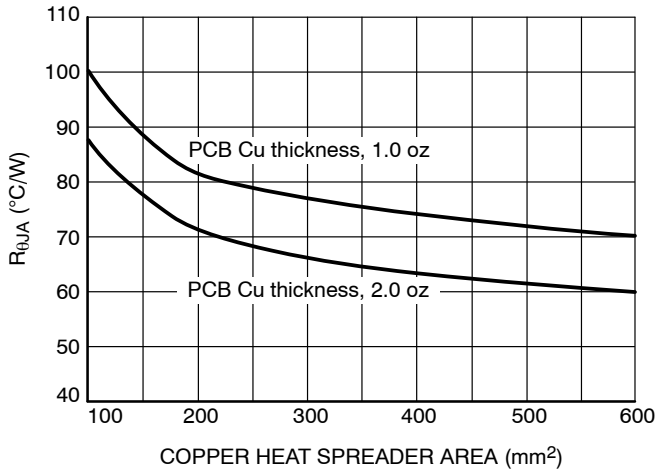


Figure 19. $R_{\theta JA}$ vs. Copper Area – SOT-223

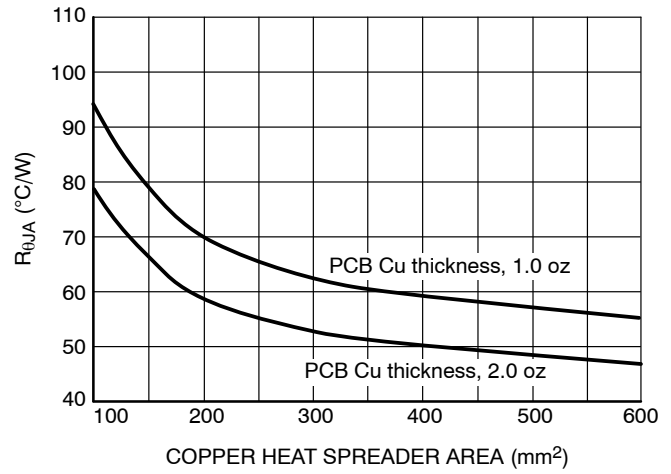


Figure 20. $R_{\theta JA}$ vs. Copper Area – DPAK

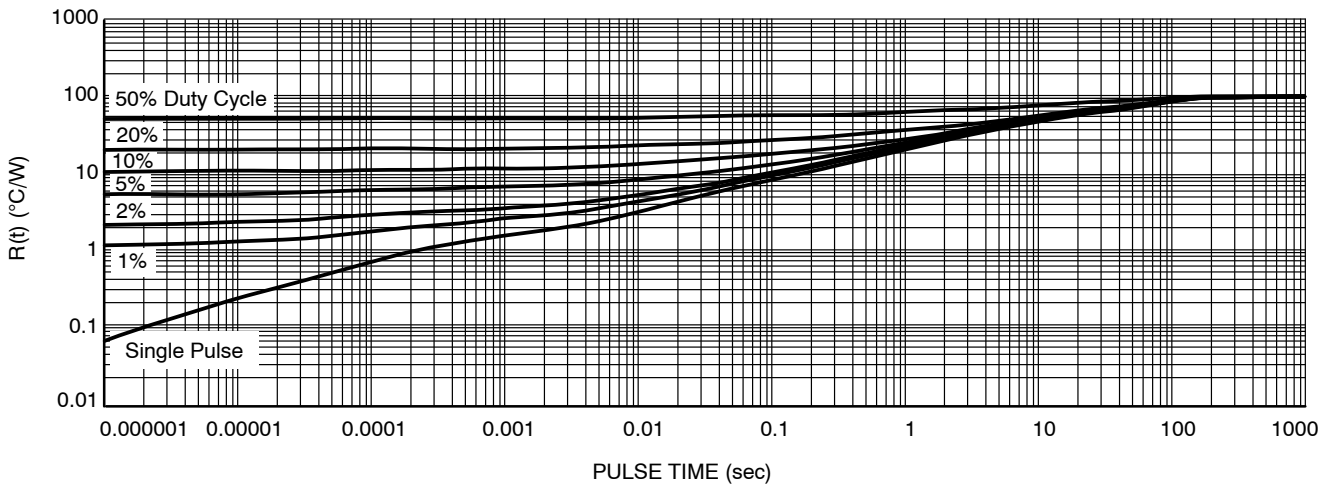


Figure 21. Transient Thermal Resistance – SOT-223 Version

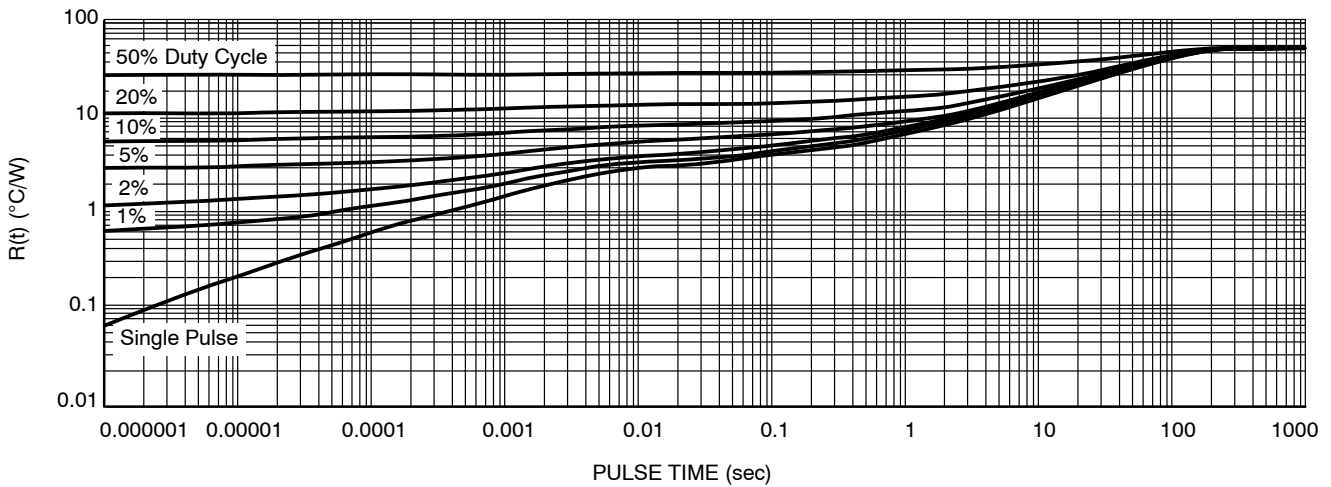


Figure 22. Transient Thermal Resistance – DPAK Version

NCV8406A, NCV8406B

TEST CIRCUITS AND WAVEFORMS



Figure 23. Resistive Load Switching Test Circuit

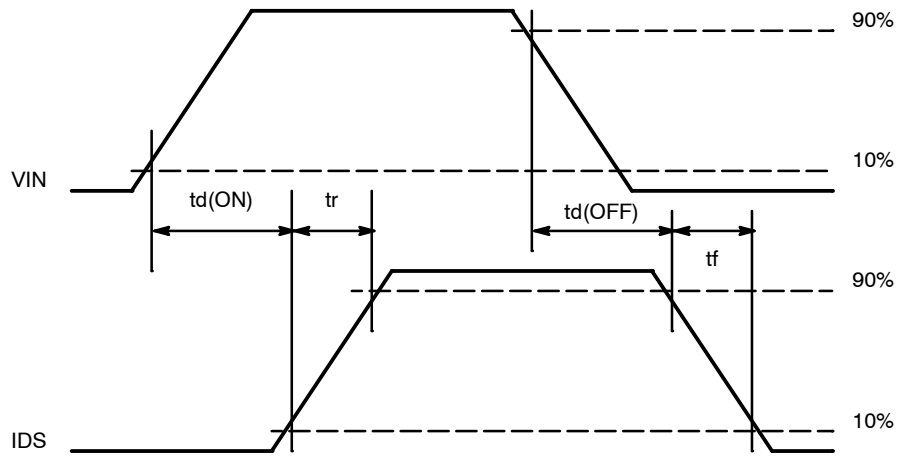


Figure 24. Resistive Load Switching Waveforms

NCV8406A, NCV8406B

TEST CIRCUITS AND WAVEFORMS



Figure 25. Inductive Load Switching Test Circuit

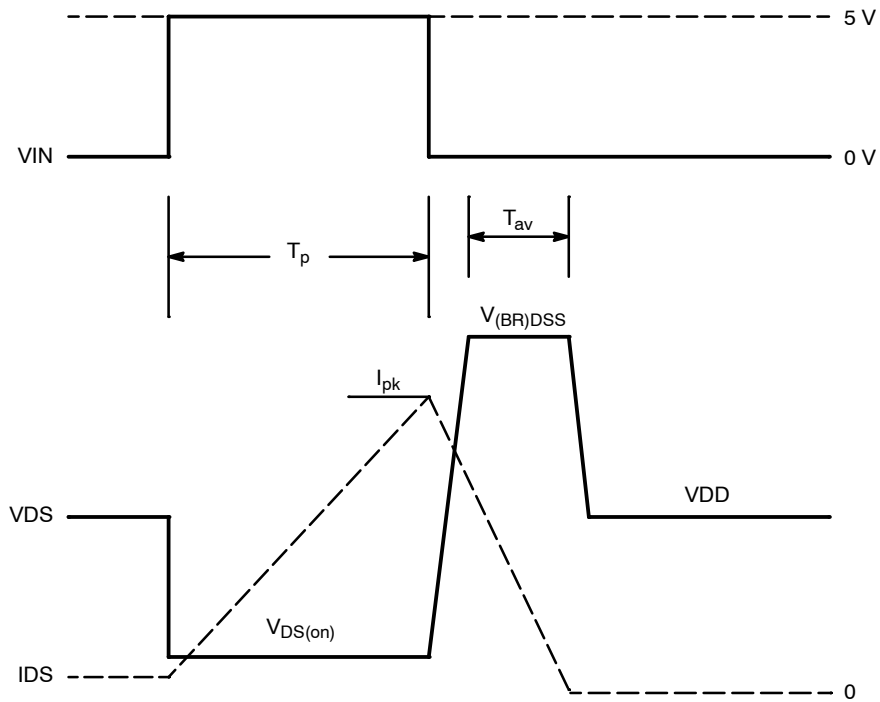


Figure 26. Inductive Load Switching Waveforms

NCV8406A, NCV8406B

ORDERING INFORMATION

Device	Package	Shipping†
NCV8406ASTT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NCV8406ASTT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV8406ADTRKG	DPAK (Pb-Free)	2500 / Tape & Reel
NCV8406BDTRKG	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

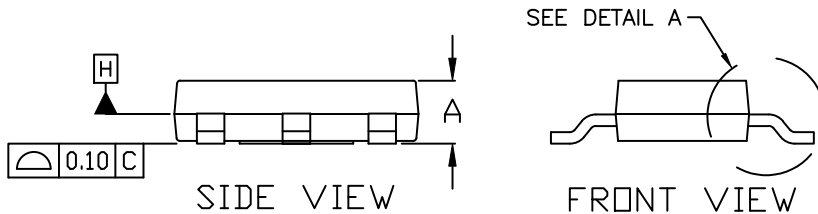
ON Semiconductor®



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

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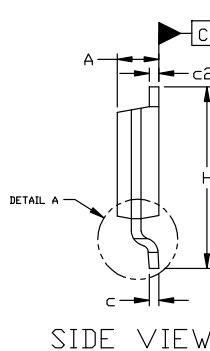
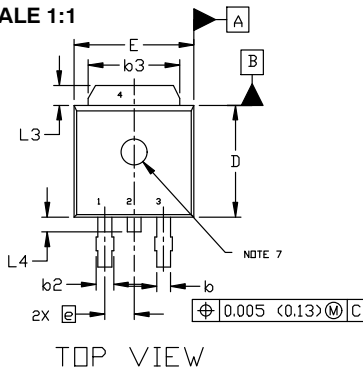
**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



**DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G**

DATE 31 MAY 2023

SCALE 1:1



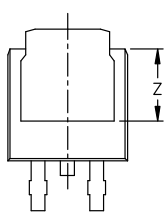
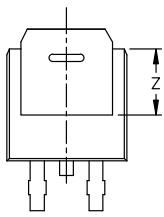
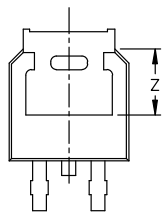
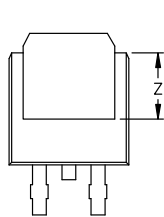
NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

TOP VIEW

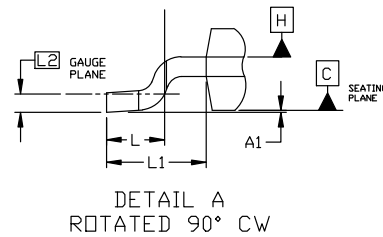
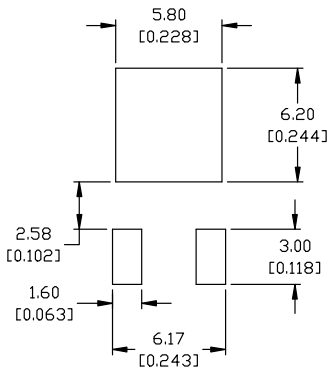
SIDE VIEW



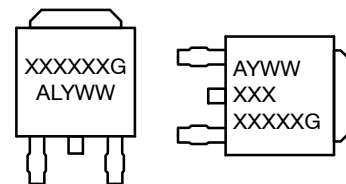
BOTTOM VIEW

BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



GENERIC MARKING DIAGRAM*



- IC
- Discrete
- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- | | | | | |
|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------|-----------------------------------------------------------------------------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> |
| <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE</p> | <p>STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE</p> |

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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