

3.3 V, Crystal to 100 MHz / 125 MHz Quad HCSL / LVDS Clock Generator

NB3N51044

The NB3N51044 is a precision, low phase noise clock generator that supports PCI Express and sRIO clock requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal or a 25 MHz single ended reference clock signal and generates four differential HCSL/LVDS outputs (See Figure 10 for LVDS interface) of 100 MHz or 125 MHz clock frequency based on frequency select input F_SEL. NB3N51044 is configurable to bypass the PLL from signal path using BYPASS, and provides the output frequency through the divider network. All clock outputs can be individually enabled / disabled through hardware input pins OE[3:0]. In addition, device can be reset using Master Reset input pin MR_OE#.

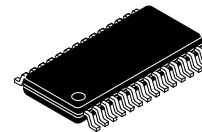
Features

- Uses 25 MHz Fundamental Crystal or Reference Clock Input
- Four Low Skew HCSL or LVDS Outputs
- Output Frequency Selection of 100 MHz or 125 MHz
- Individual OE Tri–States Outputs
- Master Reset and BYPASS Modes
- PCIe Gen 1, Gen 2, Gen 3, Gen 4 Compliant
- Typical Phase Jitter @ 125 MHz (Integrated 1.875 MHz to 20 MHz): 0.2 ps
- Typical Cycle–Cycle Jitter @ 100 MHz (10k cycles): 20 ps
- Phase Noise @ 100 MHz:

| Offset | Noise Power |
|---------|-------------|
| 100 Hz | –101 dBc/Hz |
| 1 kHz | –123 dBc/Hz |
| 10 kHz | –133 dBc/Hz |
| 100 kHz | –136 dBc/Hz |
| 1 MHz | –141 dBc/Hz |
| 10 MHz | –155 dBc/Hz |
- Operating Supply Voltage Range 3.3 V \pm 5%
- Industrial Temperature Range –40°C to +85°C
- Functionally Compatible with ICS841604I with enhanced performance
- These are Pb–Free Devices

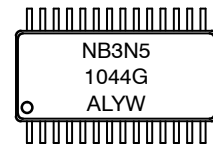
Applications

- Networking
- Consumer
- Computing and Peripherals
- Industrial Equipment
- PCIe Clock Generation Gen 1, Gen 2, Gen 3 and Gen 4



TSSOP–28
 DT SUFFIX
 CASE 948AA

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G = Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

End Products

- Switch and Router
- Set Top Box, LCD TV
- Servers, Desktop Computers
- Automated Test Equipment

NB3N51044

BLOCK DIAGRAM

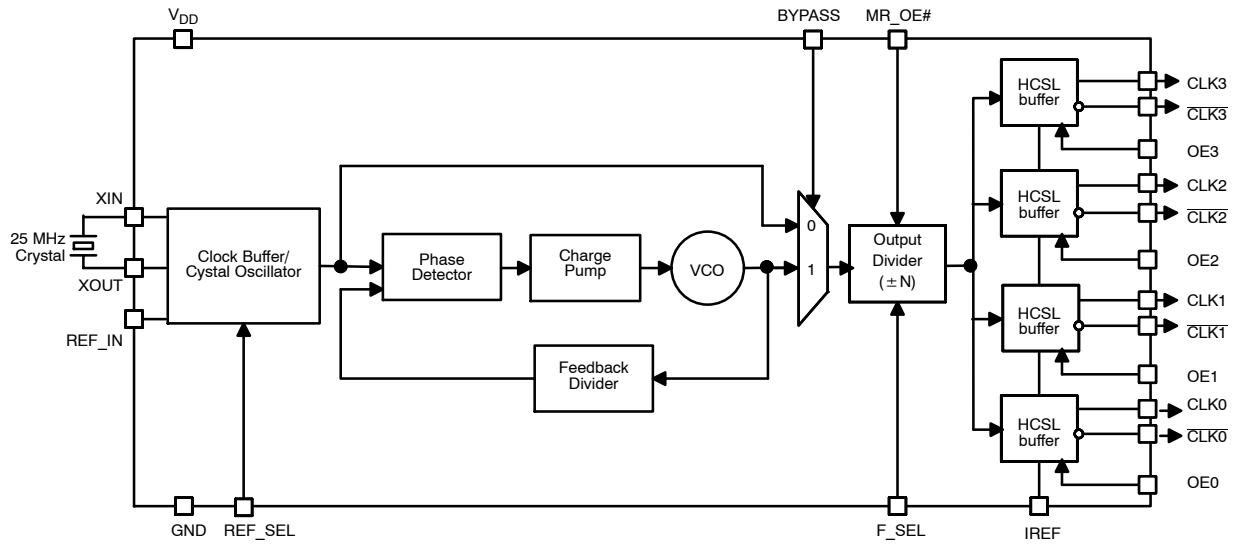


Figure 1. Block Diagram

PIN CONFIGURATION

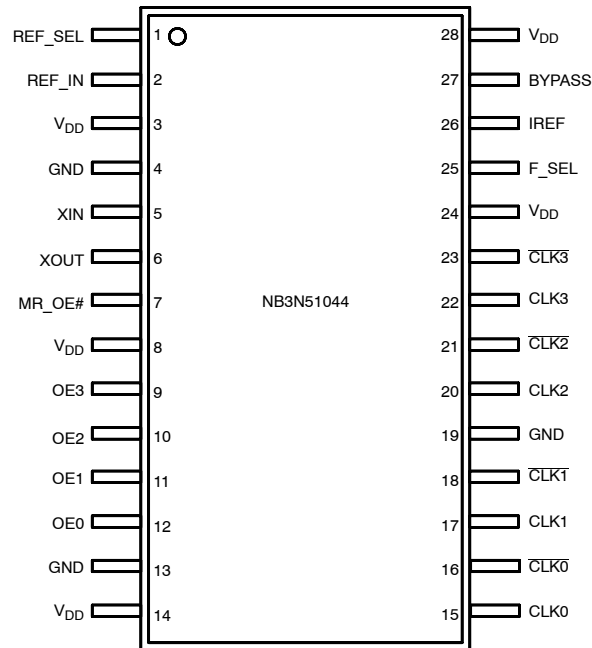


Figure 2. Pin Configuration (Top View)

NB3N51044

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

| Pin # | Pin Name | Type | Description |
|-------|--------------------------|---------------------|---|
| 1 | REF_SEL | Input | LVC MOS/ LVTTTL level input to select input reference source. Pulldown with crystal as default reference input source. |
| 2 | REF_IN | Input | 25 MHz single-ended reference input clock. |
| 3 | V _{DD} | Power | Positive supply voltage pin connected to +3.3 V typical supply voltage. |
| 4 | GND | Ground | Power supply ground 0 V. This pin provides GND return path for the device. |
| 5 | XIN | Input | 25 MHz fundamental mode crystal input connection. Ground this pin when crystal not connected. |
| 6 | XOUT | Output | 25 MHz crystal output. Float this pin when crystal not connected. |
| 7 | MR_OE# | Input | Asynchronous LVC MOS/ LVTTTL level input. When High, this pin acts as Master Reset to disable the output dividers and set outputs to high impedance (Hi-Z) mode. When Low, this pin acts as Output Enable for enabling the output buffers. Pulldown with default Low. |
| 8 | V _{DD} | Power | Positive supply voltage pin connected to +3.3 V typical supply voltage. |
| 9 | OE3 | Input | LVC MOS/ LVTTTL level interface active High output enable pin for CLK3. Pulldown with default Low and output disabled. |
| 10 | OE2 | Input | LVC MOS/ LVTTTL level interface active High output enable pin for CLK2. Pulldown with default Low and output disabled. |
| 11 | OE1 | Input | LVC MOS/ LVTTTL level interface active High output enable pin for CLK1. Pulldown with default Low and output disabled. |
| 12 | OE0 | Input | LVC MOS/ LVTTTL level interface active High output enable pin for CLK0. Pulldown with default Low and output disabled. |
| 13 | GND | Ground | Power supply ground 0 V. This pin provides GND return path for the device. |
| 14 | V _{DD} | Power | Positive supply voltage pin connected to +3.3 V typical supply voltage. |
| 15 | CLK0 | HCSL or LVDS output | Noninverted clock output. (For LVDS levels see Figure 10) |
| 16 | $\overline{\text{CLK0}}$ | HCSL or LVDS output | Inverted clock output. (For LVDS levels see Figure 10) |
| 17 | CLK1 | HCSL or LVDS output | Noninverted clock output. (For LVDS levels see Figure 10) |
| 18 | $\overline{\text{CLK1}}$ | HCSL or LVDS output | Inverted clock output. (For LVDS levels see Figure 10) |
| 19 | GND | Ground | Power supply ground 0 V. This pin provides GND return path for the device. |
| 20 | CLK2 | HCSL or LVDS output | Noninverted clock output. (For LVDS levels see Figure 10) |
| 21 | $\overline{\text{CLK2}}$ | HCSL or LVDS output | Inverted clock output. (For LVDS levels see Figure 10) |
| 22 | CLK3 | HCSL or LVDS output | Noninverted clock output. (For LVDS levels see Figure 10) |
| 23 | $\overline{\text{CLK3}}$ | HCSL or LVDS output | Inverted clock output. (For LVDS levels see Figure 10) |
| 24 | V _{DD} | Power | Positive supply voltage pin connected to +3.3 V typical supply voltage. |
| 25 | F_SEL | Input | LVC MOS/ LVTTTL level Frequency Selects PCIe (100 MHz) when Low or sRIO (125 MHz) output frequency when High. Pulldown with default of 100 MHz at outputs. |
| 26 | IREF | Output | Output current reference pin. Connect to precision resistor (typical 475 Ω) to set internal current reference |
| 27 | BYPASS | Input | LVC MOS/ LVTTTL level input. Selects PLL operation mode when Low or PLL bypass mode when High. Pulldown with default of PLL mode. |
| 28 | V _{DD} | Power | Positive supply voltage pin connected to +3.3 V typical supply voltage. |

Table 2. OUTPUT FREQUENCY SELECT FUNCTION TABLE

| Input | | Output |
|-------|--------------------|------------------------|
| F_SEL | N (Output divider) | CLK[3:0]/CLK[3:0]# |
| 0 | 5 | 100MHz (PCIe, default) |
| 1 | 4 | 125MHz (sRIO) |

Table 3. PLL BYPASS FUNCTION TABLE

| BYPASS | PLL Configuration |
|--------|------------------------------------|
| 0 | PLL Enabled (default) |
| 1 | PLL bypassed, $f_{out} = f_{IN}/N$ |

Table 4. MASTER RESET AND OE FUNCTION TABLE

| MR_OE# | OEx [x=3:0] | Function |
|-------------|-------------|---------------------------------------|
| 0 (default) | 0 (default) | CLKx, CLKx# are High impedance |
| | 1 | CLKx Output Enabled |
| 1 | x | Device reset, outputs disabled (Hi-Z) |

Table 6. ATTRIBUTES

| Characteristic | Value |
|---|----------------------|
| ESD Protection Human Body Model | 2 kV |
| Internal Input Default State Resistor | 51 kΩ |
| Moisture Sensitivity, Indefinite Time Out of Dray Pack (Note 1) | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 132,000 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

Table 7. ABSOLUTE MAXIMUM RATING (Note 2)

| Symbol | Parameter | Rating | Unit |
|------------------|---|-----------------------------------|------|
| V _{DD} | Positive power supply with respect to GND | +4.6 | V |
| V _I | Input Voltage with respect to device GND | -0.5 V to V _{DD} + 0.5 V | V |
| T _A | Operating Temperature Range | -40 to +85 | °C |
| T _{STG} | Storage temperature | -65 to +150 | °C |
| T _{SOL} | Max. Soldering Temperature (10 sec) | 265 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-ambient) 0 lfpm (Note 3) 500 lfpm | 63 55 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-case) | 50 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
- JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. INPUT REFERENCE SELECT FUNCTION TABLE

| REF_SEL | Input Reference |
|---------|--|
| 0 | Crystal, at XIN and XOUT (default) |
| 1 | Single-ended reference clock at REF_IN |

Recommended Crystal Parameters

| | |
|-----------------------------------|--------------------|
| Crystal | Fundamental AT-Cut |
| Frequency | 25 MHz |
| Load Capacitance | 16–20 pF |
| Shunt Capacitance, C ₀ | 7 pF Max |
| Equivalent Series Resistance | 50 Ω Max |
| Initial Accuracy at 25°C | ±20 ppm |
| Temperature Stability | ±30 ppm |
| Aging | ±20 ppm |

NB3N51044

Table 8. DC ELECTRICAL CHARACTERISTICS ($V_{DD} = 3.3 \text{ V} \pm 5\%$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C , Note 4)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|--|-----------|-----|--------------|---------------|
| V_{DD} | Power Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current when all outputs are ON, $OE[3:0] = 1$, $F_{CLKOUT} = 125 \text{ MHz}$ | | | 126 | mA |
| I_{OFF} | Power Supply Current when all outputs are set OFF, $OE[3:0] = 0$ | | 45 | 50 | mA |
| V_{IH} | Input HIGH Voltage (XIN, REF_IN, REF_SEL, BYPASS, F_SEL, MR_OE#) | 2.0 | | $V_{DD}+0.3$ | V |
| V_{IL} | Input LOW Voltage (XIN, REF_IN, REF_SEL, BYPASS, F_SEL, MR_OE#) | $GND-0.3$ | | 0.8 | V |
| I_{IH} | Input Leakage on logic High current at all input pins | | | 150 | μA |
| I_{IL} | Input Leakage on logic Low current at all input pins | -5 | | | μA |
| V_{OH} | Output HIGH Voltage for HCSL output (Note 5) | 660 | | 850 | mV |
| V_{OL} | Output LOW Voltage for HCSL output (Note 5) | -150 | | | mV |
| V_{MAX} | Absolute Maximum Voltage, Measured Single ended including overshoot (Notes 5, 6) | | | 1150 | mV |
| V_{MIN} | Absolute Minimum Voltage, Measured Single ended including undershoot (Notes 5, 7) | -300 | | | mV |
| V_{CROSS} | Crossing Voltage Magnitude (Absolute) for HCSL output (Notes 5, 8, 9) | 250 | | 550 | mV |
| ΔV_{CROSS} | Change in Magnitude of V_{cross} for HCSL Output (Notes 5, 8, 10) | | | 150 | mV |
| V_{RB} | Ring Back Voltage measured differentially (Note 11) | -100 | | 100 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

4. Measurement taken with outputs terminated with $R_S = 33.2 \Omega$, $R_L = 49.9 \Omega$, with test load capacitance of 2 pF and current biasing resistor set at $R_{REF} = 475 \Omega$. See Figure 9. Guaranteed by characterization.
5. Measurement taken from single-ended waveform
6. Defined as the maximum instantaneous voltage value including positive overshoot
7. Defined as the maximum instantaneous voltage value including negative overshoot
8. Measured at crossing point where the instantaneous voltage value of the rising edge of $CLKx+$ equals the falling edge of $CLKx-$.
9. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
10. Defined as the total variation of all crossing voltage of rising $CLKx+$ and falling $CLKx-$. This is maximum allowed variance in the V_{CROSS} for any particular system.
11. Differential clock must maintain a minimum $\pm 150 \text{ mV}$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{RB} \pm 100$ differential range.

NB3N51044

Table 9. AC ELECTRICAL CHARACTERISTICS ($V_{DD} = 3.3 \text{ V} \pm 5\%$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C , Note 12)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|---|-----|-----------|-----|---------------|
| f_{CLKIN} | Clock/ Crystal input frequency | | | 25 | | MHz |
| f_{CLKOUT} | Output Frequency | | | 100 / 125 | | MHz |
| $\Phi_{NOISE-100M}$ | Phase Noise Performance at 100 MHz | @ 100 Hz offset from carrier | | -101 | | dBc/Hz |
| | | @ 1 kHz offset from carrier | | -123 | | |
| | | @ 10 kHz offset from carrier | | -133 | | |
| | | @ 100 kHz offset from carrier | | -136 | | |
| | | @ 1 MHz offset from carrier | | -141 | | |
| | | @ 10 MHz offset from carrier | | -155 | | |
| $\Phi_{NOISE-125M}$ | Phase Noise Performance at 125 MHz | @ 100 Hz offset from carrier | | -98 | | dBc/Hz |
| | | @ 1 kHz offset from carrier | | -117 | | |
| | | @ 10 kHz offset from carrier | | -130 | | |
| | | @ 100 kHz offset from carrier | | -133 | | |
| | | @ 1 MHz offset from carrier | | -141 | | |
| | | @ 10 MHz offset from carrier | | -154 | | |
| $t_{JIT(\Phi)-100M}$ | RMS Phase Jitter at 100 MHz Clock | Integration Range 1.875 MHz to 20 MHz | | 0.2 | | ps |
| | | Integration Range 12 kHz to 20 MHz | | 0.4 | | |
| $t_{JIT(\Phi)-125M}$ | RMS Phase Jitter at 125 MHz Clock | Integration Range 1.875 MHz to 20 MHz | | 0.2 | | ps |
| | | Integration Range 12 kHz to 20 MHz | | 0.4 | | |
| $t_{JITTER-100M}$ | Peak Cycle-to-Cycle Jitter | Measured at 100 MHz over 10000 cycles | | 20 | | ps |
| $t_{JITTER-125M}$ | Peak Cycle-to-Cycle Jitter | Measured at 100 MHz over 10000 cycles | | 20 | | ps |
| t_R / t_F | Rise / Fall Time @ 100 MHz and 125 MHz | Measured differentially between -150 mV to 150 mV with 2 pF Load, Figure 11 | 0.6 | | 4.0 | V/ns |
| $\Delta t_R / t_F$ | Output Rise/ Fall time variation | | | | 125 | ps |
| t_{SKEW} | Within device output to output skew | | | | 40 | ps |
| t_{OE} | Output enable/disable time (Note 13) | Measured at cross point | | 10 | | μs |
| t_{DC} | Output Clock Duty Cycle | $V_{DD} = 3.3 \text{ V}$ | 45 | 50 | 55 | % |
| t_{PU} | Stabilization time from Power-up | | | 3.0 | | mS |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

12. Measurement taken from differential output on single-ended channel terminated with $R_S = 33.2 \Omega$, $R_L = 49.9 \Omega$, with test load capacitance of 2 pF and current biasing resistor set at $R_{REF} = 475 \Omega$. See Figure 9. Guaranteed by characterization.

13. Output pins are tri-stated when OE is asserted LOW. Output pins are driven differentially when OE is HIGH unless device is in power down mode, $\overline{PD} = \text{Low}$.

Table 10. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS

$V_{DD} = 3.3\text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C , $f_{OUT} = 100\text{ MHz}$, 125 MHz

| Symbol | Parameter | Test Condition | Min | Typ | Max | PCIe Industry Spec | Unit |
|---------------------------------------|---|--|-------|------|------|--------------------|------|
| t_j (PCIe Gen 1) | Phase Jitter Peak-to-Peak (Notes 15 and 18) | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 100\text{ MHz}$ Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) for 10^6 clock periods | | 10 | 20 | 86 | ps |
| | | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 125\text{ MHz}$ Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) for 10^6 clock periods | | 10 | 20 | – | |
| $t_{REFCLK_HF_RMS}$ (PCIe Gen 2) | Phase Jitter RMS (Notes 16 and 18) | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 100\text{ MHz}$ Input High Band: 1.5 MHz – Nyquist (clock frequency/2) | | 1.0 | 1.8 | 3.1 | ps |
| | | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 125\text{ MHz}$ Input High Band: 1.5 MHz – Nyquist (clock frequency/2) | | 0.8 | 1.0 | – | |
| $t_{REFCLK_LF_RMS}$ (PCIe Gen 2) | Phase Jitter RMS (Notes 16 and 18) | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 100\text{ MHz}$ Input Low Band: 10 kHz – 1.5 MHz | | 0.10 | 0.15 | 3.0 | ps |
| | | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 125\text{ MHz}$ Input Low Band: 10 kHz – 1.5 MHz | | 0.08 | 0.15 | – | |
| t_{REFCLK_RMS} (PCIe Gen 3) | Phase Jitter RMS (Notes 17 and 18) | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 100\text{ MHz}$ Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | | 0.35 | 0.70 | 0.8 | ps |
| | | $f_{CLKIN} = 25\text{ MHz}$ Crystal, $f_{CLKOUT} = 125\text{ MHz}$ Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | | 0.17 | 0.22 | – | |
| t_{REFCLK_RMS} (PCIe Gen 4) | Phase Jitter RMS (Notes 17 and 18) | $f = 100\text{ MHz}$, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | SSOFF | 0.35 | 0.5 | 0.5 | ps |

14. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
15. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86 ps peak-to-peak for a sample size of 10^6 clock periods.
16. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1 ps RMS for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0 ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band).
17. RMS jitter after applying system transfer function for the common clock architecture.
18. Measurement taken from differential output on single-ended channel terminated with $R_S = 33.2\ \Omega$, $R_L = 49.9\ \Omega$, with test load capacitance of 2 pF and current biasing resistor set at $R_{REF} = 475\ \Omega$. See Figure 9. This parameter is guaranteed by characterization. Not tested in production.

NB3N51044

PHASE NOISE

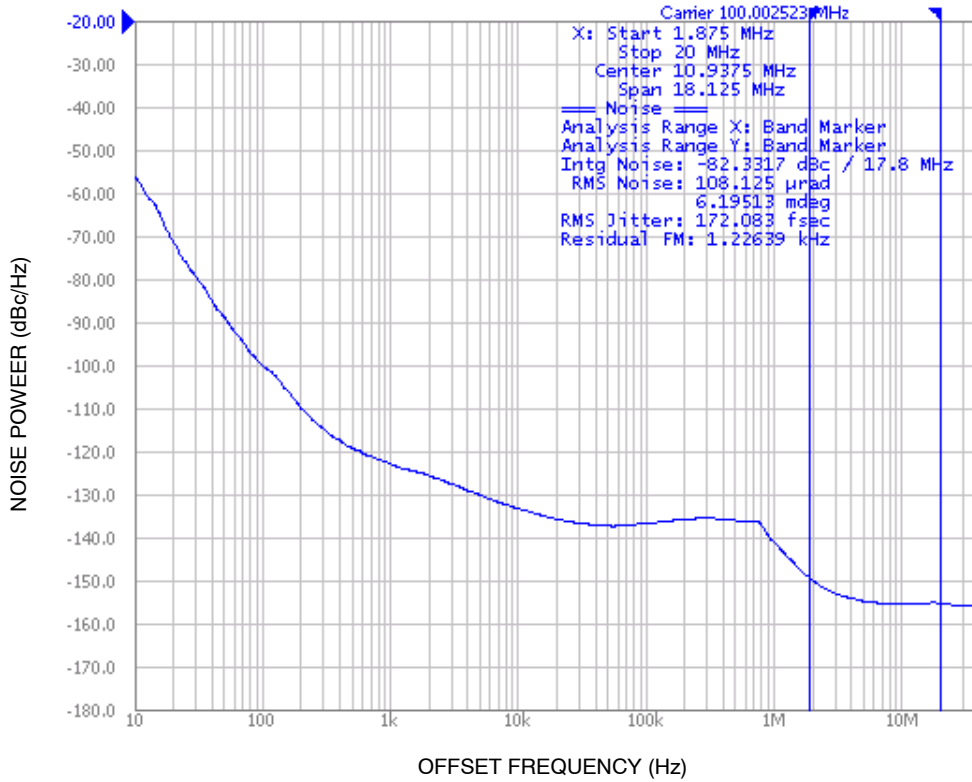


Figure 3. Typical Phase Noise Plot at 100 MHz ($f_{CLKIN} = 25$ MHz Crystal , $f_{CLKOUT} = 100$ MHz, RMS Phase Jitter = 172 fs for Integration Range of 1.875 MHz to 20 MHz, Output Termination = HCSL type)

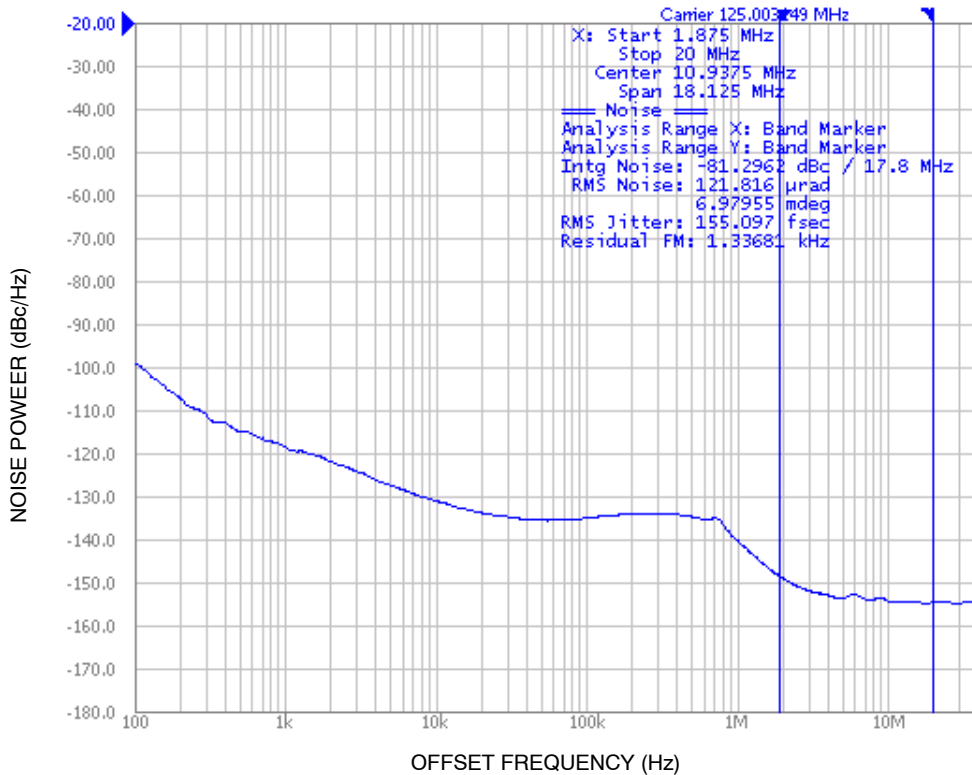


Figure 4. Typical Phase Noise Plot at 125 MHz ($f_{CLKIN} = 25$ MHz Crystal , $f_{CLKOUT} = 125$ MHz, RMS Phase Jitter = 155 fs for Integration Range of 1.875 MHz to 20 MHz, Output Termination = HCSL type)

PHASE NOISE

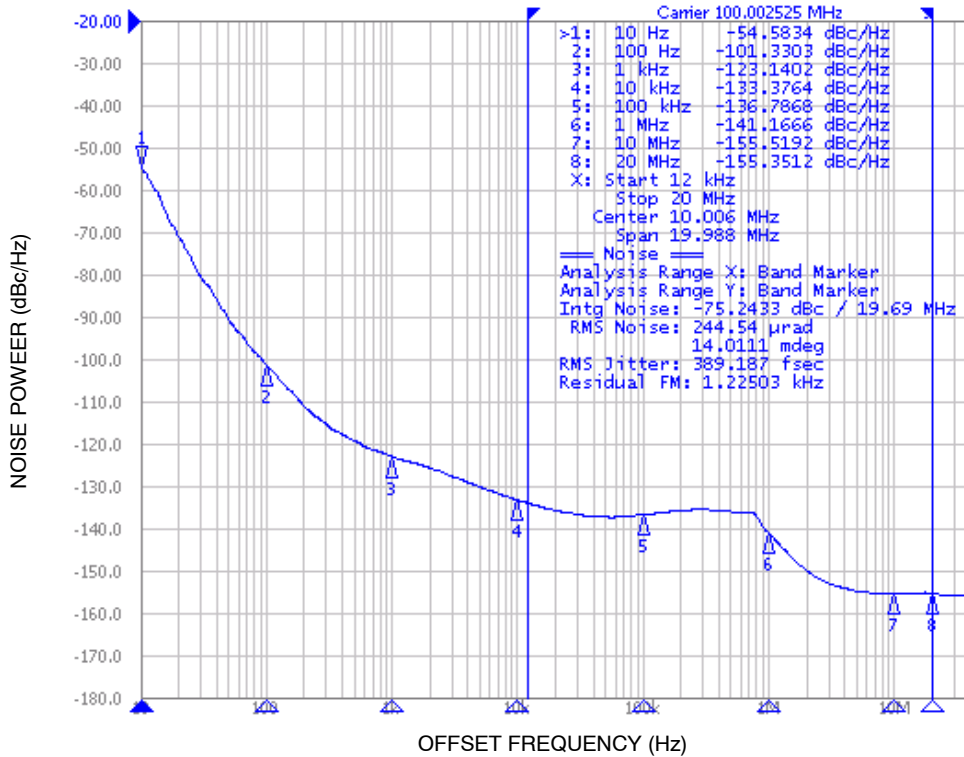


Figure 5. Typical Phase Noise Plot at 100 MHz ($f_{CLKIN} = 25$ MHz Crystal , $f_{CLKOUT} = 100$ MHz, RMS Phase Jitter = 389 fs for Integration Range of 12 kHz to 20 MHz, Output Termination = HCSL type)

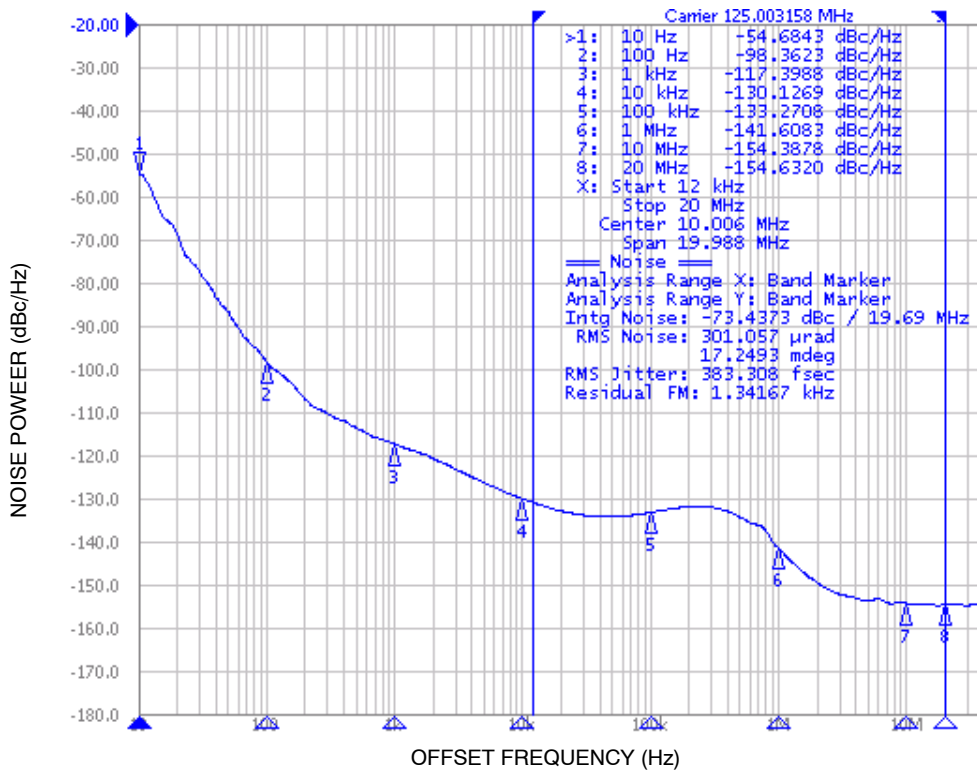


Figure 6. Typical Phase Noise Plot at 125 MHz ($f_{CLKIN} = 25$ MHz Crystal , $f_{CLKOUT} = 125$ MHz, RMS Phase Jitter = 383 fs for Integration Range of 12 kHz to 20 MHz, Output Termination = HCSL type)

APPLICATION INFORMATION

Crystal Input Interface

Figure 7 shows the NB3N51044 device crystal oscillator interface using a typical parallel resonant crystal. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors, C_1 and C_2 , need to consider the stray capacitances of the board and are used to match the nominally required crystal load capacitance C_L . A parallel crystal with loading capacitance $C_L = 18 \text{ pF}$ would use $C_1 = 26 \text{ pF}$ and $C_2 = 26 \text{ pF}$

as nominal values, assuming approximately 2 pF of stray capacitance per trace and approximately 8 pF of internal capacitance.

$$C_L = (C_1 + C_{\text{stray}} + C_{\text{in}}) / 2; C_1 = C_2$$

The frequency accuracy and duty cycle skew can be fine-tuned by adjusting the C_1 and C_2 values. For example, increasing the C_1 and C_2 values will reduce the operational frequency.

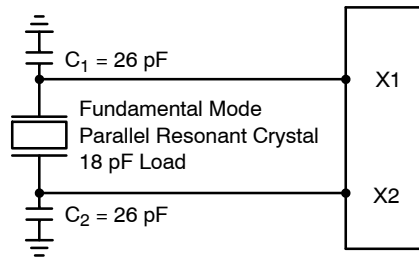


Figure 7. Crystal Interface Loading

Power Supply Filter

In order to isolate the NB3N51044 from system power supply, noise decoupling is required. The 10 μF and a 0.1 μF cap from supply pins to GND decoupling capacitor has to be connected between V_{DD} (pins 3, 8, 14, 24 and 28) and GND (pins 4, 13 and 19). It is recommended to place decoupling

capacitors as close as possible to the device to minimize lead inductance.

Termination

The output buffer structure is shown in the Figure 8.

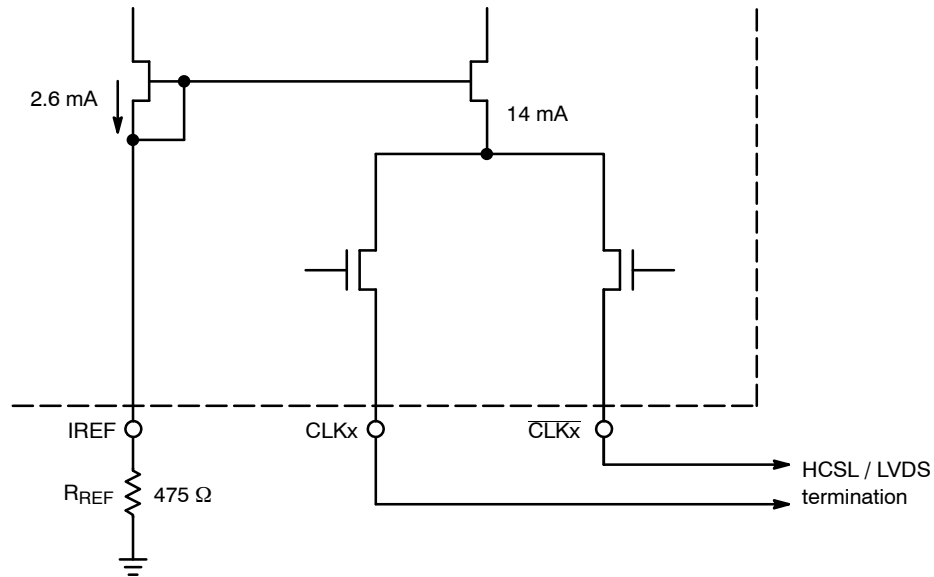


Figure 8. Simplified Output Structure

NB3N51044

The outputs can be terminated to drive HCSL receiver (see Figure 9) or LVDS receiver (see Figure 10). HCSL output interface requires $49.9\ \Omega$ termination resistors to GND for generating the output levels. LVDS output

interface may not require the $100\ \Omega$ near the LVDS receiver if the receiver has internal $100\ \Omega$ termination. An optional series resistor R_L may be connected to reduce the overshoots in case of impedance mismatch.

HCSL INTERFACE

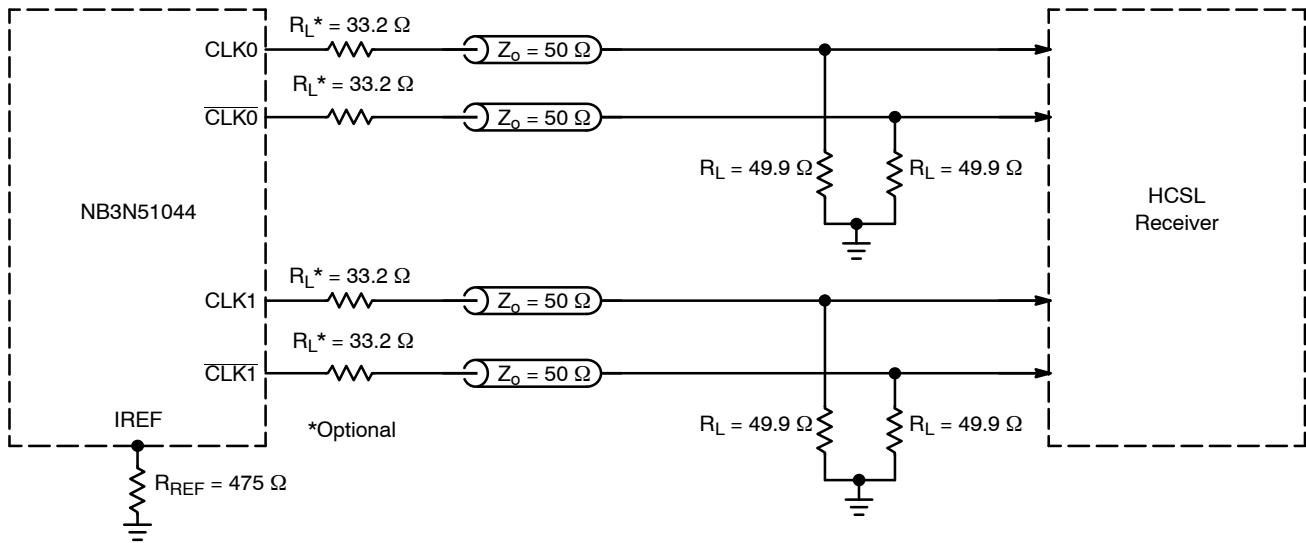


Figure 9. Typical Termination for HCSL Output Driver and Device Evaluation

LVDS COMPATIBLE INTERFACE

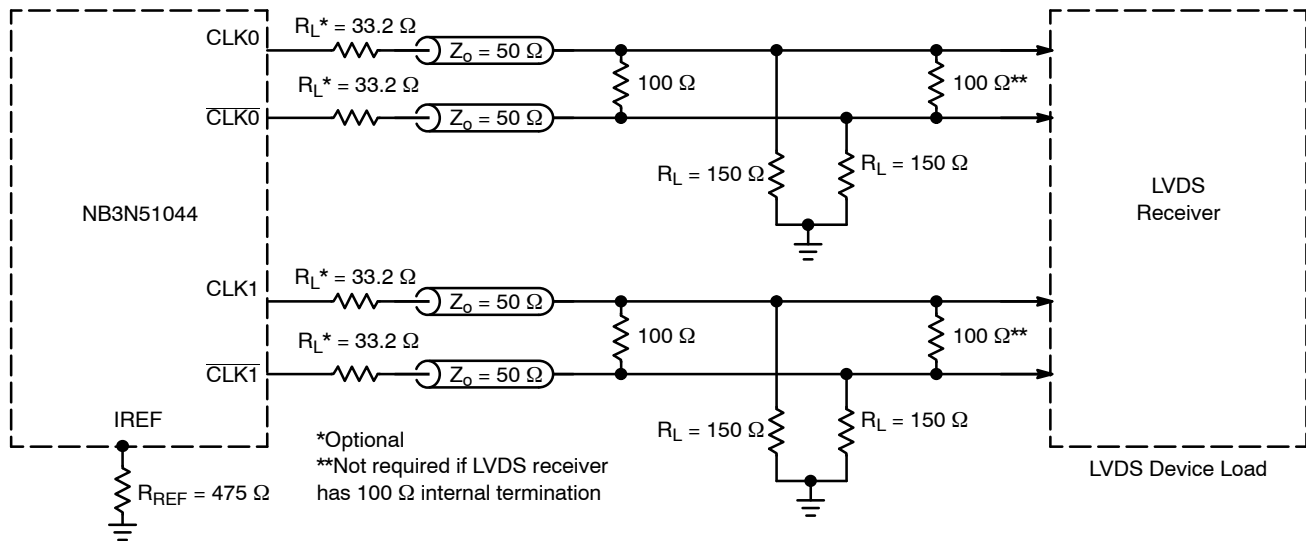


Figure 10. Typical Termination for LVDS Device Load

NB3N51044

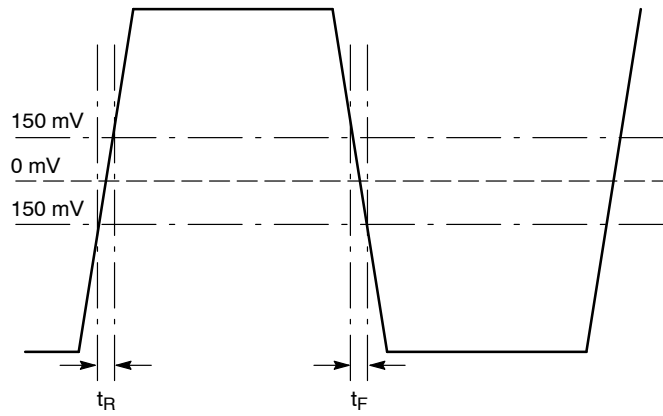


Figure 11. HCSL Differential Measurement of t_R/t_F

ORDERING INFORMATION

| Device | Temperature | Package | Shipping† |
|----------------|---------------|-----------------------|--------------------|
| NB3N51044DTR2G | -40°C to 85°C | TSSOP-28 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

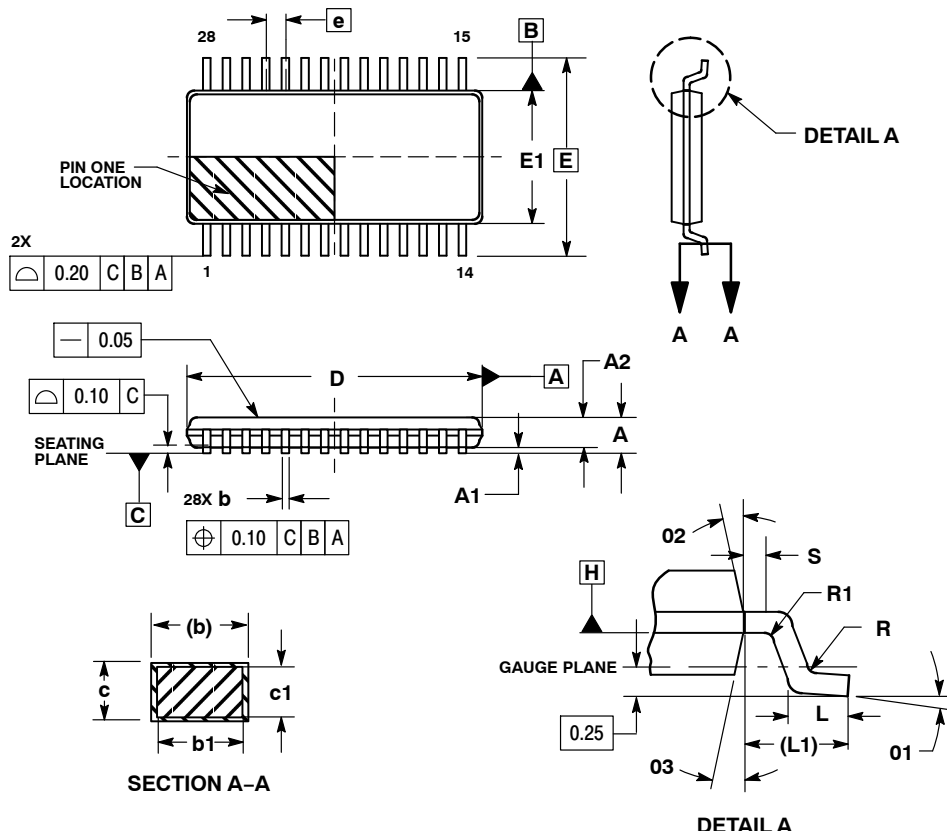
ON Semiconductor®



SCALE 1:1

TSSOP28
CASE 948AA
ISSUE A

DATE 26 OCT 2011

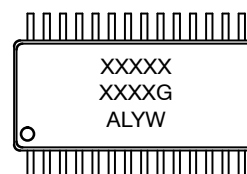


NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

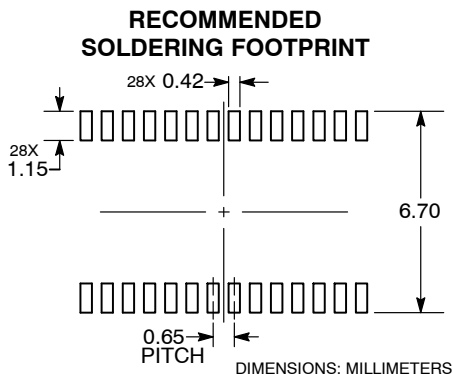
| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | --- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| b1 | 0.19 | 0.25 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 |
| D | 9.60 | 9.80 |
| E | 6.40 | BSC |
| E1 | 4.30 | 4.50 |
| e | 0.65 | BSC |
| L | 0.45 | 0.75 |
| L1 | 1.00 | REF |
| R | 0.09 | --- |
| R1 | 0.09 | --- |
| S | 0.20 | --- |
| 01 | 0° | 8° |
| 02 | 12° | REF |
| 03 | 12° | REF |

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.



| | | |
|-------------------------|--|--|
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| DESCRIPTION: | 28 LEAD TSSOP, 9.7X4.4X1.0 MM, 0.65 PITCH | PAGE 1 OF 1 |

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