

# Sinusoidal Sensorless Three-Phase Brushless DC Motor Controller and Predriver

## LV8961HUW

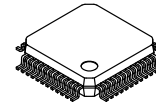
### Overview

The LV8961 is a high performance sinusoidal sensorless three-phase BLDC motor controller with predrivers for automotive applications. An integrated two-stage charge pump provides gate current for a wide range of ultra low  $R_{ds(on)}$  NFETs. The device offers a rich set of system protection and diagnostic functions such as overcurrent, overvoltage, short-circuit, undervoltage, overtemperature and many more. It supports open-loop as well as closed-loop speed control based on Back ElectroMotive Force (BEMF) observation. The user configurable startup, speed setting and proportional/integral (PI) control coefficients, make LV8961 suitable for a wide range of motor- and load combinations. With a built-in linear regulator for powering an external circuit and a watchdog timer, the LV8961 offers a very small system solution. A one-time programmable (OTP) non-volatile memory in addition to RAM and an SPI interface is provided for parameter setting and monitoring of the system status. With the operating junction temperature tolerance up to 175°C, the LV8961 is an ideal solution for stand-alone automotive and industrial BLDC motor control systems.

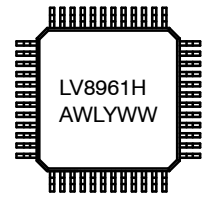
### Features

- AEC-Q100 Qualified and PPAP Capable
- Operating Junction Temperature up to 175°C
- Operating Voltage Range from 5.5 V to 28 V with Tolerance from 4.5 V to 40 V
- Embedded Proprietary Sensorless Trapezoidal and Sinusoidal Commutation
- Selectable Number of BEMF Zero-crossing Detection Window from 6, 3, 2, and 1 per Electrical Cycle
- Simple and Effective Lead Angle Adjustment Setting by Register
- Supports Open-loop as well as Closed-loop Speed Control
- Integrated Predrivers for Driving Six N-MOSFETs
- Two-stage Charge Pump for Continuous 100% Duty Cycle Operation
- 5 V / 3.3 V Regulator and Watchdog Timer Applications Using an External Microcontroller
- Configurable Speed Settings with Linear Characteristic
- PI Control Include Acceleration/Deceleration Adjustment
- Direct Access to PWM Duty and FG Cycle via SPI Interface
- Various System Protection Features Including:
  - ◆ Shoot through Protection Using Configurable Dead Time
  - ◆ Drain-source Short Detection

### MARKING DIAGRAM



SQFP48K  
CASE 131AN



- A = Assembly Site
- WL = Wafer Lot Number
- Y = Year of production, Last Number
- WW = Work Week Number
- LV8961H = Specific Device Code

### ORDERING INFORMATION

| Device       | Package              | Shipping†              |
|--------------|----------------------|------------------------|
| LV8961HUWR2G | SQFP48K<br>(Pb-Free) | 2,500 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

- ◆ Cycle-by-cycle Current Limit and Overcurrent Shutdown (Threshold Value can be Selectable by Register)
- ◆ Overvoltage and Undervoltage Shutdown
- ◆ Overtemperature Warning and Shutdown
- ◆ Input PWM Fault Detection
- ◆ Abnormal FG Cycle Monitoring
- ◆ Motor Pin Open Detection

### Typical Applications

- Pumps (Fuel, Oil, Coolant, Hydraulic Controls, Vacuum, Solar Boilers, ...)
- Fans and Blowers (HVAC, Radiator, Condenser, Battery, Inverter, Charger, ...)
- White Goods and Industrial BLDC Motor Control

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## LV8961H BLOCK DIAGRAM

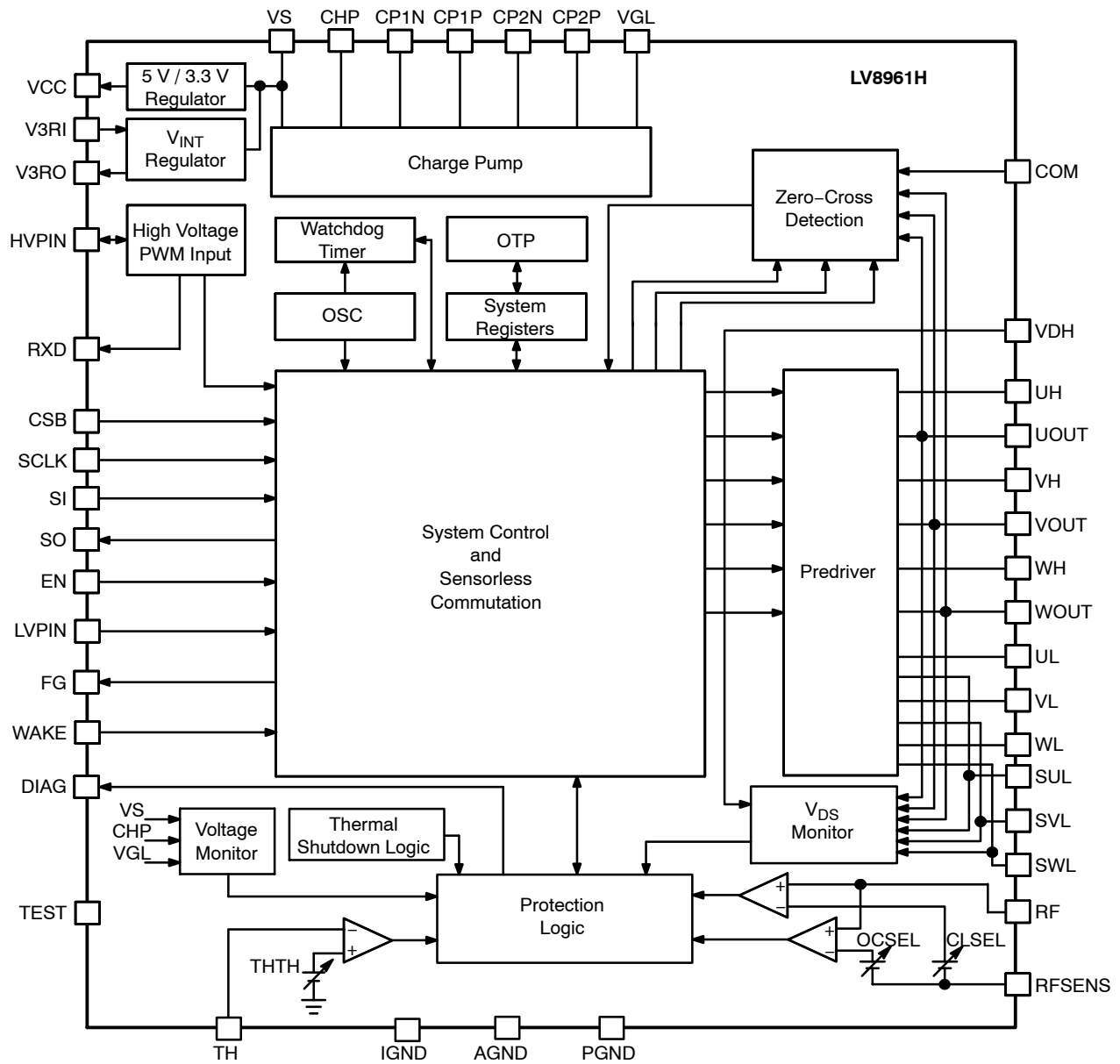


Figure 1. LV8961H Block Diagram

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## APPLICATION BLOCK DIAGRAMS

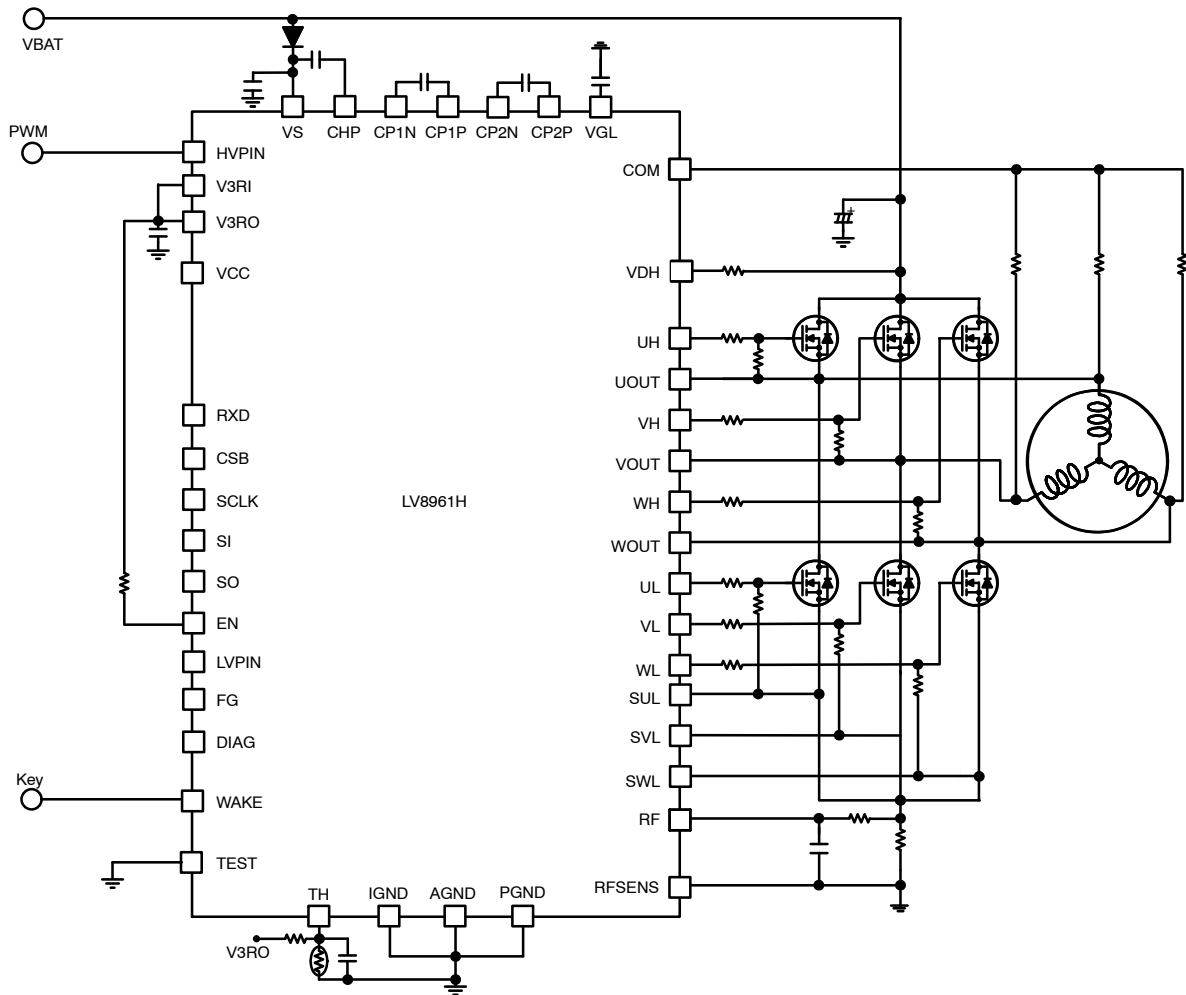


Figure 2. Example of Stand-alone Configuration

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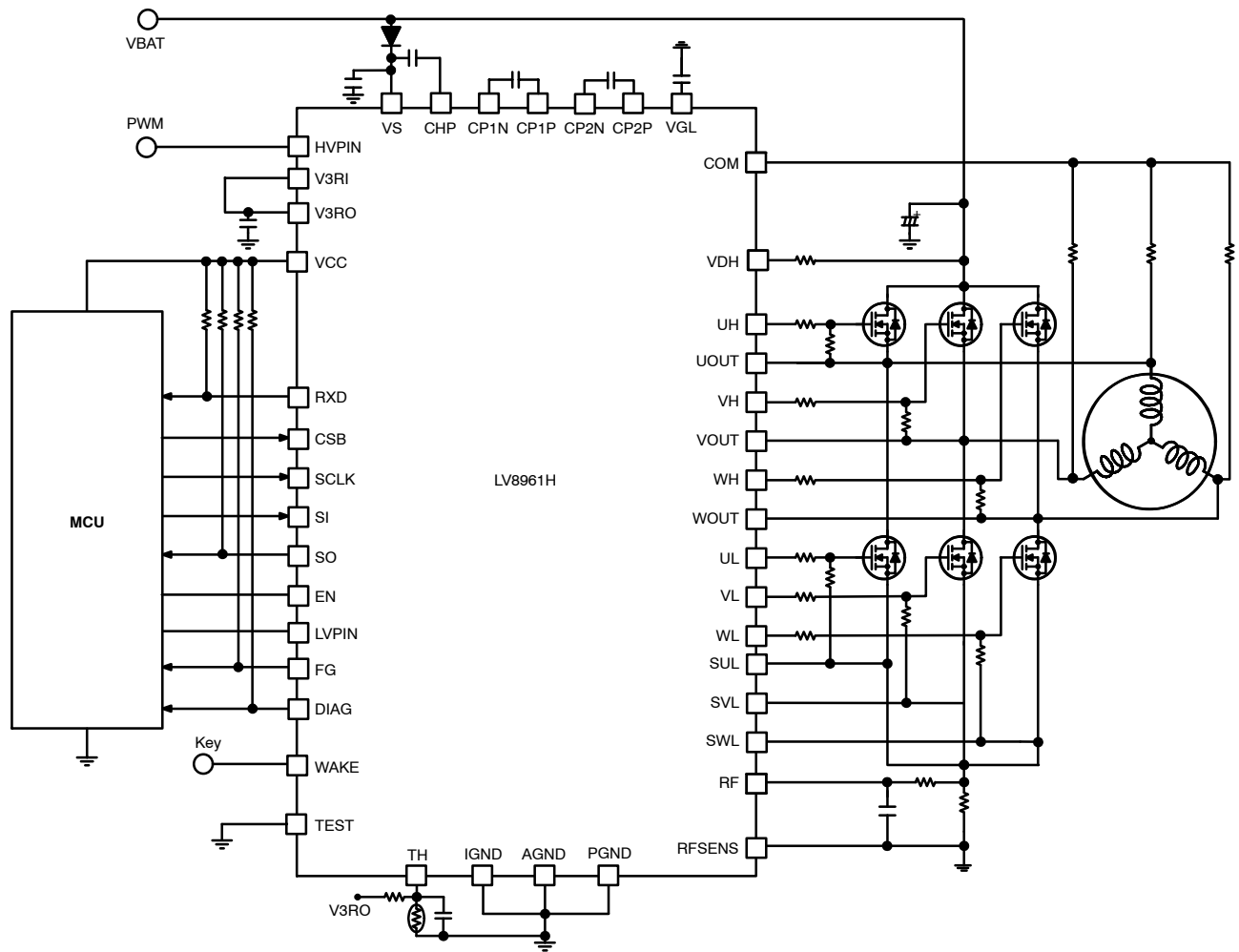


Figure 3. Example of MCU Based Control Configuration

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## PIN ASSIGNMENTS

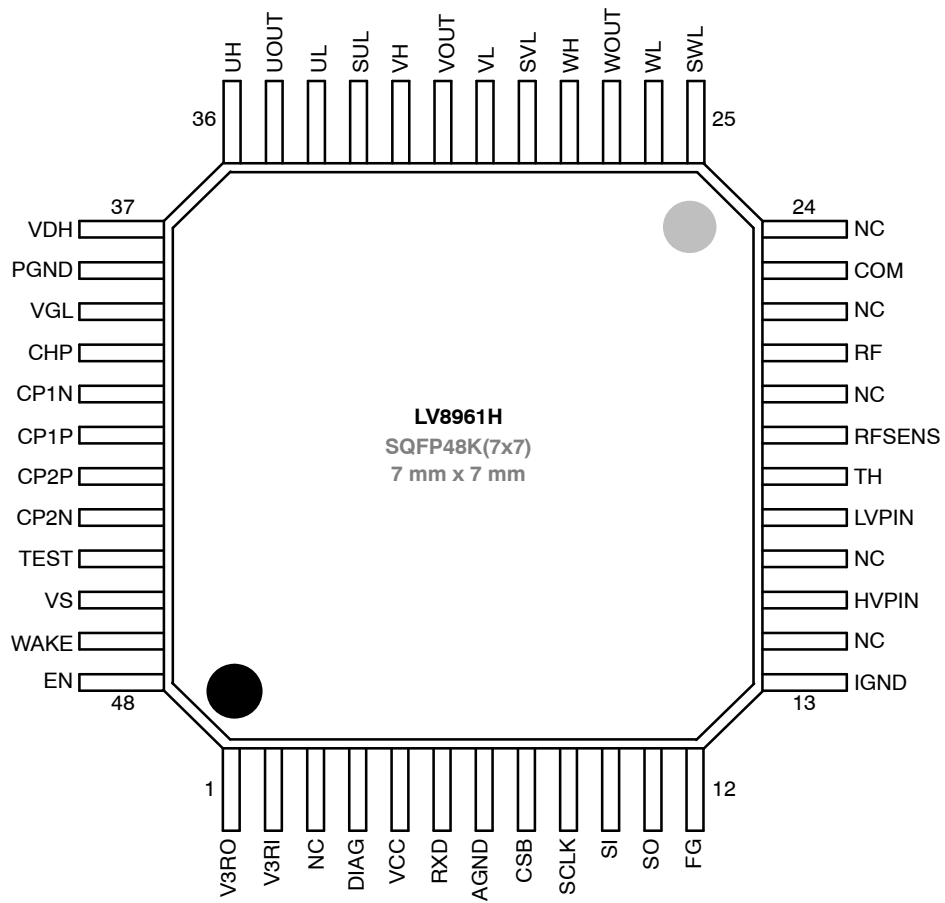


Figure 4. LV8961H Pinout

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## PIN DESCRIPTION

| Pin Name             | Pin No                   | TYPE                       | Description   | Page |
|----------------------|--------------------------|----------------------------|---|------|
| V3RO                 | 1                        | TYPE 2                     | 3 V regulator output pin. Connect capacitor between this pin and AGND   | 19   |
| V3RI                 | 2                        | TYPE 1                     | 3 V regulator input pin (internally connected to control, and logic circuits). Connect to V3RO pin  | 19   |
| NC                   | 3, 14, 16,<br>20, 22, 24 |                            | No Connections  |      |
| DIAG                 | 4                        | TYPE 4                     | Programmable open drain diagnostic output   | 21   |
| VCC                  | 5                        | TYPE 2                     | 5 V or 3.3 V regulator output pin. (Selected by internal register setting) Power supply for microcontroller. Connect capacitor to AGND for stability  | 19   |
| RXD                  | 6                        | TYPE 4                     | Open drain logic level output of HVPIN received data. Use pull-up to a voltage less than or equal to VS   | 21   |
| AGND                 | 7                        |                            | Analog GND pin  |      |
| CSB                  | 8                        | TYPE 5                     | Active low SPI interface chip selection pin   | 26   |
| SCLK                 | 9                        | TYPE 3                     | SPI interface clock input pin   | 26   |
| SI                   | 10                       | TYPE 3                     | Active high SPI interface serial data input pin   | 26   |
| SO                   | 11                       | TYPE 4                     | Open drain SPI interface serial data output pin   | 26   |
| FG                   | 12                       | TYPE 4                     | Open drain BEMF transition output pin. The frequency division ratio is selectable via register settings   | 21   |
| IGND                 | 13                       | TYPE 12                    | HV PWSMIN Block GND pin. Must be connected to AGND on the PCB   |      |
| HVPIN                | 15                       | TYPE 12                    | High voltage PWM input with a $V_{VS}/2$ threshold  | 21   |
| LVPIN                | 17                       | TYPE 3                     | Digital level PWM input pin for direct drive or speed register selection details. Input polarity can be programmed for either active high or active low   | 21   |
| TH                   | 18                       | TYPE 1                     | Thermistor input pin for power stage temperature detection. If the input voltage is below the threshold voltage, an error is triggered. The error threshold is programmable. To disable tie to V3RO | 23   |
| RFSENS               | 19                       | TYPE 13                    | Shunt resistance reference pin. Connect this pin to the GND side of the Shunt resistor with Kelvin leads  | 22   |
| RF                   | 21                       | TYPE 13                    | Output current detect pin. Connect this pin to higher terminal of the shunt resistor with Kelvin leads  | 22   |
| COM                  | 23                       | TYPE 9                     | COM input pin. Connect this pin to the motor neutral point if available. This point may be derived from a resistive network with 1 k resistors to the phases  | 15   |
| SWL<br>SVL<br>SUL    | 25<br>29<br>33           | TYPE 8<br>TYPE 8<br>TYPE 8 | Current return path for low-side predriver. Short-circuit shutoff level is measured between this pin and its corresponding phase pin  | 21   |
| WL<br>VL<br>UL       | 26<br>30<br>34           | TYPE 8<br>TYPE 8<br>TYPE 8 | Predriver output pin for the low-side NFET. Use gate resistors for wave-shaping   | 21   |
| WOUT<br>VOUT<br>UOUT | 27<br>31<br>35           | TYPE 7<br>TYPE 7<br>TYPE 7 | Current return path for high-side predriver and reference for high-side short-circuit shutoff   | 21   |
| WH<br>VH<br>UH       | 28<br>32<br>36           | TYPE 7<br>TYPE 7<br>TYPE 7 | Predriver output pin for the high-side NFET. Use gate resistors for wave-shaping  | 21   |
| VDH                  | 37                       | TYPE 14                    | Sense input for supply voltage and short-circuit detection of high-side power Fets. Connect through 100 $\Omega$ resistor to common drain of the power bridge                                       | 21   |
| PGND                 | 38                       | TYPE 10,<br>11             | GND pin for the charge pump   |      |
| VGL                  | 39                       | TYPE 10                    | Power supply pin for low-side predriver. Connect decoupling capacitor between this pin and GND  | 19   |
| CHP                  | 40                       | TYPE 11                    | Power supply pin for high-side predriver. Connect decoupling capacitor between this pin and VS  | 19   |

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## PIN DESCRIPTION (continued)

| Pin Name | Pin No | TYPE    | Description  | Page |
|----------|--------|---------|--|------|
| CP1N     | 41     | TYPE 10 | Charge transfer pin of the Charge pump (1N). Connect capacitor between CP1P and CP1N   | 19   |
| CP1P     | 42     | TYPE 10 | Charge transfer pin of the Charge pump (1P). Connect capacitor between CP1P and CP1N   | 19   |
| CP2P     | 43     | TYPE 11 | Charge transfer pin of the Charge pump (2P). Connect capacitor between CP2P and CP2N   | 19   |
| CP2N     | 44     | TYPE 11 | Charge transfer pin of the Charge pump (2N). Connect capacitor between CP2P and CP2N   | 19   |
| TEST     | 45     | TYPE 15 | Factory test pin. Connect to GND   |      |
| VS       | 46     |         | Power supply pin   |      |
| WAKE     | 47     | TYPE 6  | WAKE pin. "H" = Operating mode, "L" or "Open" = Sleep mode. In Sleep mode all predrivers are high impedance. To protect the power stage, pull-down resistors on the gate lines may be required | 18   |
| EN       | 48     | TYPE 3  | Motor stage Enable pin. "H" = Normal enabled mode; "L" or "Open" = Standby mode. In Standby mode all predrivers are driven low. Motor freewheeling   | 18   |

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## PIN CIRCUIT

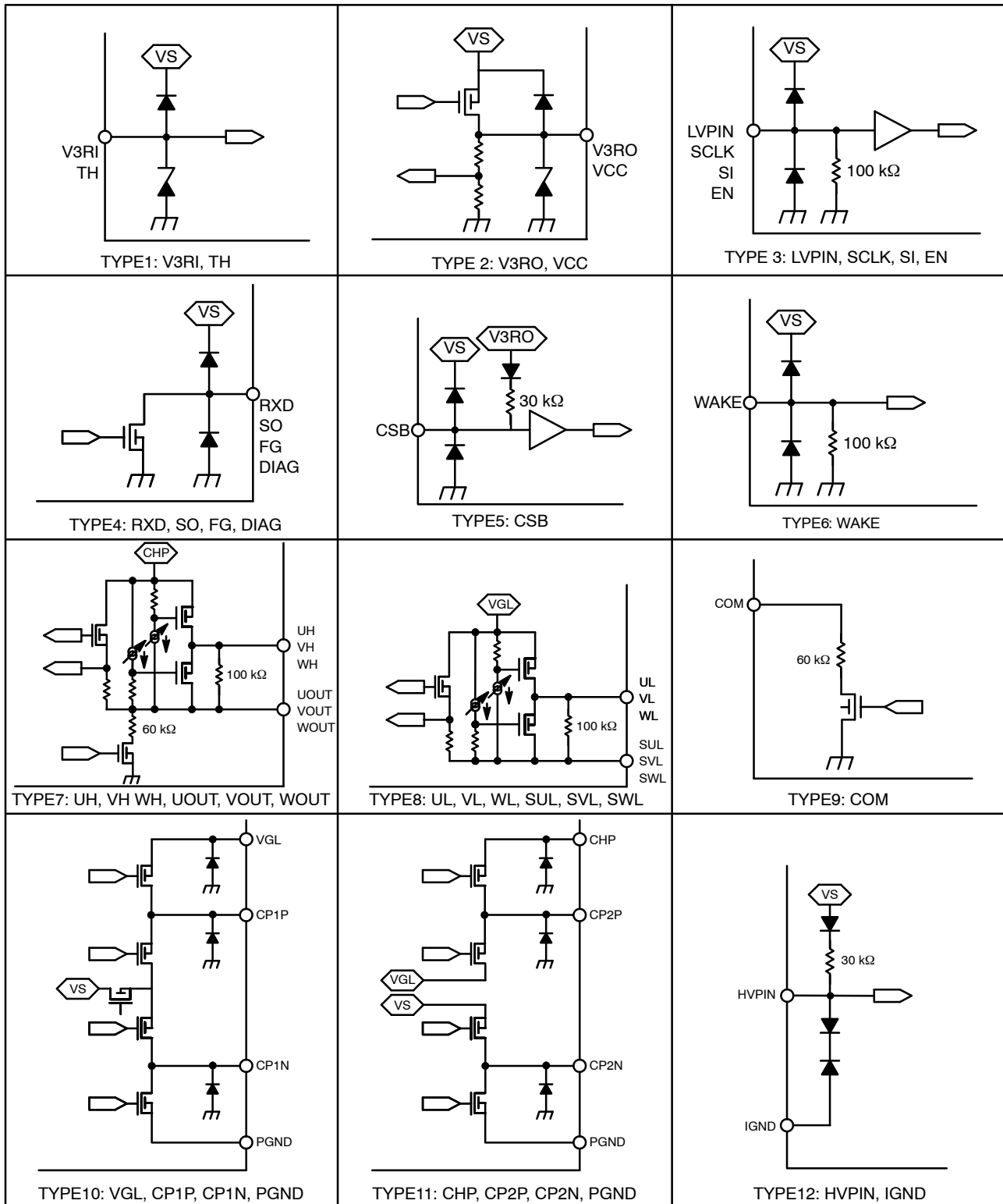


Figure 5. Pin Circuit



PIN CIRCUIT (continued)

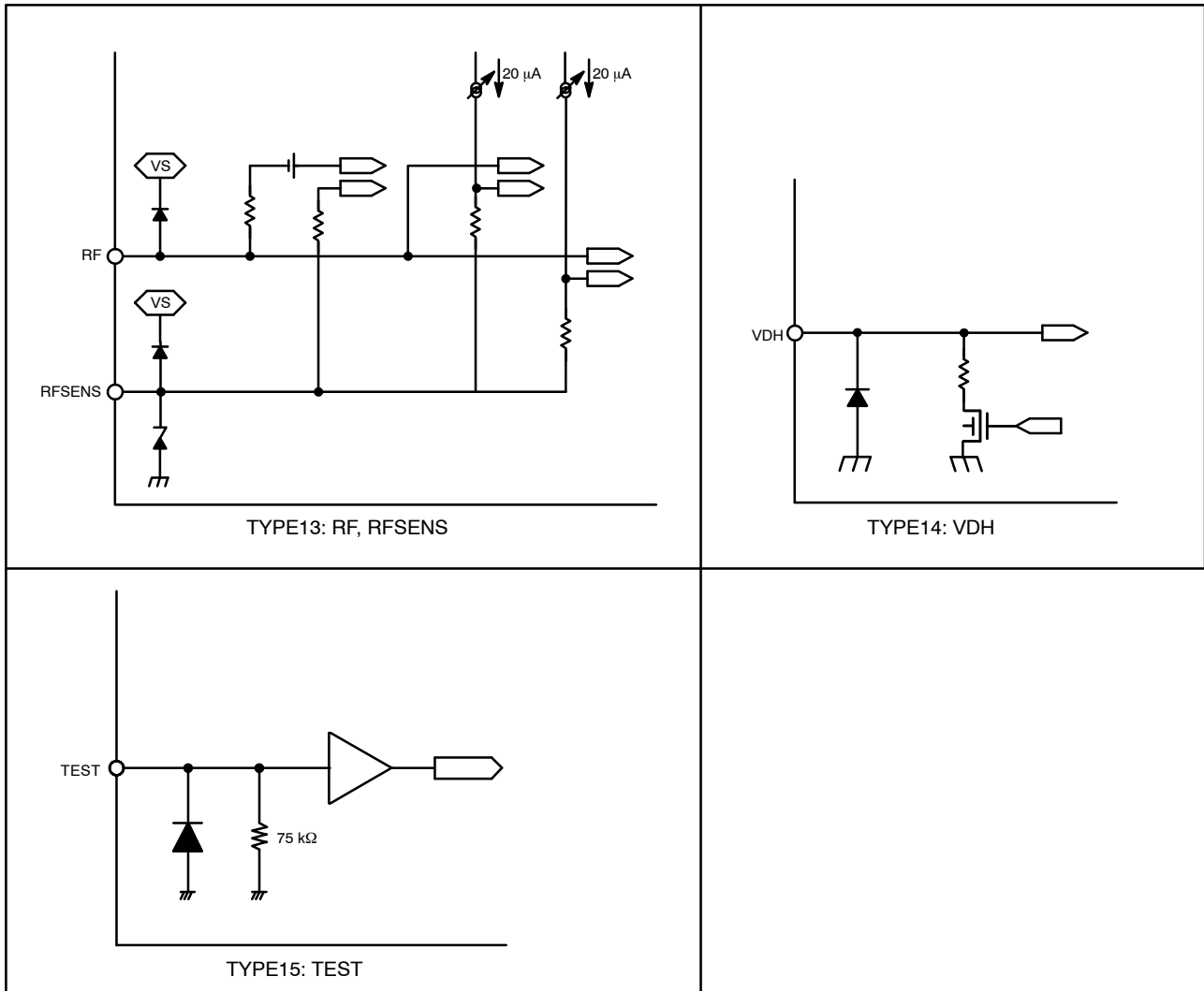


Figure 6. Pin Circuit (continued)

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## ABSOLUTE MAXIMUM RATINGS

| Parameter                              | Pins                                       | Ratings     | Unit |
|--|--|-------------|------|
| Supply Voltage                         | VS   | -0.3 to 40  | V    |
| Sense Input for Supply Voltage         | VDH  | -0.3 to 40  | V    |
| Charge Pump Voltage (High Side)        | CHP  | -0.3 to 40  | V    |
| Charge Pump Voltage (Low Side)         | VGL  | -0.3 to 16  | V    |
| Logic Power Supply                     | VR3I, VR3O                                 | -0.3 to 3.6 | V    |
| 5 V Regulator Voltage                  | VCC  | -0.3 to 5.5 | V    |
| Digital I/O Voltage1                   | WAKE, EN                                   | -0.3 to 40  | V    |
| Digital I/O Voltage2                   | CSB, SCLK, SI, LVPIN, TEST                 | -0.3 to 5.5 | V    |
| Digital Output Voltage                 | DIAG, FG, SO, RXD                          | -0.3 to 40  | V    |
| High Voltage PWMIN Voltage             | HVPIN                                      | -10 to 40   | V    |
| RF Input Voltage                       | RF   | -3 to 3.6   | V    |
| RFSENS Input Voltage                   | RFSENS                                     | -0.3 to 1.0 | V    |
| TH Input Voltage                       | TH   | -0.3 to 3.6 | V    |
| Voltage Tolerance                      | UOUT, VOUT, WOUT, COM                      | -3 to 40    | V    |
| High-side Output                       | UH, VH, WH                                 | -3 to 40    | V    |
| Low-side Output                        | UL, VL, WL                                 | -3 to 16    | V    |
| Low-side Source Output Voltage         | SUL, SVL, SWL                              | -3 to 3.6   | V    |
| Voltage between HS Gate and Phase      | UH-UOUT, VH-VOUT, WH-WOUT                  | -0.3 to 40  | V    |
| Voltage between LS Gate and Source     | UL-SUL, VL-SVL, WL-SWL                     | -0.3 to 16  | V    |
| Output Current                         | UH, VH, WH, UL, VL, WL<br>pulsed (duty 5%) | 50<br>400   | mA   |
| Open Drain Output Current              | DIAG, FG, SO, RXD                          | 10          | mA   |
| Thermal Resistance (R <sub>θJA</sub> ) | with Board (Note 1)                        | 47          | °C/W |
| ESD Human Body Model                   | AEC Q100-002                               | 2           | kV   |
| ESD Charged Device Model               | AEC Q100-011                               | 750         | V    |
| Storage Temperature                    |  | -55 to 150  | °C   |
| Junction Temperature                   |  | -40 to 150  | °C   |
|  | (Note 2)                                   | 150 to 175  | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 76.2 × 114.3 × 1.6 mm, glass epoxy board.
- Operation outside the Operating Junction temperature is not guaranteed. Operation above 150°C should not be considered without a written agreement from **onsemi** Engineering staff.

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## ELECTRICAL CHARACTERISTICS

(Valid at a junction temperature range from  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , for supply Voltage  $6.0\text{ V} \leq \text{VS} \leq 28\text{ V}$ . Typical values at  $25^{\circ}\text{C}$  and  $\text{VS} = 12\text{ V}$  unless specified otherwise)

| Parameter                        | Symbol   | Condition                                     | Min | Typ | Max | Unit               |
|----------------------------------|----------|---|-----|-----|-----|--------------------|
| Supply-voltage Range             | VS       | Normal mode                                   | 6   | 12  | 28  | V                  |
|                                  |          | Device fully functional                       | 5.5 | -   | 28  | V                  |
|                                  |          | Full logic functionality,<br>driver stage off | 4.5 | -   | 40  | V                  |
| Supply Current into VS           | $I_{s1}$ | V3RO = V3RI<br>EN = L                         | -   | 15  | 25  | mA                 |
|                                  | $I_{s2}$ | Sleep Mode                                    | -   | 40  | 80  | $\mu\text{A}$      |
| Operational junction Temperature | Topj     |   | -40 | -   | 150 | $^{\circ}\text{C}$ |

### OUTPUT BLOCK (UH, VH, WH, UL, VL, WL)

|                                  |         |                                |   |    |    |          |
|----------------------------------|---------|--------------------------------|---|----|----|----------|
| Low-side Output On-resistance 1  | RON(L1) | "L" level $I_o = 10\text{mA}$  | - | 6  | 15 | $\Omega$ |
| Low-side Output On-resistance 2  | RON(L2) | "H" level $I_o = -10\text{mA}$ | - | 12 | 22 | $\Omega$ |
| High-side Output On-resistance 1 | RON(H1) | "L" level $I_o = 10\text{mA}$  | - | 6  | 15 | $\Omega$ |
| High-side Output On-resistance 2 | RON(H2) | "H" level $I_o = -10\text{mA}$ | - | 12 | 22 | $\Omega$ |

### DRIVE OUTPUT BLOCK (PWM BLOCK)

|                                  |                        |          |      |      |      |     |
|----------------------------------|------------------------|----------|------|------|------|-----|
| Drive Output PWM Frequency       | fPWMO                  |          | 18.5 | 19.5 | 20.5 | kHz |
| Output PWM Duty Cycle Resolution | $\Delta\text{PWMDUTY}$ | (Note 3) | -    | -    | 0.1  | %   |

### 3 V CONSTANT VOLTAGE OUTPUT

|                    |                       |                                     |       |     |       |    |
|--------------------|-----------------------|-------------------------------------|-------|-----|-------|----|
| Output Voltage     | V3RO                  |                                     | 3.135 | 3.3 | 3.465 | V  |
| Voltage Regulation | $\Delta\text{V3R1}$   | VS = 6.0 to 28 V                    | -     | -   | 50    | mV |
| Load Regulation    | $\Delta\text{V3REG2}$ | $I_o = 5\text{ mA to }25\text{ mA}$ | -     | -   | 50    | mV |
| Current Limit      | IV3RO                 | Not for external loads > 5 mA       | 50    | -   | -     | mA |

### VCC 5 V CONSTANT VOLTAGE OUTPUT

|                    |                      |                                     |      |      |      |    |
|--------------------|----------------------|-------------------------------------|------|------|------|----|
| Output Voltage     | VC5RO                | VS = 6.0 to 28 V                    | 4.75 | 5.00 | 5.25 | V  |
| Voltage Regulation | $\Delta\text{VC5R1}$ | VS = 6.0 to 28 V                    | -    | -    | 50   | mV |
| Load Regulation    | $\Delta\text{VC5R2}$ | $I_o = 5\text{ mA to }25\text{ mA}$ | -    | -    | 50   | mV |
| Current Limit      | IVCC5V               |                                     | 50   | -    | -    | mA |

### VCC 3 V CONSTANT VOLTAGE OUTPUT

|                    |                      |                                     |       |     |       |    |
|--------------------|----------------------|-------------------------------------|-------|-----|-------|----|
| Output Voltage     | VC3RO                |                                     | 3.135 | 3.3 | 3.465 | V  |
| Voltage Regulation | $\Delta\text{VC3R1}$ | VS = 6.0 to 28 V                    | -     | -   | 50    | mV |
| Load Regulation    | $\Delta\text{VC3R2}$ | $I_o = 5\text{ mA to }25\text{ mA}$ | -     | -   | 50    | mV |
| Current Limit      | IVCC3V3              |                                     | 50    | -   | -     | mA |

### LOW-SIDE GATE VOLTAGE OUTPUT (VGL PIN)

|                          |       |   |      |      |      |   |
|--------------------------|-------|---|------|------|------|---|
| Low-side Output Voltage1 | VGLH1 | $6.0 < \text{VS} \leq 8.0\text{ V}$ $I_o = -10\text{ mA}$ | 8.0  | 12.0 | 14.0 | V |
| Low-side Output Voltage2 | VGLH2 | $8.0 < \text{VS} \leq 20\text{ V}$ $I_o = -10\text{ mA}$  | 10.0 | 12.0 | 14.0 | V |
| Low-side Output Voltage3 | VGLH3 | $20 < \text{VS} \leq 28\text{ V}$ $I_o = -10\text{mA}$    | 7.0  | -    | -    | V |

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## ELECTRICAL CHARACTERISTICS (continued)

(Valid at a junction temperature range from  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , for supply Voltage  $6.0\text{ V} \leq \text{VS} \leq 28\text{ V}$ . Typical values at  $25^{\circ}\text{C}$  and  $\text{VS} = 12\text{ V}$  unless specified otherwise)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------|--------|-----------|-----|-----|-----|------|
|-----------|--------|-----------|-----|-----|-----|------|

### HIGH-SIDE OUTPUT VOLTAGE (CHP PIN)

|   |         |  |            |             |             |     |
|---|---------|--|------------|-------------|-------------|-----|
| Internal Charge Pump Oscillator frequency | FCP     | SSCG = 0   | 49.6       | 52.1        | 54.6        | kHz |
| Boost Voltage1                            | VGHH1   | $6.0 \leq \text{VS} \leq 8.0\text{ V}$<br>$\text{I}_o = -10\text{ mA}$ | VS<br>+6.0 | VS<br>+12.0 | VS<br>+14.0 | V   |
| Boost Voltage2                            | VGHH2   | $8.0 < \text{VS} \leq 20\text{ V}$<br>$\text{I}_o = -10\text{ mA}$     | Vs<br>+9.0 | VS<br>+12.0 | VS<br>+14.0 | V   |
| Boost Voltage3                            | VGHH3   | $20 < \text{VS} \leq 28\text{ V}$<br>$\text{I}_o = -10\text{ mA}$      | VS<br>+6.0 | -           | -           | V   |
| CHP Voltage Limit                         | VCHPLIM | VS = 28 V  | 34         | 36.5        | 38          | V   |

### PWMIN INPUT PIN IN LOW FREQUENCY MODE

|                           |         |                                |     |     |      |    |
|---------------------------|---------|--------------------------------|-----|-----|------|----|
| Input PWM Frequency Range | fLPWM   | PWMF = 0<br>Low frequency mode | 5.3 | -   | 1000 | Hz |
| PWM Signal Timeout        | TLPWMIN | PWMF = 0<br>Low frequency mode | -   | 210 | 220  | ms |

### PWMIN INPUT PIN IN HIGH FREQUENCY MODE

|                           |       |  |     |   |       |    |
|---------------------------|-------|--|-----|---|-------|----|
| Input PWM Frequency Range | fHPWM | PWMF = 1<br>High frequency mode<br>PWMINSEL=1<br>LVPIN is used for PWM input | 5.3 | - | 18500 | Hz |
|---------------------------|-------|--|-----|---|-------|----|

### DIGITAL INPUT PIN (CSB)

|                          |        |  |                          |      |                          |            |
|--------------------------|--------|--|--------------------------|------|--------------------------|------------|
| High level Input Voltage | VIH1   |  | $0.8 \times \text{V3RO}$ | -    | -                        | V          |
| Low level Input Voltage  | VIL1   |  | -                        | -    | $0.2 \times \text{V3RO}$ | V          |
| Input Hysteresis Voltage | VIHYS1 |  | 0.1                      | 0.35 | $0.6 \times \text{V3RO}$ | V          |
| Pull-up Resistance       | RDVI1  |  | 15                       | 30   | 60                       | k $\Omega$ |

### DIGITAL INPUT PIN (SCLK, SI, LVPIN)

|                          |        |  |                          |      |                          |            |
|--------------------------|--------|--|--------------------------|------|--------------------------|------------|
| High level Input Voltage | VIH2   |  | $0.8 \times \text{V3RO}$ | -    | -                        | V          |
| Low level Input Voltage  | VIL2   |  | -                        | -    | $0.2 \times \text{V3RO}$ | V          |
| Input Hysteresis Voltage | VIHYS2 |  | 0.1                      | 0.35 | $0.6 \times \text{V3RO}$ | V          |
| Pull-down Resistance     | RDVI2  |  | 50                       | 100  | 200                      | k $\Omega$ |

### WAKE INPUT PIN

|                               |       |  |     |     |     |            |
|-------------------------------|-------|--|-----|-----|-----|------------|
| High level Input Voltage      | VIH3  |  | 2.5 | -   | -   | V          |
| Low level Input Voltage       | VIL3  |  | -   | -   | 0.6 | V          |
| Internal Pull-down Resistance | RDVI3 |  | 50  | 100 | 200 | k $\Omega$ |

### EN INPUT PIN

|                          |        |  |                          |      |                          |            |
|--------------------------|--------|--|--------------------------|------|--------------------------|------------|
| High level Input Voltage | VIH4   |  | $0.8 \times \text{V3RO}$ | -    | -                        | V          |
| Low level Input Voltage  | VIL4   |  | -                        | -    | $0.2 \times \text{V3RO}$ | V          |
| Input Hysteresis Voltage | VIHYS4 |  | 0.1                      | 0.35 | $0.6 \times \text{V3RO}$ | V          |
| Pull-down Resistance     | RDVI4  |  | 50                       | 100  | 200                      | k $\Omega$ |

### TEST INPUT PIN

|                          |        |  |                          |      |                          |            |
|--------------------------|--------|--|--------------------------|------|--------------------------|------------|
| High level Input Voltage | VIH5   |  | $0.8 \times \text{V3RO}$ |      |                          | V          |
| Low level Input Voltage  | VIL5   |  |                          |      | $0.2 \times \text{V3RO}$ | V          |
| Input Hysteresis Voltage | VIHYS5 |  | 0.1                      | 0.35 | $0.6 \times \text{V3RO}$ | V          |
| Pull-down Resistance     | RDVI5  |  | 37.5                     | 75   | 150                      | k $\Omega$ |

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## ELECTRICAL CHARACTERISTICS (continued)

(Valid at a junction temperature range from  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , for supply Voltage  $6.0\text{ V} \leq \text{VS} \leq 28\text{ V}$ . Typical values at  $25^{\circ}\text{C}$  and  $\text{VS} = 12\text{ V}$  unless specified otherwise)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------|--------|-----------|-----|-----|-----|------|
|-----------|--------|-----------|-----|-----|-----|------|

### DIGITAL OUTPUT PIN (SO, FG, DIAG, RXD)

|                        |       |                                     |   |   |     |               |
|------------------------|-------|-------------------------------------|---|---|-----|---------------|
| Output Voltage         | VOL   | $I_o = 1\text{ mA}$ pull-up current | - | - | 0.2 | V             |
| Output Leakage Current | ILOLK |                                     | - | - | 10  | $\mu\text{A}$ |

### CURRENT LIMIT / OVERCURRENT PROTECTION (RF, RFSENS)

|   |       |  |    |     |     |    |
|---|-------|--|----|-----|-----|----|
| Current Limit Voltage 1                   | VRF11 | Voltage between RF and RFSENS, CLSEL = 0   | 40 | 50  | 60  | mV |
| Current Limit Voltage 2                   | VRF12 | Voltage between RF and RFSENS, CLSEL = 1   | 90 | 100 | 110 | mV |
| Overcurrent Detection Voltage Threshold 1 | VRF21 | Voltage between RF and RFSENS, OCSEL = 00<br>The difference voltage between VRF21 and the actual current limit voltage | 15 | 25  | 35  | mV |
| Overcurrent Detection Voltage Threshold 2 | VRF22 | Voltage between RF and RFSENS, OCSEL = 01<br>The difference voltage between VRF22 and the actual current limit voltage | 40 | 50  | 60  | mV |
| Overcurrent Detection Voltage Threshold 3 | VRF23 | Voltage between RF and RFSENS, OCSEL = 10<br>The difference voltage between VRF23 and the actual current limit voltage | 65 | 75  | 85  | mV |
| Overcurrent Detection Voltage Threshold 4 | VRF24 | Voltage between RF and RFSENS, OCSEL = 11<br>The difference voltage between VRF24 and the actual current limit voltage | 90 | 100 | 110 | mV |

### EXTERNAL THERMAL PROTECTION (TH)

|                           |                              |  |         |                          |         |    |
|---------------------------|------------------------------|--|---------|--------------------------|---------|----|
| Threshold Voltage Falling | VTH0<br>VTH1<br>VTH2<br>VTH3 | THTH[1:0] = 00<br>THTH[1:0] = 01<br>THTH[1:0] = 10<br>THTH[1:0] = 11 | Typ -35 | 350<br>300<br>250<br>200 | Typ +35 | mV |
| Hysteresis Range          | VTHHYS                       |  | 25      | 50                       | 75      | mV |

### THERMAL PROTECTION

|   |                |   |            |    |   |                    |
|---|----------------|---|------------|----|---|--------------------|
| Thermal Warning Temperature             | TTW0<br>TTW1   | (Junction Temperature) (Note 3)<br>TSTS = 0<br>TSTS = 1 | 125<br>150 | -  | - | $^{\circ}\text{C}$ |
| Thermal Warning Temperature Hysteresis  | TTWHYS         | (Junction Temperature) (Note 3)                         | -          | 25 | - | $^{\circ}\text{C}$ |
| Thermal Shutdown Temperature            | TTSD0<br>TTSD1 | (Junction Temperature) (Note 3)<br>TSTS = 0<br>TSTS = 1 | 150<br>175 | -  | - | $^{\circ}\text{C}$ |
| Thermal Shutdown Temperature Hysteresis | TTSDHYS        | (Junction Temperature) (Note 3)                         |            | 25 | - | $^{\circ}\text{C}$ |

### VOLTAGE MONITORING (VS, CHP, VGL, VCC)

|                                      |         |  |      |      |      |   |
|--------------------------------------|---------|--|------|------|------|---|
| VS Undervoltage Detection            | VSLV    |  | 4.8  | -    | 5.1  | V |
| VS Undervoltage Detection Hysteresis | VSLVHYS |  | 0.1  | 0.25 | 0.4  | V |
| VS Overvoltage Detection             | VSHV    |  | 30.5 | -    | 35.5 | V |
| Overvoltage Detection Hysteresis     | VSHVHYS |  | 1.5  | 2.0  | 2.5  | V |

## LV8961HUW

### ELECTRICAL CHARACTERISTICS (continued)

(Valid at a junction temperature range from  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , for supply Voltage  $6.0\text{ V} \leq \text{VS} \leq 28\text{ V}$ . Typical values at  $25^{\circ}\text{C}$  and  $\text{VS} = 12\text{ V}$  unless specified otherwise)

| Parameter                                     | Symbol   | Condition                        | Min             | Typ  | Max             | Unit |
|---|----------|----------------------------------|-----------------|------|-----------------|------|
| <b>VOLTAGE MONITORING (VS, CHP, VGL, VCC)</b> |          |                                  |                 |      |                 |      |
| VDH Overvoltage Detection                     | VDHHV    |                                  | 30.5            | –    | 35.5            | V    |
| VDH Overvoltage Detection Hysteresis          | VDHHVHYS |                                  | 1.5             | 2.0  | 2.5             | V    |
| CHP Undervoltage Detection                    | CHPLV    |                                  | $\text{VS}+4.5$ | –    | $\text{VS}+5.5$ | V    |
| CHP undervoltage Detection Hysteresis         | CHPLVHYS |                                  | 0.2             | 0.4  | 0.7             | V    |
| VGL Undervoltage Detection                    | VGLLV    |                                  | 4.5             | –    | 5.5             | V    |
| VGL Undervoltage Detection Hysteresis         | VGLLVHYS |                                  | 0.2             | 0.4  | 0.7             | V    |
| VCC3.3 Undervoltage Detection                 | VCLV3    | REGSEL = 0, VCEN = 1, VCLVPO = 0 | 2.3             | –    | 2.7             | V    |
| VCC3.3 Undervoltage Detection Hysteresis      | VCLVHYS3 | REGSEL = 0, VCLVPO = 0           | 0.1             | 0.25 | 0.4             | V    |
| VCC5.0 Undervoltage Detection                 | VCLV5    | REGSEL = 1, VCEN = 1, VCLVPO = 0 | 3.8             | –    | 4.2             | V    |
| VCC5.0 Undervoltage Detection Hysteresis      | VCLVHYS5 | REGSEL = 1, VCLVPO = 0           | 0.1             | 0.25 | 0.4             | V    |

### HVPIN PIN

|                             |        |  |                         |    |                        |                  |
|-----------------------------|--------|--|-------------------------|----|------------------------|------------------|
| Internal Pull-up Resistance | RI5    |  | 15                      | 30 | 60                     | $\text{k}\Omega$ |
| High Level Input Voltage    | VIH5   |  | $0.6 \times \text{VS}$  | –  | VS                     | V                |
| Low Level Input Voltage     | VIL5   |  | 0                       | –  | $0.4 \times \text{VS}$ | V                |
| Input Hysteresis Voltage    | VIHYS5 |  | $0.05 \times \text{VS}$ | –  | $0.2 \times \text{VS}$ | V                |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Not tested in production. Guaranteed by design.

## DETAILED FUNCTIONAL DESCRIPTION

The LV8961H integrates full sensorless brushless DC motor commutation and Proportional/Integral (PI) speed control. A robust startup algorithm combined with OTP registers for important system parameters make this IC a solution of choice for many BLDC applications which need to turn a motor in one direction only such as pumps, fans, etc.

Building a BLDC application with the LV8961H is even simpler than building a DC motor. Only a PWM pulse train is necessary to control the motor – either directly or via speed control. Switch-only applications are also possible. Speed and error information can be fed back to the control unit via FG and DIAG outputs.

If more complex operation and flexibility are required the LV8961H can be combined with a small microcontroller. The LV8961H implements motor commutation and includes all necessary support circuitry for the microcontroller such as:

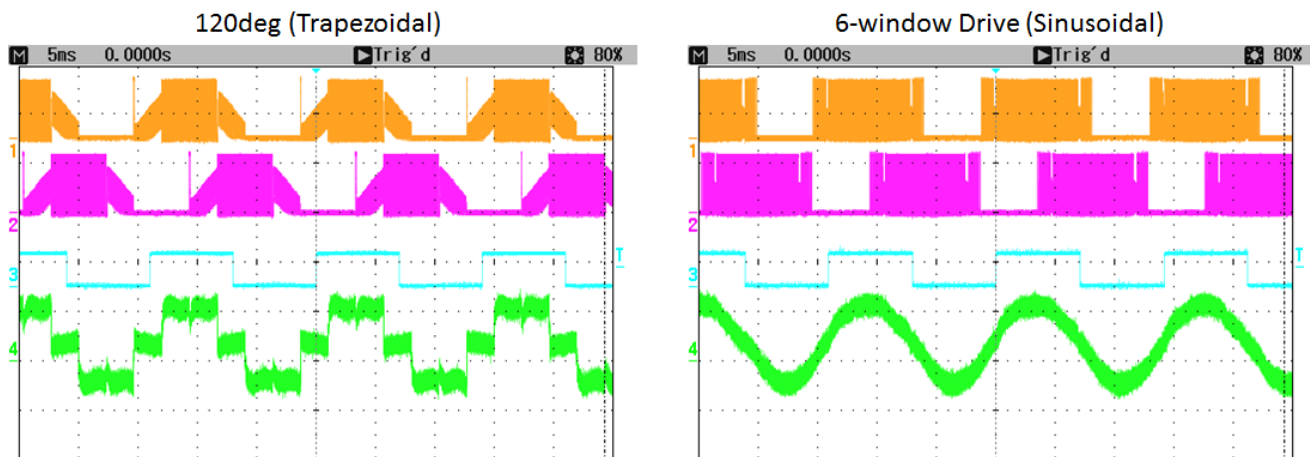
- 5 V / 3.3 V Power supply
- Integrated watchdog timer
- External Temperature Sensor

In case of system errors such as a missing control signal, or a watchdog error, the LV8961H includes auto-run settings. If one of those errors occur and connection to the microcontroller is lost, the motor can continue running at a predefined fixed duty cycle of 25%, 50%, 75% or 100% and TAG\_L or TAG\_H.

**Motor Commutation**

Motor position is detected using the BEMF of the un-driven phase of a rotating three-phase motor relative to its neutral point connected to COM. BEMF monitoring can be detected at 2 points in each phase of U/V/WOUT, and there are 6 zero-crossing signal in 3 phase in total with 6 un-driven windows. Once an adequate BEMF level has been detected voltages applied via PWM to the other two phases of the motor maintain rotation. The digital equivalent of the BEMF signal appears at FG.

Two different PWM patterns can be selected via register SLMD to match motors with trapezoidal or sinusoidal BEMF.



**Figure 7. Trapezoidal vs. Sinusoidal Drive**  
(CH1, 2 = U, V Phase Voltage, CH3 = FG, CH4 = U Phase Current)

With sinusoidal drive, each phase is driven with 6 windows for BEMF monitoring. This results in sinusoidal drive current with lower total harmonic distortion, reducing both torque ripple and noise. Trapezoidal drive results in a higher voltage across the motor phases and may be preferable for high torque and high speed operation.

**Rotor Position Detection**

The rotor position is detected with BEMF zero-cross timing. To detect the BEMF, the short window is opened by making the phase current zero or the phase float. Four types of the window mode are provided.

- 6-window mode  
All zero-crossings (rising and falling) for all three phases

will be detected by opening 6 windows per electrical cycle. This offers increased robustness at the expense of increased current waveform distortion. At the startup, this 6-window mode is automatically selected.

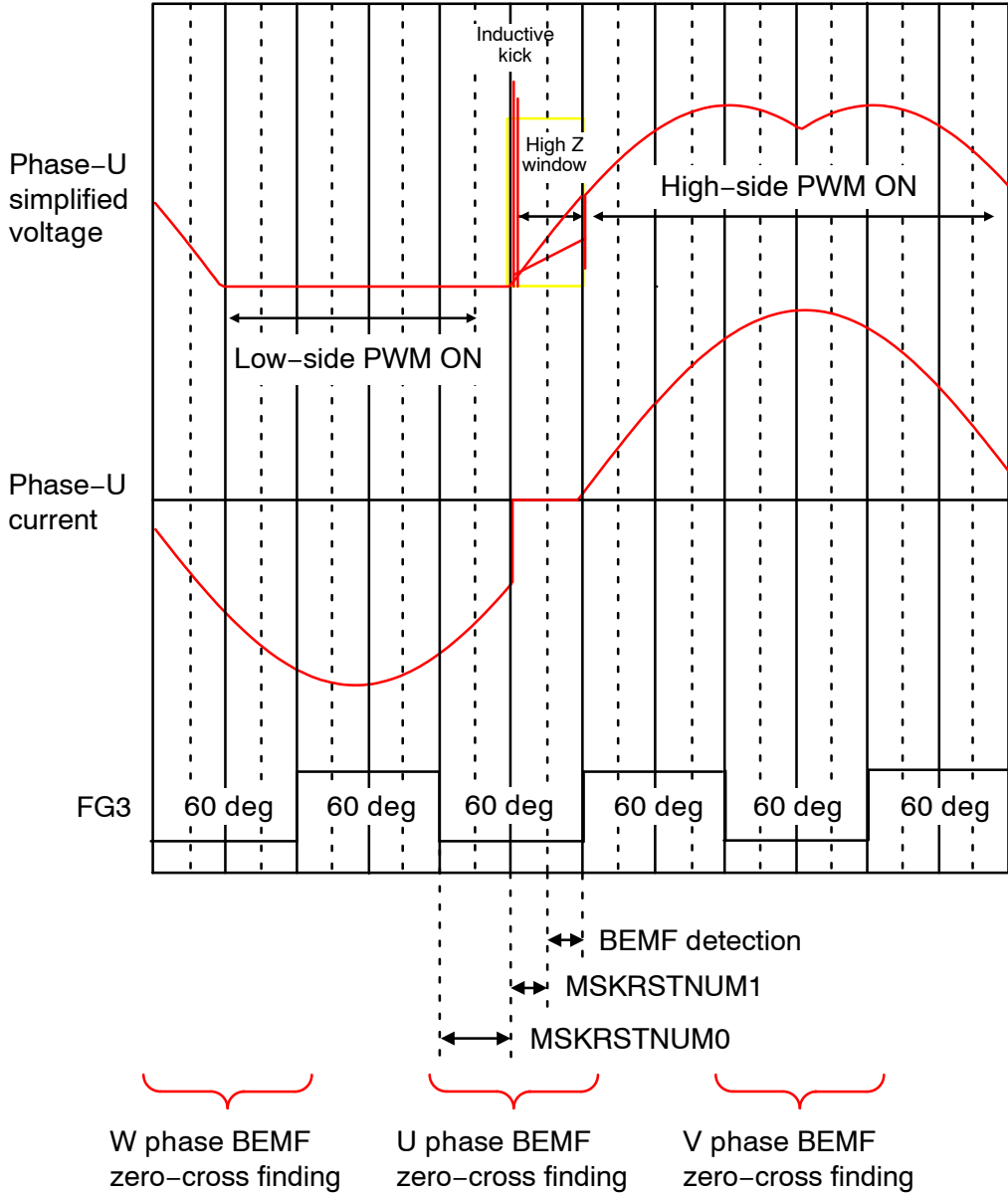
- 3-window mode  
One rising zero-crossing for each phase will be detected by opening 3 windows per electrical cycle. The same waveform is applied to the three phases.
- 1-window mode  
One rising zero-crossing in phase U will be detected by opening a window only in phase U. Therefore, the current waveform distortion will be minimized for the other phases.

- 2-window mode  
A rising- and a falling zero-crossing in phase U will be detected by opening 2 windows per electrical cycle only in phase U.

In this example (3-window mode), we will introduce two important timing parameters: MSKRSTNUM0 and MSKRSTNUM1:

*BEMF Window Timing*

Figure 8 shows a timing chart of the BEMF window with simplified phase voltage and current waveform illustrations.



**Figure 8. BEMF Window Timing Parameters**

(1) MSKRSTNUM0\_\*\*\*

Where, \*\*\* is ONE (for 1-window mode), TWO (for 2-window mode), THR (for 3-window mode), SIX (for 6-window mode), or INI (for startup 6-window mode).

MSKRSTNUM0 defines the time from the beginning of the BEMF detection window (reserved for that phase) until the moment where the phase output turns off (= start of the HiZ window).



$$\text{MSKRSTNUM0\_THR}[3:0] = x$$

$$x < 8 \rightarrow (15 + x * 3.75) \text{ deg}$$

$$x \geq 8 \rightarrow (41.25 + (x - 7) * 1.875) \text{ deg}$$

Example:  
 $x = 4 \rightarrow (15 + x * 3.75) \text{ deg} \rightarrow (15 + 4 * 3.75) \text{ deg} = 30 \text{ deg}$

(2) MSKRSTNUM1\_\*\*\*  
 Where, \*\*\* is ONE (for 1-window mode), TWO (for 2-window mode), THR (for 3-window mode), SIX (for 6-window mode), or INI (for startup 6-window mode).

MSKRSTNUM1 is a blanking (or ignoring) period from the start of the Hiz window defined by MSKRSTNUM0

until BEMF sensing. This blanking time prevents faulty zero-cross detection due to the flyback caused by the window opening.

$$\text{MSKRSTNUM1\_THR}[3:0] = x$$

$$((x + 1) + 1.875) \text{ deg}$$

Example:  
 $x = 2 \rightarrow ((x + 1) + 1.875) \text{ deg} \rightarrow ((2 + 1) + 1.875) \text{ deg} = 5.625 \text{ deg}$

These window parameters are used commonly with the sinusoidal waveform shaping mode and trapezoidal waveform shaping mode.

Table 1.

| WINDSEL | The Number of Window    |                        | Window Timing Parameters         |
|---------|-------------------------|------------------------|----------------------------------|
|         | SLMD = L<br>Trapezoidal | SLMD = H<br>Sinusoidal |                                  |
| 0       | 6                       | 6                      | MSKRSTNUM1_SIX<br>MSKRSTNUM0_SIX |
| 1       | 6                       | 3                      | MSKRSTNUM1_THR<br>MSKRSTNUM0_THR |
| 2       | 6                       | 2                      | MSKRSTNUM1_TWO<br>MSKRSTNUM0_TWO |
| 3       | 6                       | 1                      | MSKRSTNUM1_ONE<br>MSKRSTNUM0_ONE |

*Maximum Motor Speed*

The maximum physical motor speed of the application is limited by the internal clock to approximately 48000 electrical RPM. If this is exceeded the LV8961H coasts the motor until BEMF detection and drive can resume.

*Lead Angle Setting*

LV8961H can adjust the lead angle according to the output Duty as depicted in Figure 9. It is set by the registers LASET\_L, LASET\_H and LASET\_LIM.

LASET\_L sets lead angle when the output duty is 0%, and LASET\_H sets lead angle when the output duty is 100%.

And then LASET\_LIM sets the upper limit when an application requires it.

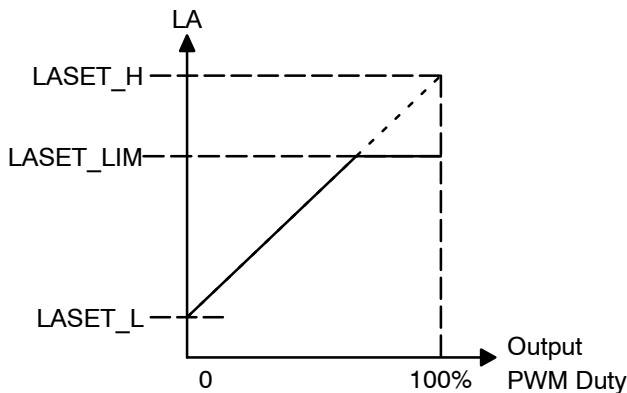


Figure 9. Lead Angle adjustment

*Motor Startup*

BEMF is used for rotor position sensing but for BEMF generation the motor has to be rotating. A stopped motor will initially be driven open-loop until BEMF can be detected.

Open-loop operation is motor parameter dependent. The most critical parameters depend on load and motor inertia: initial commutation frequency and PWM duty cycle (which affects motor flux density).

In the LV8961H, the initial commutation frequency is programmed with register STOSC. Flux density is regulated by limiting startup current with a current ramp. During this ramp the current limit is increased in 16 steps from 0 to the maximum current defined by the external shunt. The ramp time from 102 ms to 6.55 s is defined in register SSTT. Register CLREFEN\_STOP allows to disable the current ramp if necessary.

Fixed motor speed will be applied until either a valid BEMF has been detected in all three phases or the startup timer expires.

*Motor Lock*

This timer begins after the end of the current ramp and can be programmed from 400 ms to 6.4 s in register CPTM. If the timer expires a locked rotor error is flagged. In automatic retry mode, the LV8961H will restart after standby mode for time of eight times of CPTM.

## Motor Connect Open Detection

When the motor cannot be started for a certain period of time and it is in the startup mode, this IC flows current to each coil, then determines IC is in a constraint state when current flows, or an open state when no current flows. The detection time for the current to flow can be selected by OPDTM register.

## Spin-up of Rotating Motors

The LV8961H can perform freewheeling detection before applying the open-loop spin-up algorithm described above. If the motor is already turning in the right direction the IC will continue with closed-loop commutation. If the motor is turning in the wrong direction, the IC will wait for the motor to stop and then perform open-loop startup.

There are two scenarios where this behavior might not be desirable:

1. Fast Startup is required  
Freewheeling detection takes up to one electrical revolution of the motor, which may be unacceptable for some applications. In this case freewheeling detection can be disabled by setting FRREN
2. Windmilling backwards  
Should the motor be driven by some external force as it is freewheeling in the wrong direction the LV8961H will potentially wait forever. Should startup under these conditions be required, freewheeling detection must be disabled as well

## Chip Activation, Shutdown and System States

After power up of VS and WAKE above 2.5 V the LV8961H wakes up. Standby mode is entered after VS has exceeded 5.5 V (min.).

A high level on WAKE activates the IC from sleep mode which enables the internal linear regulator at V3RO. Once the voltage on V3RO as sensed on V3RI has passed the

power on reset (POR) threshold the system oscillator starts, and after 32 counts of the system clock (1.6  $\mu$ s typical) releases the internal digital reset which simultaneously starts the external regulator VCC and the charge pump, and loads the system register contents from OTP into the internal registers. During the entire wake-up sequence of 8 ms (typ.) DIAG is masked for charge pump and VCC undervoltage. After wake-up is complete, the IC enters Standby mode and DIAG is activated to display internal errors. During Standby mode full SPI access is possible.

A high on EN takes the LV8961H from Standby to Normal mode. Normal mode allows motor control and SPI access is limited. A low on EN disables the motor stage regardless of the PWM input and returns the part back to Standby mode.

The IC is shut down by taking WAKE to low level. WAKE has priority over the state of EN, if EN hold functionality is desired; it needs to be implemented with an external diode from EN to WAKE.

## System States

LV8961H has three operating modes. The operating modes are controlled by WAKE and EN.

### Sleep Mode

Sleep mode is a power saving mode. All circuits are powered down, charge pump is inactive and the SPI port is unusable. Activating WAKE allows the transition from the sleep mode to either Standby or Normal mode.

### Standby Mode

In Standby mode the OTP content has been transferred into the main registers. In this mode all outputs are turned off. Any internal writable register that is not locked can be configured by SPI interface.

### Normal Mode

In normal mode, outputs can be controlled and all blocks are active. All registers can be read through the SPI interface.

| Mode    | WAKE | EN | Internal Bias | Logic  | VCC     | Charge Pump | Drivers |
|---------|------|----|---------------|--------|---------|-------------|---------|
| Sleep   | L    | x  | Disable       | Reset  | Disable | Disable     | High-Z  |
| Standby | H    | L  | Enable        | Active | Enable  | Enable      | Low     |
| Normal  | H    | H  | Enable        | Active | Enable  | Enable      | Enable  |

## Supply Voltage Transients

The LV8961H is well suited to operate during typical automotive transients. It is fully functional during start-stop transients, as it maintains all specified parameters for supply voltages from 6 V < VS < 28 V. If the supply voltage falls below 5 V, for example during cold cranking, undervoltage error is flagged, but digital functionality is maintained until the internal regulator falls below its undervoltage lockout level of 2.2 V. The VCC regulator must be configured for 3.3 V if low transient operation is desired.

If overvoltage protection is enabled in MRCONF8 an overvoltage error is indicated if the supply rises beyond 28 V(min). In both under- and overvoltage error modes, the

power stage drivers UH, VH, WH and UL, VL, and WL go low, turning the external power stage high impedance and letting the motor freewheel. The LV8961H will re-engage the motor after conditions have returned to normal.

## System Power Supplies

Three power supplies are integrated into the LV8961H:

- An internal 3.3 V regulator provides power to the digital and interface section
- The VCC regulator can be configured to provide 5 V or 3.3 V to an external processor and other loads

- A two-stage charge pump allows 100% duty cycle operation and maintains full enhancement to the power stage at low input voltages

**Internal Regulator V3RO, V3RI**

The internal regulator is supplied from VS and provides 3.3 V at V3RO. V3RI is connected to the power supply inputs of the control- and logic circuit blocks. V3RO and V3RI need to be connected externally and decoupled to the GND plane for stability. V3RO should not be connected to external loads.

**VCC Regulator**

The VCC regulator may power external loads, VCC becomes active during Standby mode and can be configured via register REGSEL to provide 5 V or 3.3 V. WARNING: the microcontroller can be damaged if the wrong REGSEL value is selected. Undervoltage error is flagged if the output voltage drops below VCLV5 in 5 V operation, or VCLV3 in 3.3 V operation.

The VCC regulator can be enabled or disabled with register VCEN.

**Charge Pump Circuit for CHP and VGL**

LV8961H has an integrated charge pump circuit for low-side and high-side predriver supply. Low-side drive voltage at VGL is 12 V(typ.) and high-side drive voltage at CHP is VS + 12 V(typ.). For functionality see Figure 10.

Undervoltage protection for the low-side drivers activates if VGL falls below VGLLV in which case the output FET's will be turned off and VGL undervoltage error is flagged in register MRDIAG. Overvoltage protection for the high-side drivers activates if VS becomes greater than 28 V(min). In that event the driver stage is disabled, overvoltage error is flagged in register MRDIAG, and both VGL and CHP are discharged to prevent output circuit destruction.

The charge pump circuit operates nominally at 52.1 kHz. A SSCG function is provided to add a spread-spectrum component for EMI reduction.

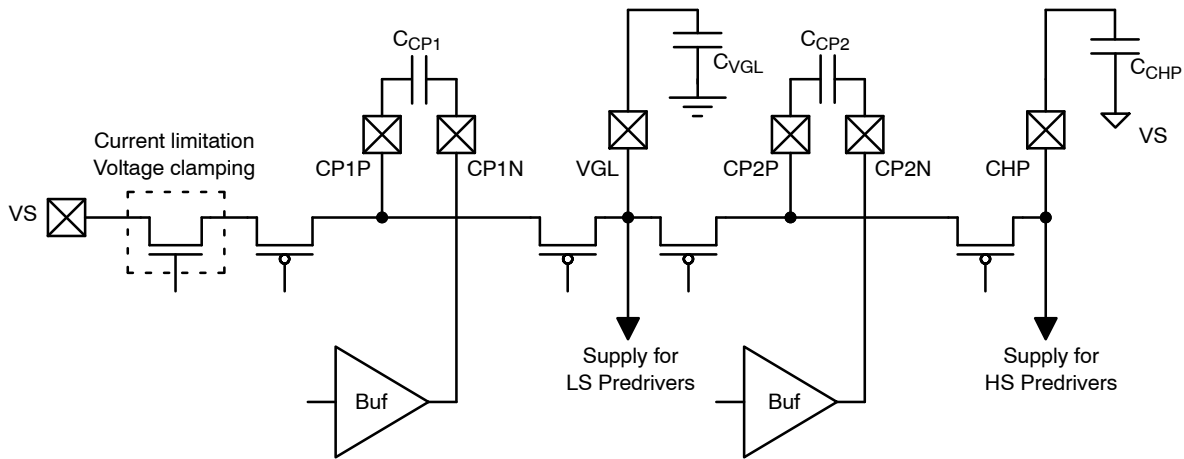


Figure 10. Charge Pump Circuit

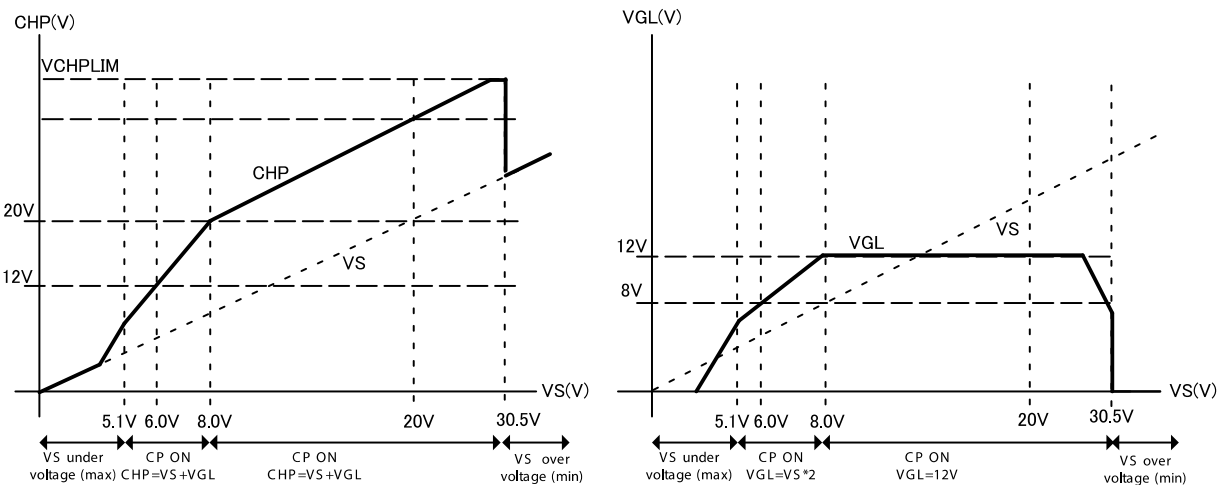


Figure 11. High-Side and Low-Side Gate Voltages

**INPUT PWM and SPEED CONTROL**

The LV8961H provides three speed control methods through the input PWM signal:

1. Indirect PWM translation
2. Closed-loop speed control
3. Direct register command

*Indirect PWM Translation*

This is the preferred mode for stand-alone operation. The frequency range has two modes, high and low frequency. In the high frequency mode, it corresponds to frequency input up to 18.5 kHz. In the low frequency mode, it is limited to the frequency input up to 1 kHz, and when the frequency input is above 1 kHz, it is ignored. Frequency mode can be configured in high frequency mode by setting register PWMF to 1. In both modes the input PWM signal is compared against minimum PWM frequency thresholds to allow for more robust operation. Frequencies below 5.3 Hz (typ.) are considered as 0% or 100% duty cycle (no frequency).

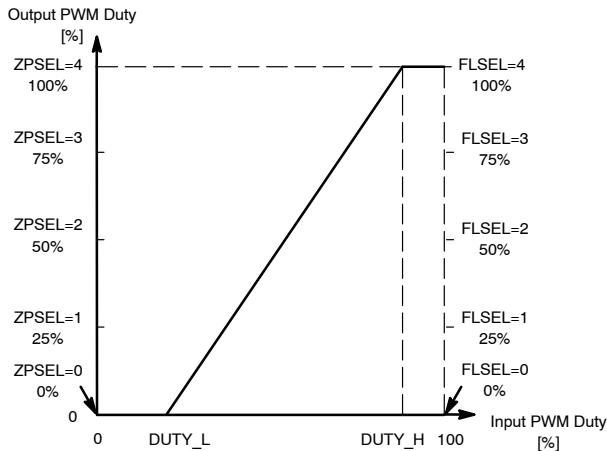
The duty cycle of the PWM input signal is measured with a resolution of 10 bits. There is an inherent delay to detect and utilize this duty cycle information. It is the delay time from input PWM input signal to output PWM. The delay time is determined by

$$T_{PWM} + 19.8 \mu s \text{ (max.)}$$

Where,  $T_{PWM}$  is the period of the PWM input signal. 19.8  $\mu s$  is fixed value.

If faster startup is necessary, see section “Fast Startup” below. If no frequency is detected after 210ms (typ.) the PWMPO flag is set in system warning register MRDIAG1. Even without PWM input the LV8961H can run as described below in section “Fast Startup”.

If a valid frequency was detected, the LV8961H evaluates the input duty cycle and translates it into an output duty cycle as shown in Figure 12. The output PWM frequency is fixed to 19.5 kHz (typ.).



**Figure 12. Duty Cycle Translation**

Input duty cycles lower than the minimum Duty setting by DUTY\_L register are considered a motor-off command and

will also reset the error registers. Input duty cycles higher than the maximum Duty setting by DUTY\_H register are considered a full drive command. Input to output duty cycle translation is described by the following formula:

|             |   |                                |
|-------------|---|--------------------------------|
|             | 0   | $0 \leq d_{IN} \leq DUTY\_L$   |
| $d_{OUT} =$ | $\frac{100}{DUTY\_H - DUTY\_L} \times (d_{IN} - DUTY\_L)$ | $DUTY\_L < d_{IN} < DUTY\_H$   |
|             | 100   | $DUTY\_H \leq d_{IN} \leq 100$ |

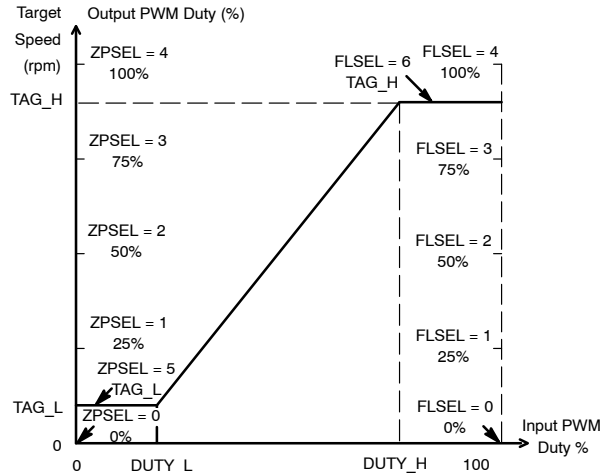
*Closed-loop Speed Control*

For stand-alone operation, the LV8961H offers a PI controller for motor speed which is activated by clearing bit SCEN. Frequencies below 5.3 Hz (typ.) are considered as 0% or 100% duty cycle (no frequency). The output PWM frequency is fixed to 19.5 kHz (typ.).

LV8961H provides Linear characteristic target speed setting as shown in Figure 13.

*Direct Register Command*

LV8961H allows user to access the register directly, which is connected to the control logic, and set the PWM duty cycle command from the PWMDTIN register. This mode can be configured by setting register SPIINSEL to 1. Also, FG frequency information can be obtained from the STATUS register by setting register STATSEL to 0h, and It can minimize delay that occurs when the PWM frequency is low.



**Figure 13. Target Speed by Input PWM Duty Cycle**

*The Control Algorithm*

The LV8961H controls the motor speed by comparing the selected target speed to the actual motor speed and incorporating a PI controller with configurable gains for the P, I and T components which are stored in register MRSPCT7, MRSPCT8 and MRSPCT9 respectively.

*Ramping of Speed Control Values*

While tight control is required for optimal speed tracking, it may be undesirable during large input changes as it may

lead to sudden supply loading, increasing noise and motor wear. To limit the slope of the control signal, register USTEPSEL and DSTEPSSEL imposes a ramp on an input step to slew the speed response of the motor.

Decreasing motor speed too fast results in energy recuperation back into the system. To limit overvoltage

during energy recuperation, the variable DWNSET allows to prevent energy recuperation entirely by switching the synchronous rectification off.

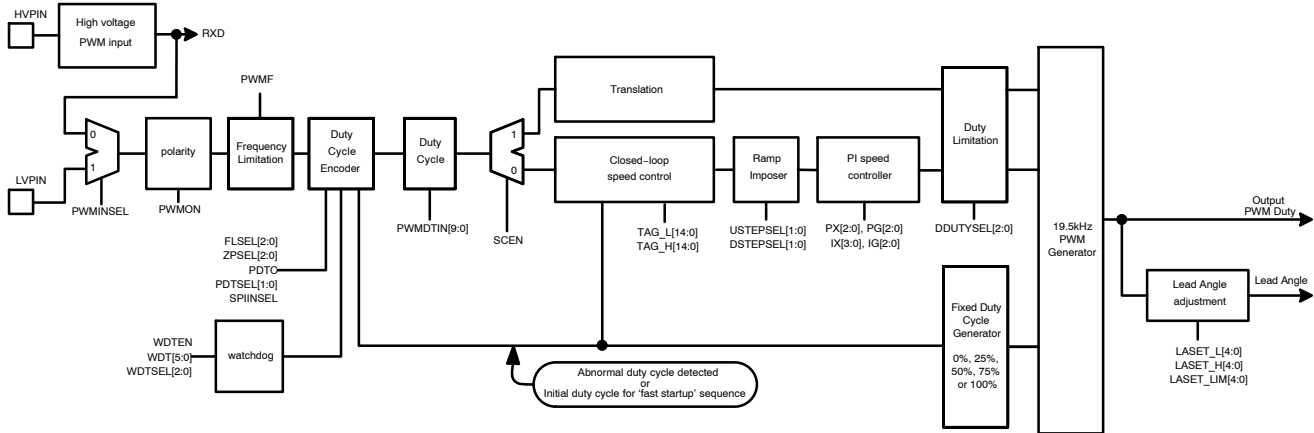


Figure 14. PWM Command Flow and Related Registers

### Fast Startup

It may be desirable to have the motor start immediately after EN goes high and not wait for PWM input duty cycle evaluation. Two register settings enable motor operation during this evaluation time: bit PDTC determines if the motor should be running during this time at all, and PDTSEL selects a motor duty cycle of 25, 50, 75 or 100%. This is used as the initial value of the duty cycle command for the closed-loop speed control mode. To guarantee smooth transition from fast startup to PWM operation it is important to apply a comparable external PWM duty cycle at startup.

### Abnormal Duty Cycle Operation (100% or 0%)

For normal duty cycle controlled operation the PWM signal is expected to have a frequency between 5.3 Hz or more. If no frequency is detected, the LV8961H will flag PWMPO error and enter 0% or 100% duty cycle mode depending on the level of the PWM signal (all low or all high). Operation during this mode can be selected to be either no motor operation, or motor operation at a fixed motor duty cycle of 25, 50, 75 or 100% and TAG\_L or TAG\_H as defined by the variables FLSEL or ZPSEL. These PWM values do not enter into the speed control loop.

### Limit the Amount of Change of Output Duty

The register DDUTYSEL allows to limit the amount of change in output duty to avoid sudden acceleration and deceleration.

### Speed Feedback FG

The motor speed is shown at open drain output FG where the transitions are direct representations of the BEMF signal transitions on the motor. The relationship between motor rotation and FG pulses is defined in register FGOF.

### Fault Output DIAG

A low on open drain output DIAG indicates a system fault and a shutdown of the driver stage. Per default all system faults self-recover when the fault condition is removed. For some potentially destructive faults such as overcurrent, FET short-circuit and locked rotor conditions, it is possible to latch the fault condition. For more information on system diagnostics see section “[System Errors and Warnings](#)”.

### High Voltage PWM Interface

The PWM interface translates a VS level signal with a threshold of 50%(Typ) VS to a digital signal appearing at RXD pin. This signal can be used for input PWM translation from outside units to the microcontroller.

### Predriver Circuit

The predriver circuit of the LV8961H includes 3 half-bridge drivers which control external NFETs for the motor phases U, V and W. The high-side drivers UH, VH, WH switch their gate connection either to CHP or the respective phase connection UOUT, VOUT and WOUT. The low-side drivers are switched from VGL to the corresponding source connection SUL, SVL, SWL. Both high- and low-side switches are not current controlled. Slope control has to be implemented with external components.

Current shoot through protection of the bridge drivers is implemented by a dead time counter that delays the turning-on of the complementary switch. The dead time can be programmed from 200 ns < t<sub>FDTI</sub> < 6.4 μs into 5bit parameter FDTI.

To protect against external shorts the drain–source voltage of the active external Power FETs is monitored as well. 4 bit register FSCDL selects a short–circuit shutoff voltage  $100\text{ mV} < V_{\text{FSCDL}} < 1.6\text{ V}$ . To suppress false triggering during the rising edge of FET activation, FSCDT selects the masking time.

**Current Limit and Overcurrent Shutoff**

An integrated current sense amplifier implements current limiting and overcurrent shutoff by measuring the motor phase current across a single shunt between RF and RFSENS.

Figure 15 shows a summary of the current limit and the overcurrent shutoff, and the descriptions for each function are in the following sections.

In Sleep mode, the high– and low–side gate outputs of each U, V, W phase become High Z.

A 100 kΩ pull–down resistor is built–in between UH and UOUT of the high–side predriver output so that the gate and source of the external FET do not become High Z.

The low–side output also has a built–in 100 kΩ pull–down resistor between the UL and SUL terminals (similar for V and W phases).

An external resistor (typ. 100 kΩ) is visible in the application circuit between the gate and source of the FET.

*Cycle–by–cycle Current Limit*

If the voltage between RF and RFSENS exceeds VRF1, the active bridge is turned off until the next PWM period. VRF1 can be selectable 100 mV(Typ) or 50 mV(Typ) by register CLSEL. To suppress switching transients a current limit blanking time  $0.2\text{ }\mu\text{s} < t_{\text{CLMASK}} < 3.2\text{ }\mu\text{s}$  can be programmed into register CLMASK.

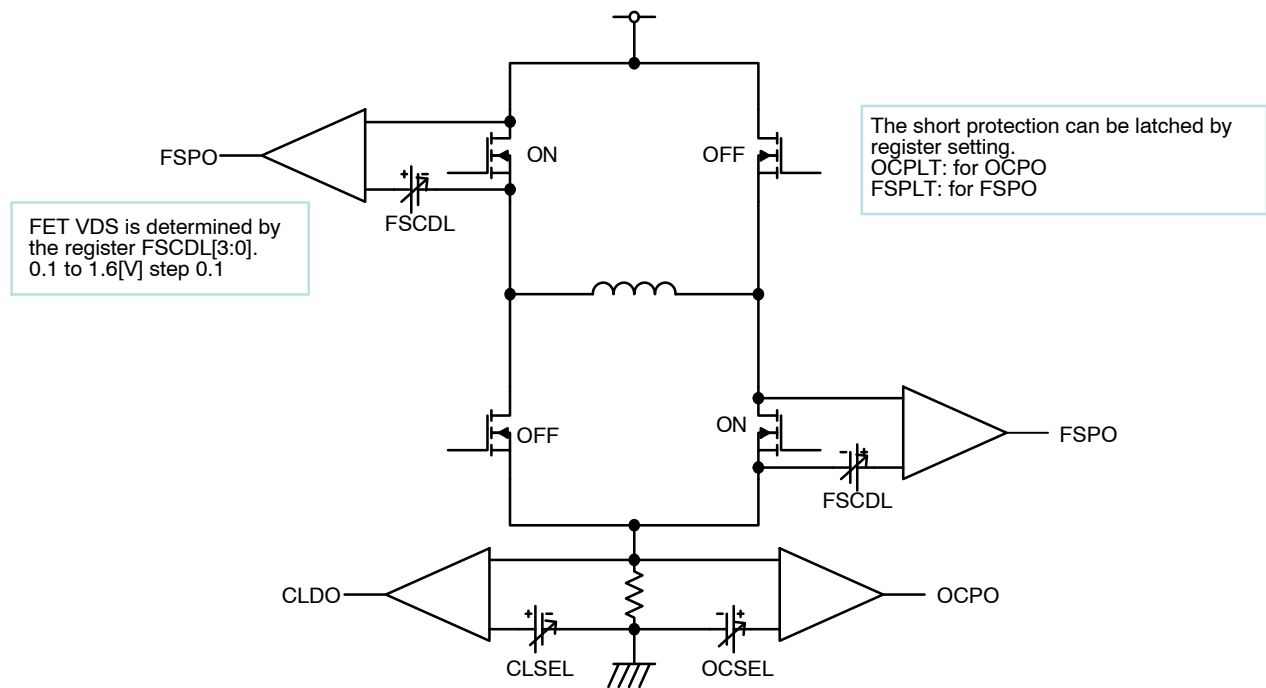
During soft start this current limit is ramped from 0 to VRF1 in 16 steps during a programmable time  $102\text{ ms} < t_{\text{SST}} < 6.55\text{ s}$  as defined in register SSTT.

*Overcurrent Shutoff*

If the bit OCPEN is set and the voltage between RF and RFSENS exceeds VRF2, the LV8961H goes into overcurrent shutoff and all predrivers are driving low turning the power FETs high impedance. VRF2 can be selectable VRF1 + 25 mV, +50 mV, +75 mV and +100 mV by register OCSEL. To suppress switching transients an overcurrent shutoff blanking time  $0.2\text{ }\mu\text{s} < t_{\text{OCMASK}} < 3.2\text{ }\mu\text{s}$  can be programmed into register OCMASK.

**Table 2. SUMMARY OF POWER STAGE PROTECTIONS**

| Current        | Purpose   | Flag | Sense point        | Threshold                             | Turn–off | Recovery       |
|----------------|-----------|------|--------------------|---------------------------------------|----------|----------------|
| Cycle–by–cycle | Limiter   | CLDO | Sense Resistor VRF | VRF1 100 mV or 50 mV                  | PWM FET  | Next PWM cycle |
| Short to VS    | Protector | OCPO | Sense Resistor VRF | VRF1+25 mV, +50 mV, +75 mV and 100 mV | All FET  | 50 ms later    |
|                |           | FSPO | FET VDS MOUT–SXL   | Configurable                          |          |                |
| Short to GND   | Protector | FSPO | FET VDS VDH–MOUT   | Configurable                          | All FET  | 50 ms later    |



**Figure 15. Current Limit vs. Overcurrent Shutoff**

**Temperature Sensing**

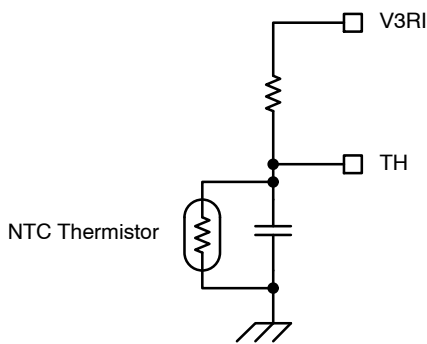
The LV8961H measures the die temperature and implements internal thermal warning and shutdown. It is also possible to protect external devices by monitoring the voltage at pin TH. Internal and external overtemperature can shut down the driver section.

*Internal Overtemperature Measurement*

A thermal warning is issued if the internal temperature of the device reaches approximately 25°C below the overtemperature shutoff level. The shutoff level is selected by bit TSTS as 150°C or 175°C(min).

*External Overtemperature Shutoff*

An analog comparator triggers external overtemperature error if the voltage at pin TH falls below the two bit programmable level  $0.2\text{ V} < V_{\text{THTH}} < 0.35\text{ V}$  as defined by register THTH. For external temperature measurement connect a resistor between V3RO and TH and an NTC between TH and AGND. The programmed threshold voltage at  $V_{\text{THTH}}$  should be reached at the intended thermal shutdown temperature of the external component to be protected. During the overtemperature condition, the predrivers are disabled and a flag, THPO in MRDIAG0 is set.



**Figure 16. Example Circuit for External Temperature Sensing**

**Watchdog Operation**

The LV8961H includes a watchdog timer to monitor a companion microcontroller and disable the motor if the

microcontroller stops working properly. Bit WD TEN enables and disables the watchdog timer. Access to this bit can be blocked – see section “OTP Register” for details. The enabled watchdog will issue an error whenever the watchdog time  $1.6\text{ ms} < t_{\text{WDT}} < 102.4\text{ ms}$  expires. A write of 00h to register MRRST resets the watchdog timer.

A watchdog timeout can result in either a motor stop, or motor operation at four predefined duty cycles of 25%, 50%, 75% or 100% and TAG\_L or TAG\_H as defined by WDTSEL. The duty cycle is directly applied to the power stage, not through the speed selection registers. The microprocessor is not reset.

**System Errors and Warnings**

All system errors and most warnings cause a transition on DIAG. The polarity of this transition can be selected in bit DIAGSEL. The ability of stand-alone applications without microcontroller to react to errors and warnings is limited. For this case various auto-retry strategies are implemented.

If a companion microcontroller exists, more complex error handling is possible and DIAG should be connected to an interrupt input of the microcontroller. Errors that may cause serious damage such as short-circuit, overcurrent and locked rotor can be latched by enabling the corresponding latch bit in MRCONF9. In this case the LV8961H will keep the output stage disabled until the latch is cleared by one of the following actions:

- Power on reset
- EN low
- Input the output duty 0% or 0 rpm command
- SPI write of FFh to MRRST

If bit DLTO is set ONLY latched errors will cause a transition of DIAG. To detect the other less serious errors and warnings, the diagnostic registers MRDIAG0 /MRDIAG1/MRDIAG2 have to be read regularly via SPI access.

**Table 3. ERROR AND WARNING DIAGNOSTIC REGISTER** (Note 4)

| ADDR  | Bit | Error   | Description       | Enabled Set | Latched Set | Self-Recovery Timing                      |
|-------|-----|---------|-------------------|-------------|-------------|---|
| 0201h | 0   | OCPO    | Overcurrent Error | OCPEN       | OCPLT       | After 50 ms (typ.) the motor will restart |
| 0201h | 1   | VSLVPO  | VS Undervoltage   | N/A         | N/A         | Motor is restarted when voltage recovers  |
| 0201h | 2   | VSOVPO  | VS Overvoltage    | OVPEN       | N/A         | Motor is restarted when voltage recovers  |
| 0201h | 3   | CHPLVPO | CHP Undervoltage  | N/A         | N/A         | Motor is restarted when voltage recovers  |
| 0201h | 4   | VGLLVPO | VGL Undervoltage  | N/A         | N/A         | Motor is restarted when voltage recovers  |

**Table 3. ERROR AND WARNING DIAGNOSTIC REGISTER** (Note 4) (continued)

| ADDR  | Bit | Error   | Description                   | Enabled Set               | Latched Set | Self-Recovery Timing                                |
|-------|-----|---------|-------------------------------|---------------------------|-------------|---|
| 0201h | 5   | FSPO    | FET Short-Circuit             | FSPEN                     | FSPLT       | After 50 ms (typ.) the motor will restart           |
| 0201h | 6   | THPO    | External Overtemperature      | THPEN                     | N/A         | Motor is restarted when temperature recovers        |
| 0201h | 7   | CPO     | Locked Rotor                  | CPEN                      | CPLT        | Wait 8 t <sub>CPTM</sub> periods (see "Motor Lock") |
| 0202h | 0   | THWPO   | Chip Junction Warning         | THWEN                     | N/A         | Only warning  |
| 0202h | 1   | THSPO   | Chip Junction Overtemperature | N/A                       | N/A         | Motor is restarted when temperature recovers        |
| 0202h | 2   | WDTPO   | Watchdog Timeout              | WDTEN                     | N/A         | Motor is restarted when WDT is reset                |
| 0202h | 3   | CLDO    | Current Limit Warning         | CLDOEN                    | N/A         | Only warning  |
| 0202h | 4   | OOPO    | Motor Open Detect             | OOPOEN                    | N/A         | Same as Motor Lock protect                          |
| 0202h | 5   | RCSMPO  | Register Checksum Error       | N/A                       | N/A         | Write MRRST = 55h or MRODL = 00h or MRODL = FFh     |
| 0202h | 6   | VCLVPO  | VCC undervoltage              | VCLVPEN                   | N/A         | Motor is restarted when voltage recovers            |
| 0202h | 7   | PWMPO   | PWM Input Fault               | FLSEL<br>ZPSEL<br>PPDOSEL | N/A         | Motor is restarted when PWM input recovers          |
| 0203h | 0   | VDHOVPO | VDH overvoltage               | VDHOVPEN                  | N/A         | Motor is restarted when voltage recovers            |
| 0203h | 1   | STUPO   | Startup Operation             | N/A                       | N/A         | Only warning  |
| 0203h | 2   | SPCO    | Loss of speed lock            | N/A                       | N/A         | Only warning  |
| 0203h | 3   | FGERPO  | FG error protection output    | FGERACCEN<br>FGERDECEN    | N/A         | Wait t <sub>RCV<sub>TM</sub></sub> periods          |
| 0203h | 4   | REGAZ   | Register data all 0 output    | N/A                       | N/A         | Only warning  |
| 0203h | 5   | OTPAZ   | OTP data all 0 output         | N/A                       | N/A         | Only warning  |

4. See register MRCONF 7 to 12 for error and warning activation, masking and latching options.

### Detection of Loss of Commutation Synchronization

Three methods are provided to detect the loss of commutation synchronization which is significant for sensorless motor control applications.

1. Open load
2. Abnormal rotational speed change
3. Locked rotor

They are explained in the following sections.

#### Open Load Detection

LV8961H can detect an open motor phase connection by means of setting OOPOEN = 1.

When this function is enabled, then after the detection of a blocked rotor (CPO=1), a testcurrent is briefly pulsed from UH to VL, from VH to WL and from WH to UL. The current will increase and stop when the current limit is reached (outputs are switched off). When the current limit is not reached within the time set by OPDTM, the outputs are switched off and an open connection is assumed. However, a motor phase is considered open (bit OOPO=1) only if both

sequences related to that motorphase don't reach in time the current limit. Therefore it is important to set OPDTM sufficiently long.

It can be checked which U, V, W connector is open by reading the status register. One connector opening of U, V, W can be distinguished, but when two or three openings overlap, it is judged that everything is open so it cannot be distinguished what is not open. Also, if only one of UH-VL, VH-WL, WH-UL combinations don't reach the current limit, it is judged that all phases are connected.

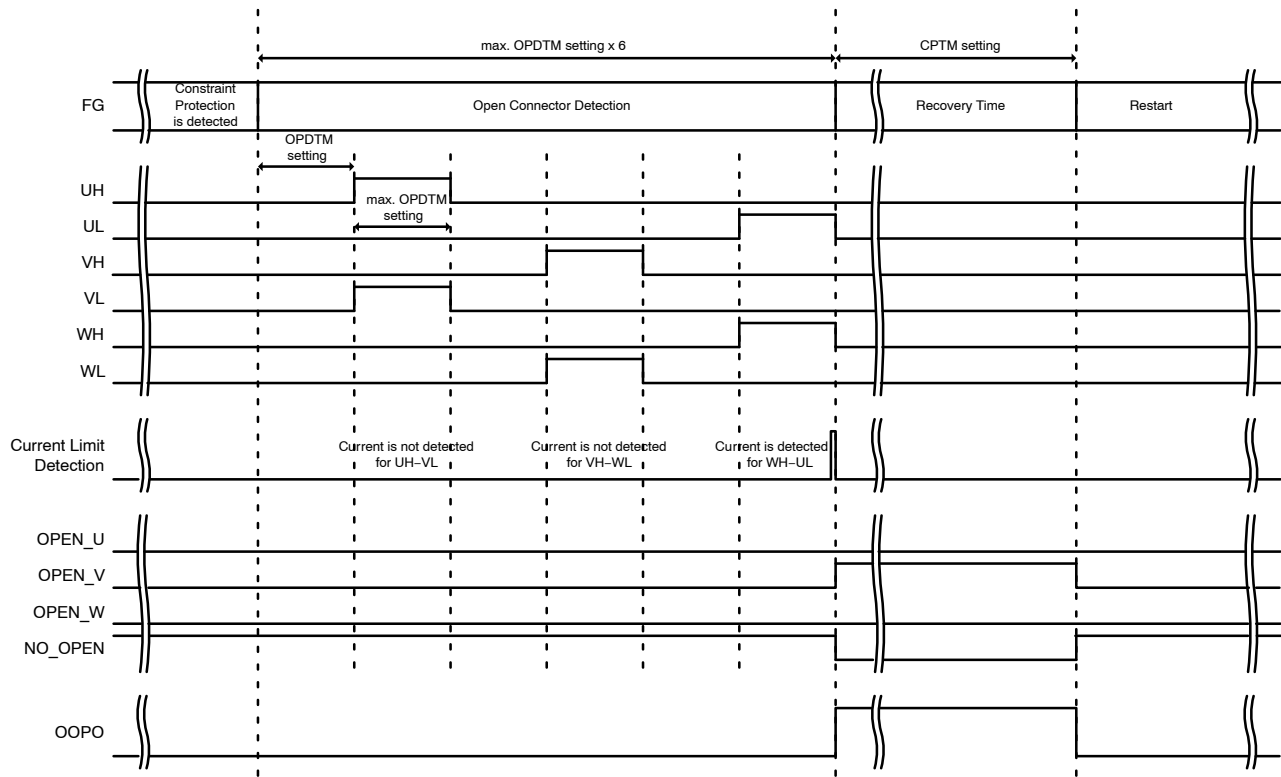
When automatic recovery mode is set, OOPO returns to 0 when the time set in the CPTM register (the constraint protection detection time multiplied by 8) has elapsed. When latch mode is set, OOPO returns to 0 by EN = L input, PWM 0% input, or MRRST command.

Because the open load detection is performed after the constraint protection detection, CPO = 1 is output.

Figure 17 shows an example where automatic recovery mode is set and phase-V is detected to be open.



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**Figure 17. Timing Chart of OPO**

### Abnormal Rotational Speed Change Detection

The abnormal rotational speed change detection is activated for acceleration through bit FGERACCEN and for deceleration by means of FGERDECEN.

An abnormal acceleration is detected if the number of detected BEMF zero-crossings immediately after the mask is opened is equal or larger than the number represented by FGERACC.

An abnormal deceleration is detected if no zero-crossings are observed during the time represented by FGERDEC (Table 4).

If it is judged that the rotation speed is abnormal, LV8961H restarts from free-run detection after the recovery time set by RCVTM has elapsed.

Upon detection of abnormal rotational speed change, all predriver outputs are switched off and bits FGERACCO resp. FGERDECO are set. They will reset when the recovery time (RCVTM) elapses.

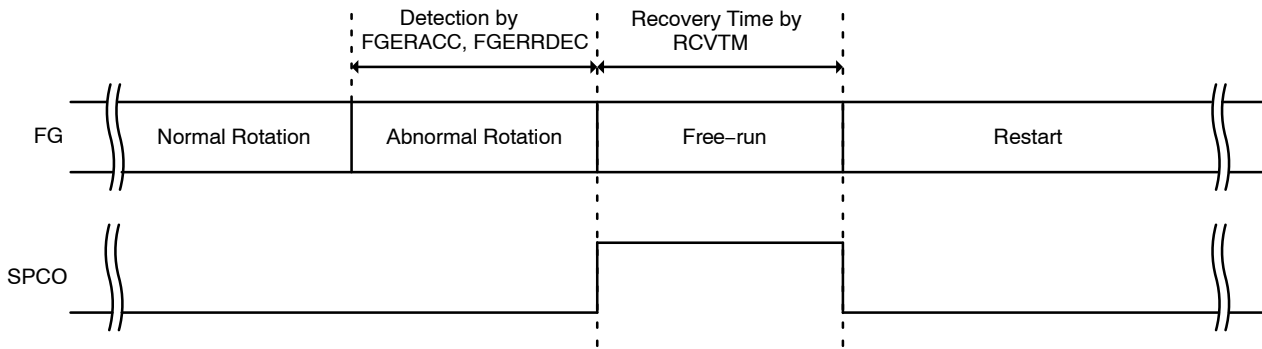
The protection state also returns to normal state by either EN = L input, sensorless logic reset pulse by MRRST.

When FGERACCEN/FGERDECEN = 0, although the rotation speed abnormality is detected, state transition to the protection state does not occur.

**Table 4. FGERDEC SETTING**

| FGERDEC[2:0] | Detection Setting                              |
|--------------|--|
| 0            | (previous 60 electrical degrees period) × 1.25 |
| 1            | (previous 60 electrical degrees period) × 1.5  |
| 2            | (previous 60 electrical degrees period) × 1.75 |
| 3            | (previous 60 electrical degrees period) × 2    |
| 4            | (previous 60 electrical degrees period) × 3    |
| 5            | (previous 60 electrical degrees period) × 4    |
| 6            | (previous 60 electrical degrees period) × 6    |
| 7            | (previous 60 electrical degrees period) × 8    |

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**Figure 18. Timing Chart of SPCO**

## Locked Rotor Detection

Open-loop startup continues for the time programmed into CPTM (MRCONF6[6:3]). If no BEMF is detected during that time a locked rotor error is indicated.

**Table 5. MRCONF6**

| ADDR  | Data Name | D[7] | D[6]      | D[5] | D[4] | D[3]      | D[2] | D[1] | D[0] |
|-------|-----------|------|-----------|------|------|-----------|------|------|------|
| 0106h | MRCONF6   | 0    | CPTM[3:0] |      |      | THTH[1:0] |      | TSTS |      |

CPTM[3:0] : Constrained movement Protection Time

The locked rotor is detected by counting the time LV8961H is in the startup mode without BEMF detection. If consecutive seven BEMF zero-crossings are not detected within the time programmed into CPTM register, the driver outputs are turned off and the locked rotor is flagged.

In auto-recovery mode, the motor will remain off for the open-loop startup timeout duration multiplied by 8, before another startup is attempted.

Detection time has maximum 1 ms error, because it is sampled by 1 ms clock.

**Table 6. MRDIAG0**

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4]    | D[3]    | D[2]   | D[1]   | D[0] |
|-------|-----------|------|------|------|---------|---------|--------|--------|------|
| 0201h | MRDIAG0   | CPO  | THPO | FSPO | VGLLVPO | CHPLVPO | VSOVPO | VSLVPO | OCPO |

CPO : Constrained movement Protection Output

If no BEMF is detected during the entire open-loop startup time as programmed in CPTM, then either the rotor

is blocked, or startup parameters are not correct. The drivers will be disabled.

## SPI Interface

In the LV8961H the SPI interface is used to perform general communications for status reporting, control and programming. The SPI format is MODE-0 MSB first.

SPI communication with the LV8961H follows the established industry standard practices. Data is transferred MSB first, and it is captured at the rising edge of the clock which stays in logical low during idle. Figure 19 shows LV8961H SPI format. When the first SI bit “R/W” is LOW, the register data will be transferred from LV8961H to the master device. When “R/W” is HIGH, the register data is transferred from the master device to the LV8961H register.

The address data is composed of 16 bits and has a function of accessing from the address specified by the data Length [2:0] setting to the address of continuous 8 bytes by one communication. In addition, the LV8961H offers CRC

check feature to ensure SPI communication. Therefore, Format 1 in Figure 19 requires a minimum 5 bytes data length with one access. Format 2 in Figure 19 is prepared to access with a short data length. It can be used for addresses requiring access in a short time and is set by the data BASEL[3:0].

When the repeating access to the same register access is required, a shorter bit-length alias of the target address can reduce the total length of the SPI serial communication data train. In LV8961H, the base address pointers are provided as an alias of the full-bit address. The base address can be specified with the register “BAREG[15:0]”. And, BAREG[15:0] is activated as the base address pointer when the bit-field “BASEL[3:0]” value in the SPI serial data train is 15. Without BAREG setting, 14 preset base addresses,

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which might be read or written frequently and repeatedly,

are provided. The following table shows the those addresses selected by the bit-field BASEL[3:0].

**Table 7.**

| BASEL[3:0] | Register name | Register address | Description                             |
|------------|---------------|------------------|---|
| 0          | NA            | NA               | Direct addressing in full-bit           |
| 1          | MRACK0        | 0000h            | 55h fixed value read-only               |
| 2          | MRSPCT0       | 0002h            | Current control parameters              |
| 3          | MRSPCT1       | 0003h            | Lead angle parameters                   |
| 4          | MRSPCT3       | 0005h            | Startup parameters                      |
| 5          | MRSPCT7       | 0009h            | Speed control PI parameters             |
| 6          | MRSPCT10      | 000Ch            | Speed control parameters                |
| 7          | MRSPCT11      | 000Dh            | Speed curve parameters                  |
| 8          | MRSPCT19      | 0015h            | BEMF window parameters                  |
| 9          | MRDIAG0       | 0201h            | Diagnosis flags                         |
| 10         | MRSTAT0       | 0205h            | Status                                  |
| 11         | MRRST         | 0300h            | Reset related                           |
| 12         | MRCTL0        | 0301h            | PWM duty cycle input                    |
| 13         | MRCTL2        | 0303h            | commutation parameter                   |
| 14         | MRCTL5        | 0306h            | STATUS selection                        |
| 15         | Selectable    | Selectable       | Any register selected with the register |

The base address is the first one, and the consecutive multiple address can be accessed by setting the bit-field "LENGTH[2:0]".

For example, to write the duty cycle data to the register PWMDTIN[9:0] (located in MRCTL0 0301h and MRCTL1 0302h), the following three data patterns are applicable and typical.

1. Writing twice by one byte (total 64 bits)

**Table 8.**

| 1  | 2      | 3 | 4 | 5     | 6 | 7 | 8 | 9 to 16       | 17 to 24     | 25 to 32     |
|----|--------|---|---|-------|---|---|---|---------------|--------------|--------------|
| WR | Length |   |   | BASEL |   |   |   | Address[15:8] | Address[7:0] | Data LSB     |
| 1  | 0      | 0 | 0 | 0     | 0 | 0 | 0 | 03            | 01h          | PWMDTIN[7:0] |

**Table 9.**

| 33 | 34     | 35 | 36 | 37    | 38 | 39 | 40 | 41 to 48      | 49 to 56     | 57 to 64     |
|----|--------|----|----|-------|----|----|----|---------------|--------------|--------------|
| WR | Length |    |    | BASEL |    |    |    | Address[15:8] | Address[7:0] | Data MSB     |
| 1  | 0      | 0  | 0  | 0     | 0  | 0  | 0  | 03h           | 02h          | PWMDTIN[9:8] |

2. Writing once by two-byte with the full address (total 40 bits)

**Table 10.**

| 1  | 2      | 3 | 4 | 5     | 6 | 7 | 8 | 9 to 16       | 17 to 24     | 25 to 32     | 33 to 40     |
|----|--------|---|---|-------|---|---|---|---------------|--------------|--------------|--------------|
| WR | Length |   |   | BASEL |   |   |   | Address[15:8] | Address[7:0] | Data LSB     | Data MSB     |
| 1  | 0      | 0 | 1 | 0     | 0 | 0 | 0 | 03h           | 01h          | PWMDTIN[7:0] | PWMDTIN[9:8] |

3. Writing once by two-byte with the base address (total 24 bits)

Table 11.

|    |        |   |   |       |   |   |   |              |              |
|----|--------|---|---|-------|---|---|---|--------------|--------------|
| 1  | 2      | 3 | 4 | 5     | 6 | 7 | 8 | 9 to 16      | 17 to 24     |
| WR | Length |   |   | BASEL |   |   |   | Data LSB     | Data MSB     |
| 1  | 0      | 0 | 1 | 1     | 1 | 0 | 0 | PWMDTIN[7:0] | PWMDTIN[9:8] |

Where, the bit sequence of data bytes is;

Table 12.

|             |                 |                 |                 |                 |                 |                 |                 |                 |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| sequence    | 1 <sup>st</sup> | 2 <sup>nd</sup> | 3 <sup>rd</sup> | 4 <sup>th</sup> | 5 <sup>th</sup> | 6 <sup>th</sup> | 7 <sup>th</sup> | 8 <sup>th</sup> |
| PWMDTIN LSB | [7]             | [6]             | [5]             | [4]             | [3]             | [2]             | [1]             | [0]             |

Table 13.

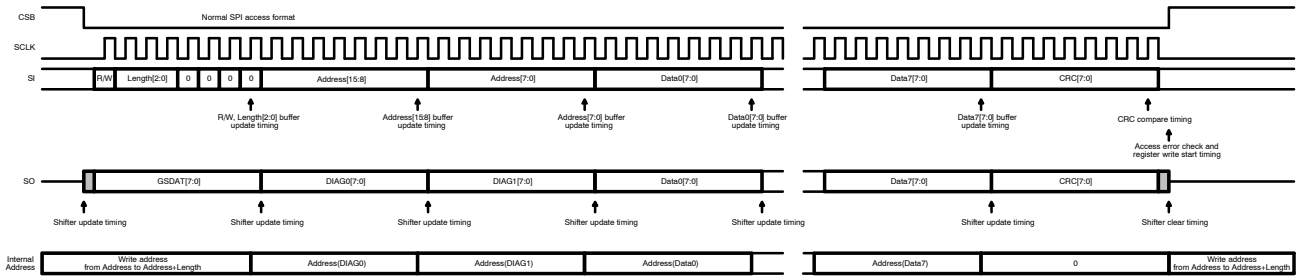
|             |                 |                 |                 |                 |                 |                 |                 |                 |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| sequence    | 1 <sup>st</sup> | 2 <sup>nd</sup> | 3 <sup>rd</sup> | 4 <sup>th</sup> | 5 <sup>th</sup> | 6 <sup>th</sup> | 7 <sup>th</sup> | 8 <sup>th</sup> |
| PWMDTIN MSB | NA              | NA              | NA              | NA              | NA              | NA              | [9]             | [8]             |

There are two items to be especially careful of with the general communication scheme:

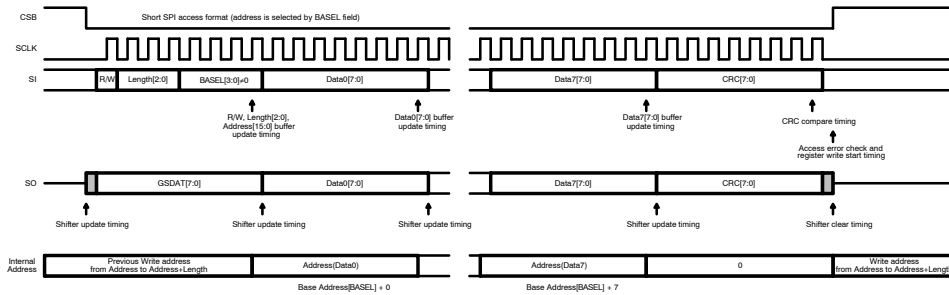
1. Communications must be full duplex and simultaneous. It is not allowed to send one transaction and then read data on a second transaction as the status register information will be updated on the first transaction and then be out of date for the second. Some systems break transactions into separate read and write operations which is not acceptable with the LV8961H.
2. It is important the system master uses the clock and data polarities and phases as shown above. Both the clock and data on some systems can be

inverted for various reasons but must arrive at the LV8961H per the above drawing. Common errors include SCLK inversion such that the leading edge arrives as a downward transition rather than a rising edge, or having the data to clock phase incorrect. Data phase must be such that the data only changes during a clock falling edge and is completely stable during a clock rising edge. This means a good margin of one half of a bit time exists to eliminate transmission delay hazards.

The first byte returned on all transactions is always the status register, GSDAT, and contains information such as the busy flag during programming operations.



Format 1 : Normal SPI access format



Format 2 : Short SPI access format

Figure 19. SPI Format

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The header byte structure of the SPI format can be described by the following C language program.

```
enum readwrite {RD, WR};
enum regCount {cnt1, cnt2, cnt3, cnt4, cnt5, cnt6, cnt7, cnt8};
enum baseReg {na, MRACK0, MRSPCT0, MRSPCT1, MRSPCT3, MRSPCT7, MRSPCT10, MRSPCT11, \
  MRSPCT19, MRDIAG0, MRSTAT0, MRRST, MRCTL0, MRCTL2, MRCTL5, BY_BAREG};

union {
  uint8_t bitwise;
  struct {
    baseReg   BASEL: 4;
    regCount  Length: 3;
    readwrite RW: 1;
  };
} header;
```

The checksum (CRC) code of the SPI data train is calculated by the following function.

```
#define CHAR_BIT      8          /* number of bits in a char */
#define MSB_CRC8      (0x4D)    /* polynomial*/

uint8_t GetCRC8_2(uint8_t seed, const void *buff, size_t data_size)
{
  uint8_t *p = (uint8_t *)buff;
  uint8_t crc8;
  int i;

  for (crc8 = seed; data_size != 0; data_size--){
    crc8 ^= *p++;

    for (i = 0; i < CHAR_BIT; i++){
      if (crc8 & 0x80){
        crc8 <<= 1; crc8 ^= MSB_CRC8;
      }
      else{
        crc8 <<= 1;
      }
    }
  }
  return crc8;
}
```

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An example SPI communication is shown below. It shows the case that the two bytes from the register MRACK0 within one transaction, using the base address scheme.

```
uint8_t SPI_WR_BUF[32];
uint8_t SPI_RD_BUF[32];

void example_main()
{
    int i;

    header.RW = RD;           /* read */
    header.Length = cnt2;     /* 2 bytes */
    header.BASEL = MRACK0;   /* from MRACK0 */
    Serial.print("Header = ");
    Serial.print(header.bytwise, HEX);
    Serial.println("h");

    SPI_WR_BUF[0] = header.bytwise;
    SPI_WR_BUF[1] = 0;        /* dummy data */
    SPI_WR_BUF[2] = 0;        /* dummy data */
    SPI_WR_BUF[3] = GetCRC8_2((uint8_t)0, SPI_WR_BUF, 3);
    Serial.print("CRC = ");
    Serial.print(SPI_WR_BUF[3], HEX);
    Serial.println("h");

    digitalWrite(CSB_pin, LOW);
    for (i = 0; i < 4; ++i)
    {
        SPI_RD_BUF[i] = SPI.transfer(SPI_WR_BUF[i]);
        Serial.print(SPI_WR_BUF[i], HEX); Serial.print("h, ");
        Serial.print(SPI_RD_BUF[i], HEX); Serial.println("h");
    }
    digitalWrite(CSB_pin, HIGH);
}
```

This output is shown below.

```
Header = 11h
CRC = 66h

WR,  RD
11h, 02h
00h, 55h
00h, AAh
66h, B3h
```

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### GSDAT Field

Global status is always output to this field. Global status contains following information.

#### GSDAT[7:0]

| Bit 7 | 6    | 5     | 4     | 3    | 2         | 1 | Bit 0 |                                 |
|-------|------|-------|-------|------|-----------|---|-------|---------------------------------|
| ORBEN | SACF | DIAGS | LATCH | OBSY | SMOD[2:0] |   |       |                                 |
|       |      |       |       |      | 0         | 0 | 0     | Sleep mode                      |
|       |      |       |       |      | 0         | 0 | 1     | Device startup time             |
|       |      |       |       |      | 0         | 1 | 0     | Standby mode                    |
|       |      |       |       |      | 0         | 1 | 1     | N/A                             |
|       |      |       |       |      | 1         | 0 | 0     | N/A                             |
|       |      |       |       |      | 1         | 0 | 1     | Normal mode without FG output   |
|       |      |       |       |      | 1         | 1 | 0     | Normal mode with FG output      |
|       |      |       |       |      | 1         | 1 | 1     | Sleep mode                      |
| 0     | x    | 0     | 0     | 0    | x         | x | x     | Normal operation                |
|       |      |       |       | 1    |           |   |       | OTP busy with read/write access |
|       |      |       | 1     |      |           |   |       | Latched shutdown condition      |
|       |      | 1     |       |      |           |   |       | Failure condition               |
|       | 0    |       |       |      |           |   |       | Last SPI access OK              |
|       | 1    |       |       |      |           |   |       | Last SPI access failed*         |
| 1     |      |       |       |      |           |   |       | OTP integrity test mode         |

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The following SPI failures are detectable and reported collectively in GSDAT as general SPI failures:

- Any access to an address which are outside the defined address space
- The number of SCLK transitions is not 16 within one word transfer
- Any access to MRCONF, MRACS, ORCONF, ORACS while OBSY = 1 (during write operations)
- Write access to MRODL register while OBSY=1 (during write operations)
- Write access to any of the main registers after setting MSAENB = 1 (Implies MRxxxx registers are locked)
- Write access to any of the OTP registers after OSAENB = 1 (Implies ORxxxx registers are locked)
- Write access attempt to a read-only or locked register
- SI signal changed at positive edge of SCLK (Incorrect data/sclk phase setup)

### SPI Timing

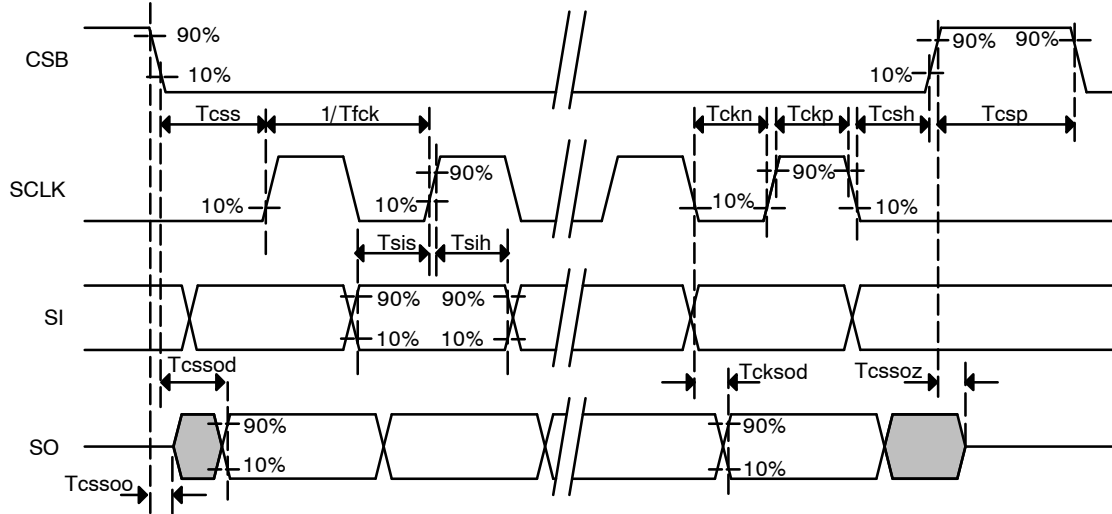


Figure 20. SPI Timing Chart

### SPI TIMING

( $T_J = -40$  to  $150^\circ\text{C}$ ,  $V_S = 4.5$  to  $28$  V, Pull-up resistance of SO pin =  $2.4$  k $\Omega$ , Output load of SO pin =  $30$  pF)

| Symbol | Comment                             | Min  | Typ | Max | Unit |
|--------|-------------------------------------|------|-----|-----|------|
| Tfck   | SCLK clock frequency                |      |     | 500 | kHz  |
| Tckp   | SCLK high pulse width               | 950  |     |     | ns   |
| Tckn   | SCLK low pulse width                | 950  |     |     | ns   |
| Tcss   | CSB setup time                      | 950  |     |     | ns   |
| Tcsh   | CSB hold time                       | 950  |     |     | ns   |
| Tcsp   | CSB high pulse width                | 1900 |     |     | ns   |
| Tsis   | SI setup time                       | 450  |     |     | ns   |
| Tsih   | SI hold time                        | 450  |     |     | ns   |
| Tcssod | CSB fall edge to SO delay time      |      |     | 950 | ns   |
| Tcksod | SCLK fall edge to SO delay time     |      |     | 950 | ns   |
| Tcssoo | CSB fall edge to SO data out time   | 0    |     |     | ns   |
| Tcssoz | CSB rise edge to SO High Z out time |      |     | 950 | ns   |



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## Register Description

### SPI Register Map

The SPI interface allows read access to the entire address space of the main registers. The main registers can only be

written in Standby mode and then only if the write lock bit MSAENB has never been set high.

### SPEED CONTROL OVERVIEW

| Write Enable | Limitation by OBSY | ADDR      | Data Name | D[7]                | D[6]          | D[5]                | D[4]           | D[3]                | D[2]      | D[1]                | D[0] |              |        |
|--------------|--------------------|-----------|-----------|---------------------|---------------|---------------------|----------------|---------------------|-----------|---------------------|------|--------------|--------|
| Read-Only    | Read-Only          | -         | GSDAT     | ORBEN               | SACF          | DIAGS               | LATCH          | OBSY                | SMOD[2:0] |                     |      |              |        |
| Read-Only    | Read-Only          | 0000h     | MRACK0    | 0                   | 1             | 0                   | 1              | 0                   | 1         | 0                   | 1    |              |        |
|              |                    | 0001h     | MRACK1    | 1                   | 0             | 1                   | 0              | 1                   | 0         | 1                   | 0    |              |        |
| MSAENB=L     | OBSY=L             | 0002h     | MRSPCT0   | 0                   | 0             | CLSEL               | CLDWN OFF      | OCSEL[1:0]          |           | CLMSPD[1:0]         |      |              |        |
|              |                    | 0003h     | MRSPCT1   | 0                   | 0             | SSTT[5:0]           |                |                     |           |                     |      |              |        |
|              |                    | 0004h     | MRSPCT2   | STOSC[7:0]          |               |                     |                |                     |           |                     |      |              |        |
|              |                    | 0005h     | MRSPCT3   | SLMD                | 0             | 0                   | LASET_L[4:0]   |                     |           |                     |      |              |        |
|              |                    | 0006h     | MRSPCT4   | 0                   | 0             | 0                   | LASET_H[4:0]   |                     |           |                     |      |              |        |
|              |                    | 0007h     | MRSPCT5   | 0                   | 0             | 0                   | LASET_LIM[4:0] |                     |           |                     |      |              |        |
|              |                    | 0008h     | MRSPCT6   | MSKRSTNUM0_SIX[3:0] |               |                     |                | MSKRSTNUM1_SIX[3:0] |           |                     |      |              |        |
|              |                    | 0009h     | MRSPCT7   | 0                   | PX[2:0]       |                     |                | 0                   | PG[2:0]   |                     |      |              |        |
|              |                    | 000Ah     | MRSPCT8   | IX[3:0]             |               |                     |                | 0                   | IG[2:0]   |                     |      |              |        |
|              |                    | 000Ch     | MRSPCT10  | 0                   | DDUTYSEL[2:0] |                     |                | USTEPSEL[1:0]       |           | DSTEPSEL[1:0]       |      |              |        |
|              |                    | 000Dh     | MRSPCT11  | DUTY_L[7:0]         |               |                     |                |                     |           |                     |      |              |        |
|              |                    | 000Eh     | MRSPCT12  | DUTY_H[7:0]         |               |                     |                |                     |           |                     |      |              |        |
|              |                    | 000Fh     | MRSPCT13  | TAG_L[7:0]          |               |                     |                |                     |           |                     |      |              |        |
|              |                    | 0010h     | MRSPCT14  | 0                   | TAG_L[14:8]   |                     |                |                     |           |                     |      |              |        |
|              |                    | 0011h     | MRSPCT15  | TAG_H[7:0]          |               |                     |                |                     |           |                     |      |              |        |
|              |                    | 0012h     | MRSPCT16  | 0                   | TAG_H[14:8]   |                     |                |                     |           |                     |      |              |        |
|              |                    | Always OK |           | 0013h               | MRSPCT17      | 0                   | 0              | 0                   | 0         | 0                   | 0    | 0            | RECALC |
|              |                    | MSAENB=L  |           | 0015h               | MRSPCT19      | 0                   | 0              | 0                   | 0         | 0                   | 0    | WINDSEL[1:0] |        |
|              |                    |           |           | 0016h               | MRSPCT20      | MSKRSTNUM0_INI[3:0] |                |                     |           | MSKRSTNUM1_INI[3:0] |      |              |        |
|              |                    |           |           | 0017h               | MRSPCT21      | MSKRSTNUM0_THR[3:0] |                |                     |           | MSKRSTNUM1_THR[3:0] |      |              |        |
|              | 0018h              |           | MRSPCT22  | MSKRSTNUM0_TWO[3:0] |               |                     |                | MSKRSTNUM1_TWO[3:0] |           |                     |      |              |        |
|              | 0019h              |           | MRSPCT23  | MSKRSTNUM0_ONE[3:0] |               |                     |                | MSKRSTNUM1_ONE[3:0] |           |                     |      |              |        |
|              | 001Ah              |           | MRSPCT24  | 0                   | 0             | 0                   | 0              | 0                   | 0         | 0                   | 0    | RBSEL        |        |

### MRACK0

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|------|------|------|------|------|------|------|
| 0000h | MRACK0    | 0    | 1    | 0    | 1    | 0    | 1    | 0    | 1    |

**MRACK0[7:0]: Main Register Access Check**  
MRACK0[7:0] read data is fixed to 55h

This read-only register is used to check IC and SPI interface. 55h is read from this register in standby and normal mode, FFh during sleep mode.

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## MRACK1

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|------|------|------|------|------|------|------|
| 0001h | MRACK1    | 1    | 0    | 1    | 0    | 1    | 0    | 1    | 0    |

**MRACK1[7:0]: Main Register Access Check**  
MRACK1[7:0] read data is fixed to AAh

This read-only register is used to check IC and SPI interface. AAh is read from this register in standby and normal mode, FFh during sleep mode.

## MRSPT0 (DEFAULT: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5]  | D[4]     | D[3]       | D[2] | D[1]        | D[0] |
|-------|-----------|------|------|-------|----------|------------|------|-------------|------|
| 0002h | MRSPT0    | 0    | 0    | CLSEL | CLDWNOFF | OCSEL[1:0] |      | CLMSPD[1:0] |      |

**CLSEL: Current Limit threshold SElection**  
CLSEL=0: Threshold voltage 50 mV  
CLSEL=1: Threshold voltage 100 mV

**CLDWNOFF: Current Limit semi-powerDoWN OFF**  
CLDWNOFF=0: function ON  
CLDWNOFF=1: function OFF

**OCSEL[1:0]: OverCurrent threshold SElection**  
CLSEL=0  
OCSEL[1:0]=0h: Threshold voltage 75 mV  
OCSEL[1:0]=1h: Threshold voltage 100 mV  
OCSEL[1:0]=2h: Threshold voltage 125 mV

OCSEL[1:0]=3h: Threshold voltage 150 mV  
CLSEL=1  
OCSEL[1:0]=0h: Threshold voltage 125 mV  
OCSEL[1:0]=1h: Threshold voltage 150 mV  
OCSEL[1:0]=2h: Threshold voltage 175 mV  
OCSEL[1:0]=3h: Threshold voltage 200 mV

**CLMSPD[1:0]: Current LiMit Semi-PowerDown level**  
CLMSPD[1:0]=0h: 0.1%  
CLMSPD[1:0]=1h: 1.3%  
CLMSPD[1:0]=2h: 2.5%  
CLMSPD[1:0]=3h: 5.07%

## MRSPT1 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5]      | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|------|-----------|------|------|------|------|------|
| 0003h | MRSPT1    | 0    | 0    | SSTT[5:0] |      |      |      |      |      |

**SSTT[5:0]: Soft Start Time**  
SSTT[5:0]=00h: Soft start time 0.102 s  
SSTT[5:0]=x: Soft start time  $0.102 * (1 + x)$  s  
SSTT[5:0]=3Fh: Soft start time 6.55 s  
Soft start allows startup of motors with higher inertia by ramping the current. The soft start algorithm divides the

current limit voltage 100 mV (Typ) into 16 sections and increases the value from 6.25 mV to 100 mV to switch over the current limit value. Case of 50 mV, increases the value from 3.125 mV to 50 mV.

## MRSPT2 (Default: 00h)

| ADDR  | Data Name | D[7]       | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------------|------|------|------|------|------|------|------|
| 0004h | MRSPT2    | STOSC[7:0] |      |      |      |      |      |      |      |

**STOSC[7:0]: SStartup OSCillator**  
STOSC[7:0]=00h: 1.024 ms

STOSC[7:0]=x:  $1.024 * (1 + x)$  ms  
STOSC[7:0]=FFh: 262.14 ms

## MRSPT3 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4]         | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|------|------|--------------|------|------|------|------|
| 0005h | MRSPT3    | SLMD | 0    | 0    | LASET_L[4:0] |      |      |      |      |

**SLMD: Sinusoidal Mode Driving**  
SLMD=0: Trapezoidal drive with 120 degrees energization.  
SLMD=1: Sinusoidal drive with 6 windows BEMF detection.

This bit selects whether the motor phases are driven with a trapezoidal or sinusoidal signal.

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*LASET\_L[4:0]: Lead Angle SETting at Low output duty cycle (0%)*

- LASET\_L[4:0]=00h: Lead angle 0 deg.
- LASET\_L[4:0]=x: Lead angle (x \* 1.875) deg
- LASET\_L[4:0]=1Fh: Lead angle 58.125 deg.

It is possible to advance the commutation point towards zero-crossing of the BEMF signal. This helps to achieve BEMF field-weakening for higher rotational speeds and to compensate for delays in high speed operation.

### MRSPT4 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4]         | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|------|------|--------------|------|------|------|------|
| 0006h | MRSPT4    | 0    | 0    | 0    | LASET_H[4:0] |      |      |      |      |

*LASET\_H[4:0]: Lead Angle SETting at High output duty cycle (100%)*

- LASET\_H[4:0]=00h: Lead angle 0 deg.
- LASET\_H[4:0]=x: Lead angle (x \* 1.875) deg
- LASET\_H[4:0]=1Fh: Lead angle 58.125 deg.

It is possible to advance the commutation point towards zero-crossing of the BEMF signal. This helps to achieve BEMF field-weakening for higher rotational speeds and to compensate for delays in high speed operation.

### MRSPT5 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4]           | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|------|------|----------------|------|------|------|------|
| 0007h | MRSPT5    | 0    | 0    | 0    | LASET_LIM[4:0] |      |      |      |      |

*LASET\_LIM[4:0]: Lead Angle SETting max. LIMit*

- LASET\_LIM[4:0]=00h: Lead angle 0 deg.
- LASET\_LIM[4:0]=x: Lead angle (x \* 1.875) deg
- LASET\_LIM[4:0]=1Fh: Lead angle 58.125 deg.

It is possible to advance the commutation point towards zero-crossing of the BEMF signal. This helps to achieve BEMF field-weakening for higher rotational speeds and to compensate for delays in high speed operation.

### MRSPT6 (Default: 00h)

| ADDR  | Data Name | D[7]                | D[6] | D[5] | D[4] | D[3]                | D[2] | D[1] | D[0] |  |
|-------|-----------|---------------------|------|------|------|---------------------|------|------|------|--|
| 0008h | MRSPT6    | MSKRSTNUM0_SIX[3:0] |      |      |      | MSKRSTNUM1_SIX[3:0] |      |      |      |  |

*MSKRSTNUM0\_SIX[3:0]: MaSK Rate SeTting for bemf observation NUMber 0 for 6-window mode*

- MSKRSTNUM0\_SIX[3:0]= x:
- (x < 8) -> (15 + x \* 3.75) deg.
- (x ≥ 8) -> (41.25 + (x - 7) \* 1.875) deg.

*MSKRSTNUM1\_SIX[3:0]: MaSK Rate SeTting for bemf observation NUMber 1 for 6-window mode*

- MSKRSTNUM1\_SIX[3:0]=x:
- ((x + 1) \* 1.875) deg.

### MRSPT7 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6]    | D[5] | D[4] | D[3] | D[2]    | D[1] | D[0] |
|-------|-----------|------|---------|------|------|------|---------|------|------|
| 0009h | MRSPT7    | 0    | PX[2:0] |      |      | 0    | PG[2:0] |      |      |

*PX[2:0]: Proportional gain eXponent*

- PX[2:0]=0h: Proportional gain 1 (through)
- PX[2:0]=1h: Proportional gain 2
- PX[2:0]=2h: Proportional gain 4
- PX[2:0]=3h: Proportional gain 8
- PX[2:0]=4h: Proportional gain 16
- PX[2:0]=5h: Proportional gain 32
- PX[2:0]=6h: Proportional gain 64
- PX[2:0]=7h: Proportional gain 0 (cut)

*PG[2:0]: Proportional Gain*

- PG[2:0]=0h: Proportional gain 1 (through)
- PG[2:0]=1h: Proportional gain 7/8
- PG[2:0]=2h: Proportional gain 6/8
- PG[2:0]=3h: Proportional gain 5/8
- PG[2:0]=4h: Proportional gain 4/8
- PG[2:0]=5h: Proportional gain 3/8
- PG[2:0]=6h: Proportional gain 2/8
- PG[2:0]=7h: Proportional gain 1/8

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## MRSPT8 (Default: 00h)

| ADDR  | Data Name | D[7]    | D[6] | D[5] | D[4] | D[3] | D[2]    | D[1] | D[0] |
|-------|-----------|---------|------|------|------|------|---------|------|------|
| 000Ah | MRSPT8    | IX[3:0] |      |      |      | 0    | IG[2:0] |      |      |

### IX[3:0]: Integral gain eXponent

IX[3:0]=0h: Integral gain 1 (through)  
 IX[3:0]=1h: Integral gain 2  
 IX[3:0]=2h: Integral gain 4  
 IX[3:0]=3h: Integral gain 8  
 IX[3:0]=4h: Integral gain 16  
 IX[3:0]=5h: Integral gain 32  
 IX[3:0]=6h: Integral gain 64  
 IX[3:0]=7h: Integral gain 0 (cut)  
 IX[3:0]=8h: Integral gain 1 (through)  
 IX[3:0]=9h: Integral gain 1/2  
 IX[3:0]=Ah: Integral gain 1/4  
 IX[3:0]=Bh: Integral gain 1/8  
 IX[3:0]=Ch: Integral gain 1/16  
 IX[3:0]=Dh: Integral gain 1/32  
 IX[3:0]=Eh: Integral gain 1/64  
 IX[3:0]=Fh: Integral gain 0 (cut)

### IG[2:0]: Integral Gain

IG[2:0]=0h: Integral gain 1 (through)  
 IG[2:0]=1h: Integral gain 7/8  
 IG[2:0]=2h: Integral gain 6/8  
 IG[2:0]=3h: Integral gain 5/8  
 IG[2:0]=4h: Integral gain 4/8  
 IG[2:0]=5h: Integral gain 3/8  
 IG[2:0]=6h: Integral gain 2/8  
 IG[2:0]=7h: Integral gain 1/8

## MRSPT10 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6]          | D[5] | D[4]          | D[3] | D[2]          | D[1] | D[0] |
|-------|-----------|------|---------------|------|---------------|------|---------------|------|------|
| 000Ch | MRSPT10   | 0    | DDUTYSEL[2:0] |      | USTEPSEL[1:0] |      | DSTEPSEL[1:0] |      |      |

### DDUTYSEL[2:0]: Detection level of DUTY output changes SElection

DDUTYSEL[2:0]=0h: No limitation.  
 DDUTYSEL[2:0]=1h: Limit to  $\pm 20.3\%$  ( $\pm 208$ )  
 DDUTYSEL[2:0]=2h: Limit to  $\pm 17.8\%$  ( $\pm 182$ )  
 DDUTYSEL[2:0]=3h: Limit to  $\pm 15.2\%$  ( $\pm 156$ )  
 DDUTYSEL[2:0]=4h: Limit to  $\pm 12.7\%$  ( $\pm 130$ )  
 DDUTYSEL[2:0]=5h: Limit to  $\pm 10.2\%$  ( $\pm 104$ )  
 DDUTYSEL[2:0]=6h: Limit to  $\pm 7.6\%$  ( $\pm 78$ )  
 DDUTYSEL[2:0]=7h: Limit to  $\pm 5.1\%$  ( $\pm 52$ )

### USTEPSEL[1:0]: UpSpeed Transition stEP SElectio. (Case of Motor is 2 poles)

USTEPSEL[1:0]=0h: max. 32766 rpm.  
 USTEPSEL[1:0]=1h: Upper limit is 400% of current speed and max. 32766 rpm.

USTEPSEL[1:0]=2h: Upper limit is current speed and max. 16384 rpm.

USTEPSEL[1:0]=3h: Upper limit is 25% of current speed and max. 4096 rpm.

### DSTEPSEL[1:0]: DownSpeed Transition stEP SElection. (Case of Motor is 2 poles)

DSTEPSEL[1:0]=0h: Upper limit is current speed and max. 32766 rpm.

DSTEPSEL[1:0]=1h: Upper limit is 25% of current speed and max. 4096 rpm.

DSTEPSEL[1:0]=2h: Upper limit is 6.25% of current speed and max. 1024 rpm.

DSTEPSEL[1:0]=3h: Upper limit is 1.5625% of current speed and max. 256 rpm.

## MRSPT11 (Default: 00h)

| ADDR  | Data Name | D[7]        | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|-------------|------|------|------|------|------|------|------|
| 000Dh | MRSPT11   | DUTY_L[7:0] |      |      |      |      |      |      |      |

### DUTY\_L[7:0]: input pwm DUTY cycle Low limit

DUTY\_L[7:0]=00h: Lower limit 0.098%  
 DUTY\_L[7:0]=x:

Lower limit  $((x * 2 + 1) * 100 / 1024) \%$   
 DUTY\_L[7:0]=FFh: Lower Limit 49.9%

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### MRSPT12 (Default: 00h)

| ADDR  | Data Name | D[7]        | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|-------------|------|------|------|------|------|------|------|
| 000Eh | MRSPT12   | DUTY_H[7:0] |      |      |      |      |      |      |      |

*DUTY\_H[7:0]: input pwm DUTY cycle High limit*  
 DUTY\_H[7:0]=00h: Upper limit 50%  
 DUTY\_H[7:0]=x:

Upper limit  $((x * 2) * 100 / 1024 + 50) \%$   
 DUTY\_H[7:0]=FEh: Upper Limit 99.6%  
 DUTY\_H[7:0]=FFh: Upper Limit 99.9%

### MRSPT13 (Default: 00h)

| ADDR  | Data Name | D[7]       | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------------|------|------|------|------|------|------|------|
| 000Fh | MRSPT13   | TAG_L[7:0] |      |      |      |      |      |      |      |

### MRSPT14 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6]        | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|-------------|------|------|------|------|------|------|
| 0010h | MRSPT14   | 0    | TAG_L[14:8] |      |      |      |      |      |      |

*TAG\_L[14:0]: TArGet speed Low.*  
 (Case of Motor is 2 poles)

SCEN=0 (Closed-loop)  
 TAG\_L[14:0]=0000h: Lower limit 0 rpm  
 TAG\_L[14:0]=0001h: Lower limit 2 rpm  
 TAG\_L[14:0]=x:  
 (x ≥ 4E20h) → Lower limit 40000 rpm  
 (x < 4E20h) → Lower limit x \* 2 rpm

TAG\_L[14:0]=7FFEh: Lower Limit 40000 rpm  
 TAG\_L[14:0]=7FFFh: Lower Limit 40000 rpm  
 SCEN=1 (Open-loop)  
 Ignore TAG\_L  
 0% duty output is fixed.

### MRSPT15 (Default: 00h)

| ADDR  | Data Name | D[7]       | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------------|------|------|------|------|------|------|------|
| 0011h | MRSPT15   | TAG_H[7:0] |      |      |      |      |      |      |      |

### MRSPT16 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6]        | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------|-------------|------|------|------|------|------|------|
| 0012h | MRSPT16   | 0    | TAG_H[14:8] |      |      |      |      |      |      |

*TAG\_H[14:0]: TArGet speed High.*  
 (Case of Motor is 2 poles)

SCEN=0 (Closed-loop)  
 TAG\_H[14:0]=0000h: Upper limit 0 rpm  
 TAG\_H[14:0]=0001h: Upper limit 2 rpm  
 TAG\_H[14:0]=x:  
 (x ≥ 4E20h) → Upper limit 40000 rpm  
 (x < 4E20h) → Upper limit x \* 2 rpm

TAG\_H[14:0]=7FFEh: Upper Limit 40000 rpm  
 TAG\_H[14:0]=7FFFh: Upper Limit 40000 rpm  
 SCEN=1 (Open-loop)  
 Ignore TAG\_H  
 100% duty output is fixed.

### MRSPT17 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0]   |
|-------|-----------|------|------|------|------|------|------|------|--------|
| 0013h | MRSPT17   | 0    | 0    | 0    | 0    | 0    | 0    | 0    | RECALC |

*RECALC: RECALCulate target speed from input pwm control table*  
 RECALC=0: No operation.

RECALC=1: Update latched values (SCEN, DUTY\_L, DUTY\_H, TAG\_L and TAG\_H) in the target speed calculation module and RECALC will be cleared automatically.

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## MRSPT19 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1]         | D[0] |
|-------|-----------|------|------|------|------|------|------|--------------|------|
| 0015h | MRSPCT19  | 0    | 0    | 0    | 0    | 0    | 0    | WINDSEL[1:0] |      |

WINDSEL[1:0]: Bemf WINDow mode SELECTION

WINDSEL[1:0]=0h: 6-window

WINDSEL[1:0]=1h: 3-window

WINDSEL[1:0]=2h: 2-window

WINDSEL[1:0]=3h: 1-window

## MRSPT20 (Default: 00h)

| ADDR  | Data Name | D[7]                | D[6] | D[5] | D[4] | D[3]                | D[2] | D[1] | D[0] |
|-------|-----------|---------------------|------|------|------|---------------------|------|------|------|
| 0016h | MRSPCT20  | MSKRSTNUM0_INI[3:0] |      |      |      | MSKRSTNUM1_INI[3:0] |      |      |      |

MSKRSTNUM0\_INI[3:0]: MaSK Rate SeTting for bemf observation NUMber 0 for startup 6-window mode

MSKRSTNUM0\_INI[3:0]=x:

(x < 8) -> (15 + x \* 3.75) deg.

(x ≥ 8) -> (41.25 + (x - 7) \* 1.875) deg.

MSKRSTNUM1\_INI[3:0]: MaSK Rate SeTting for bemf observation NUMber 1 for startup 6-window mode

MSKRSTNUM1\_INI[3:0]=x: ((x + 1) \* 1.875) deg.

## MRSPT21 (Default: 00h)

| ADDR  | Data Name | D[7]                | D[6] | D[5] | D[4] | D[3]                | D[2] | D[1] | D[0] |
|-------|-----------|---------------------|------|------|------|---------------------|------|------|------|
| 0017h | MRSPCT21  | MSKRSTNUM0_THR[3:0] |      |      |      | MSKRSTNUM1_THR[3:0] |      |      |      |

MSKRSTNUM0\_THR[3:0]: MaSK Rate SeTting for bemf observation NUMber 0 for 3-window mode

MSKRSTNUM0\_THR[3:0]=x:

(x < 8) -> (15 + x \* 3.75) deg.

(x ≥ 8) -> (41.25 + (x - 7) \* 1.875) deg.

MSKRSTNUM1\_THR[3:0]: MaSK Rate SeTting for bemf observation NUMber 1 for 3-window mode

MSKRSTNUM1\_THR[3:0]=x: ((x + 1) \* 1.875) deg.

## MRSPT22 (Default: 00h)

| ADDR  | Data Name | D[7]                | D[6] | D[5] | D[4] | D[3]                | D[2] | D[1] | D[0] |
|-------|-----------|---------------------|------|------|------|---------------------|------|------|------|
| 0018h | MRSPCT22  | MSKRSTNUM0_TWO[3:0] |      |      |      | MSKRSTNUM1_TWO[3:0] |      |      |      |

MSKRSTNUM0\_TWO[3:0]: MaSK Rate SeTting for bemf observation NUMber 0 for 2-window mode

MSKRSTNUM0\_TWO[3:0]=x:

(x < 8) -> (15 + x \* 3.75) deg.

(x ≥ 8) -> (41.25 + (x - 7) \* 1.875) deg.

MSKRSTNUM1\_TWO[3:0]: MaSK Rate SeTting for bemf observation NUMber 1 for 2-window mode

MSKRSTNUM1\_TWO[3:0]=x: ((x + 1) \* 1.875) deg.

## MRSPT23 (Default: 00h)

| ADDR  | Data Name | D[7]                | D[6] | D[5] | D[4] | D[3]                | D[2] | D[1] | D[0] |
|-------|-----------|---------------------|------|------|------|---------------------|------|------|------|
| 0019h | MRSPCT23  | MSKRSTNUM0_ONE[3:0] |      |      |      | MSKRSTNUM1_ONE[3:0] |      |      |      |

MSKRSTNUM0\_ONE[3:0]: MaSK Rate SeTting for bemf observation NUMber 0 for 1-window mode

MSKRSTNUM0\_ONE[3:0]=x:

(x < 8) -> (15 + x \* 3.75) deg.

(x ≥ 8) -> (41.25 + (x - 7) \* 1.875) deg.

MSKRSTNUM1\_ONE[3:0]: MaSK Rate SeTting for bemf observation NUMber 1 for 1-window mode

MSKRSTNUM1\_ONE[3:0]=x: ((x + 1) \* 1.875) deg.

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### MRSPT24 (DEFAULT: 00H)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0]  |
|-------|-----------|------|------|------|------|------|------|------|-------|
| 001Ah | MRSPCT24  | 0    | 0    | 0    | 0    | 0    | 0    | 0    | RBSEL |

*RBSEL*: Reverse detection Brake SElection

RBSEL=0: Short brake is disabled when reverse rotation is detected.

RBSEL=1: Short brake is enabled when reverse rotation is detected.

If RBSEL is set, short brake (all low-side FET are ON) is done until the rotation stops after reverse rotation is detected.

### MOTOR CONFIGURATION REGISTER OVERVIEW

| Write Enable    | Limitation by OBSY | ADDR  | Data Name | D[7]        | D[6]         | D[5]         | D[4]          | D[3]         | D[2]      | D[1]         | D[0]      |  |
|-----------------|--------------------|-------|-----------|-------------|--------------|--------------|---------------|--------------|-----------|--------------|-----------|--|
| MSAENB=L & EN=L | OBSY=L             | 0100h | MRCONF0   | FRMD        | FRREN        | SCEN         | PWMF          | REGSEL       | VCEN      | SPCFG        | PWMIN SEL |  |
|                 |                    | 0101h | MRCONF1   | FLSEL[2:0]  |              |              | ZPSEL[2:0]    |              |           | PDTC         | PWM ON    |  |
|                 |                    | 0102h | MRCONF2   | FGST BLMD   | FGOF[1:0]    |              | FDTI[4:0]     |              |           |              |           |  |
|                 |                    | 0103h | MRCONF3   | CLMASK[3:0] |              |              |               | OCMASK[3:0]  |           |              |           |  |
|                 |                    | 0104h | MRCONF4   | SROFFT[3:0] |              |              |               | CRMASK[3:0]  |           |              |           |  |
|                 |                    | 0105h | MRCONF5   | SYNC EN     | PPDO SEL     | FSCDT[1:0]   |               | FSCDL[3:0]   |           |              |           |  |
|                 |                    | 0106h | MRCONF6   | 0           | CPTM[3:0]    |              |               |              | THTH[1:0] |              | TSTS      |  |
|                 |                    | 0107h | MRCONF7   | WDTEN       | WDTS EL[2]   | WDT[5:0]     |               |              |           |              |           |  |
|                 |                    | 0108h | MRCONF8   | VCLVP EN    | CPEN         | THWEN        | THPEN         | FSPEN        | OVPEN     | OCPEN        | DIAGSEL   |  |
|                 |                    | 0109h | MRCONF9   | RCVTM[1:0]  |              | WDTSEL[1:0]  |               | CPLT         | FSPLT     | OCPLT        | DLTO      |  |
|                 |                    | 010Ah | MRCONF10  | VDHO VPEN   | OOPO EN      | CLDO EN      | FGERACCEN     | RCSM PMD     | RCSM PEN  | OPDTM[1:0]   |           |  |
|                 |                    | 010Bh | MRCONF11  | INIODU TYMD | INITA GMD    | CLREFE N_ROT | CLREFE N_STOP | ATSYN COFF   | 0         | STSYN EN     | SPIIN SEL |  |
|                 |                    | 010Ch | MRCONF12  | FGERD ECEN  | FGERDEC[2:0] |              |               | FGERACC[3:0] |           |              |           |  |
|                 |                    | 010Dh | MRCONF13  | 0           | DWNSET       | PDTSEL[1:0]  |               | FSPDTM[1:0]  |           | OVPMASK[1:0] |           |  |
|                 |                    | 010Eh | MRCONF14  | RCSM[7:0]   |              |              |               |              |           |              |           |  |
| 010Fh           | MRCONF15           | 0     | 0         | 0           | SSCG EN      | SSCGCN[1:0]  |               | Internal use |           |              |           |  |

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## MRCONF0 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6]  | D[5] | D[4] | D[3]   | D[2] | D[1]  | D[0]     |
|-------|-----------|------|-------|------|------|--------|------|-------|----------|
| 0100h | MRCONF0   | FRMD | FRREN | SCEN | PWMF | REGSEL | VCEN | SPCFG | PWMINSEL |

### FRMD: Forward / Reverse MoDe

FRMD=0: Forward motor rotation  
FRMD=1: Reverse motor rotation

### FRREN: FRee Running ENable

FRREN=0: Motor will start with a BEMF detection.  
FRREN=1: Motor will start open-loop with startup parameters.

### SCEN: external Speed Control ENable

SCEN=0: Speed feedback loop is active. RPM is selected from input duty cycle.  
SCEN=1: Power stage duty cycle is translated from input duty cycle.

### PWMF: PWM input Frequency selection

PWMF=0: Valid PWM input frequency range from 5.3 Hz to 1 kHz.  
PWMF=1: Valid PWM input frequency range from 5.3 Hz to 18.5 kHz.

### REGSEL: Vcc REGulator SElection

REGSEL=0: VCC output set to 3.3 V.  
REGSEL=1: VCC output set to 5 V.

### VCEN: Vcc regulator ENable

VCEN=0: VCC is off.  
VCEN=1: VCC is active.

### SPCFG: Speed feedback loop calculation Period ConFiGuration

SPCFG=0: Calculate per 360 electrical degrees.  
SPCFG=1: Calculate per 120 electrical degrees. (Using speed just before 360 electrical degrees)

### PWMINSEL: PWM INput pin SElection

PWMINSEL=0: HVPIN is used for PWM input. (High voltage)  
PWMINSEL=1: LVPIN is used for PWM input. (Low voltage)

## MRCONF1 (Default: 00h)

| ADDR  | Data Name | D[7]       | D[6] | D[5] | D[4]       | D[3] | D[2] | D[1] | D[0]  |
|-------|-----------|------------|------|------|------------|------|------|------|-------|
| 0101h | MRCONF1   | FLSEL[2:0] |      |      | ZPSEL[2:0] |      |      | PDTC | PWMON |

### FLSEL[2:0]: Full Load fallback level SElection (PWM input 100% duty mode)

FLSEL[2:0]=0h,7h: Motor is turned off  
FLSEL[2:0]=1h: Motor duty cycle 25%  
FLSEL[2:0]=2h: Motor duty cycle 50%  
FLSEL[2:0]=3h: Motor duty cycle 75%  
FLSEL[2:0]=4h: Motor duty cycle 100%  
FLSEL[2:0]=5h: Motor duty cycle is decided by TAG\_L setting  
FLSEL[2:0]=6h: Motor duty cycle is decided by TAG\_H setting

### ZPSEL[2:0]: Zero Power fallback level SElection (PWM input 0% duty mode)

ZPSEL[2:0]=0h,7h: Motor is turned off  
ZPSEL[2:0]=1h: Motor duty cycle 25%  
ZPSEL[2:0]=2h: Motor duty cycle 50%

ZPSEL[2:0]=3h: Motor duty cycle 75%  
ZPSEL[2:0]=4h: Motor duty cycle 100%  
ZPSEL[2:0]=5h: Motor duty cycle is decided by TAG\_L setting  
ZPSEL[2:0]=6h: Motor duty cycle is decided by TAG\_H setting

### PDTC: Pending Detection of a Transition Control

PDTC=0: Fast startup operation is disabled.  
PDTC=1: Fast startup operation is enabled.  
If PDTC is set, the motor is driven with the duty cycle programmed into PDTSEL, as soon as EN is high.  
This feature is bridging the initial 200 ms of operation until a valid PWM duty cycle can be decoded.

### PWMON: PWM ON polarity

PWMON=0: PWM input signal is active high.  
PWMON=1: PWM input signal is active low.



**MRCONF2 (Default: 00h)**

| ADDR  | Data Name | D[7]     | D[6]      | D[5] | D[4]      | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|----------|-----------|------|-----------|------|------|------|------|
| 0102h | MRCONF2   | FGSTBLMD | FGOF[1:0] |      | FDTI[4:0] |      |      |      |      |

*FGSTBLMD: Frequency Generator STaBLe MoDe*

FGSTBLMD=0: Disable

FGSTBLMD=1: Enable

It affects only for the 6-window mode (WINDSEL = 0). To determine the lead angle timing, the previous BEMF zero-cross interval is sampled. When this function is disabled, the sampling is done every 60 degree electrical cycle. When this function is enabled, the sampling is done every 120 degree, and the previous 60 degree interval will be estimated as 1/2 of 120 degree interval. It ignores the BEMF asymmetric characteristics (or waveform) between rise and fall.

*FGOF[1:0]: Frequency Generator Output Frequency (= rotation speed)*

FGOF[1:0]=0h: One transition per BEMF detection (FG3)

FGOF[1:0]=1h: One transition per every two BEMF detection (FG3/2)

FGOF[1:0]=2h: One pulse per electrical revolution (FG1)

FGOF[1:0]=3h: One pulse per every two electrical revolutions (FG1/2)

The FG3 signal is a representation of a successfully detected BEMF transition which occurs three times during every electrical revolution.

*FDTI[4:0]: Fet Dead Time*

FDTI[4:0]=00h: 6.4 μs

FDTI[4:0]=x: (6.4 - x \* 0.2) μs

FDTI[4:0]=1Fh: 0.2 μs

During phase switching between supply and GND it is possible for both low- and high-side drivers to be temporarily on at the same time causing large current spikes. Register FDTI defines a dead time during which both drivers will be kept off during these transitions.

**MRCONF3 (Default: 00h)**

| ADDR  | Data Name | D[7]        | D[6] | D[5] | D[4] | D[3]        | D[2] | D[1] | D[0] |
|-------|-----------|-------------|------|------|------|-------------|------|------|------|
| 0103h | MRCONF3   | CLMASK[3:0] |      |      |      | OCMASK[3:0] |      |      |      |

*CLMASK[3:0]: Current Limit MASKing time*

CLMASK[3:0]=0h: Mask Time 0.2 μs

CLMASK[1:0]=x: Mask Time 0.2 \* (1 + x) μs

CLMASK[3:0]=Fh: Mask Time 3.2 μs

In order to prevent noise and glitches causing from false current limiting, this mask time can be programmed.

*OCMASK[3:0]: OverCurrent MASKing time*

OCMASK[3:0]=0h: Overcurrent mask time 0.2 μs

OCMASK[3:0]=x:

Overcurrent mask time 0.2 \* (1 + x) μs

OCMASK[3:0]=Fh: Overcurrent mask time 3.2 μs

The time to detect overcurrent can be programmed with OCMASK.

**MRCONF4 (Default: 00h)**

| ADDR  | Data Name | D[7]        | D[6] | D[5] | D[4] | D[3]        | D[2] | D[1] | D[0] |
|-------|-----------|-------------|------|------|------|-------------|------|------|------|
| 0104h | MRCONF4   | SROFFT[3:0] |      |      |      | CRMASK[3:0] |      |      |      |

*SROFFT[3:0]: Synchronous Rectification OFF Time*

A reverse current detection at -25% of CLSEL can disable for a programmable time the synchronous rectification, e.g. to avoid that the power supply is lifted when the motor current is reduced quickly.

SROFFT[3:0]=0h: Synchronous rectification off time 4 FG

SROFFT[3:0]=x:

Synchronous rectification off time 4 \* (1 + x) FG

SROFFT[3:0]=Fh: Synchronous rectification off time 64 FG

*CRMASK[3:0]: Current Reversed MASKing time*

This is the masking time of the reverse current detection before triggering SROFFT.

CRMASK[3:0]=0h: Mask time 3.2 μs

CRMASK[3:0]=x: Mask time 0.2 \* (16 - x) μs

CRMASK[3:0]=Fh: Mask time 0.2 μs

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### MRCONF5 (Default: 00h)

| ADDR  | Data Name | D[7]   | D[6]    | D[5]       | D[4] | D[3] | D[2]       | D[1] | D[0] |
|-------|-----------|--------|---------|------------|------|------|------------|------|------|
| 0105h | MRCONF5   | SYNCEN | PPDOSEL | FSCDT[1:0] |      |      | FSCDL[3:0] |      |      |

*SYNCEN: SYNchronous rectification ENable (active low)*

SYNCEN=0: Synchronous rectification is ON.  
(Synchronous rectification mode)

SYNCEN=1: Synchronous rectification is OFF.  
(Asynchronous rectification mode)

SYNCEN defines synchronous rectification mode for the output stage. In synchronous rectification mode, the high and low-side switches are always switched in complementary mode. In asynchronous rectification mode, both complementary switches may be off and the motor current is circling through the body diodes.

*PPDOSEL: Pwm Problem Diagnostics Output SElection*

PPDOSEL=0: Abnormal PWM input detected result is reflected to DIAG pin.

PPDOSEL=1: Abnormal PWM input detected result is not reflected to DIAG pin.

*FSCDT[1:0]: Fet Short-Circuit Detection Time*

FSCDT[1:0]=0h: Detection time 3.2  $\mu$ s

FSCDT[1:0]=1h: Detection time 6.4  $\mu$ s

FSCDT[1:0]=2h: Detection time 9.6  $\mu$ s

FSCDT[1:0]=3h: Detection time 12.8  $\mu$ s

By monitoring FET V<sub>ds</sub>, the time from FET's ON signal output until detecting shorted status can be set with FSCDT.

*FSCDL[3:0]: Fet Short-Circuit Detection Level*

FSCDL[3:0]=0h: Detection voltage 0.1 V

FSCDL[3:0]=x: Detection voltage 0.1 \* (1 + x) V

FSCDL[3:0]=Fh: Detection voltage 1.6 V

### MRCONF6 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6]      | D[5] | D[4] | D[3] | D[2]      | D[1] | D[0] |
|-------|-----------|------|-----------|------|------|------|-----------|------|------|
| 0106h | MRCONF6   | 0    | CPTM[3:0] |      |      |      | THTH[1:0] |      | TSTS |

*CPTM[3:0]: Constrained movement Protection TiMe*

CPTM[3:0]=0h: Detection time 0.4 s / Restart time 3.2 s

CPTM[3:0]=x: Detection time 0.4 \* (1 + x) s / Restart time 0.4 \* 8 \* (1 + x) s

CPTM[3:0]=Fh: Detection time 6.4 s / Restart time 51.2 s

A locked rotor protection circuit is embedded in order to protect IC and Motor during locked rotor conditions. A locked rotor is detected by counting the time the IC is in Startup mode (without BEMF detection). If no BEMF is detected for the time programmed into CPTM register, the motor is turned off and a locked rotor is flagged.

In auto-recovery mode, the motor will remain off for eight times the Open-Loop Startup Timeout before another startup is attempted.

*THTH[1:0]: THreshold of THermometer*

THTH[1:0]=0h: Detection voltage 0.35 V

THTH[1:0]=1h: Detection voltage 0.30 V

THTH[1:0]=2h: Detection voltage 0.25 V

THTH[1:0]=3h: Detection voltage 0.20 V

LV8961H has an embedded comparator to monitor the external power FET temperature via an external thermistor. If the voltage at TH exceeds the threshold shown in the table, the power stage is shut off and a THPO error is triggered.

*TSTS: Thermal Shutdown Temperature Setting*

TSTS=0: Overtemperature warning occurs at 125°C (typ), shutdown at 150°C (typ).

TSTS=1: Overtemperature warning occurs at 150°C (typ), shutdown at 175°C (typ).

The LV8961H monitors its own junction temperature to protect against overtemperature damage. Two different warning- and shutoff levels can be selected.

**MRCONF7 (Default: 00h)**

| ADDR  | Data Name | D[7]  | D[6]      | D[5]     | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|-------|-----------|----------|------|------|------|------|------|
| 0107h | MRCONF7   | WDTEN | WDTSEL[2] | WDT[5:0] |      |      |      |      |      |

*WDTEN: WatchDog Timeout Enable*

WDTEN=0: Watchdog is disabled.

WDTEN=1: Watchdog is active.

This bit can enable or disable the watchdog.

*WDTSEL[2:0]: WatchDog Target duty SELECTION*

*1bit [2] of WDTSEL[2:0] register*

WDTSEL[2:0]=0h,7h: Motor duty cycle 0%

WDTSEL[2:0]=1h: Motor duty cycle 25%

WDTSEL[2:0]=2h: Motor duty cycle 50%

WDTSEL[2:0]=3h: Motor duty cycle 75%

WDTSEL[2:0]=4h: Motor duty cycle 100%

WDTSEL[2:0]=5h: Motor duty cycle is indicated by TAG\_L

WDTSEL[2:0]=6h: Motor duty cycle is indicated by TAG\_H

If this register is set, a watchdog timeout causes Halt mode (0% drive) or Drive mode. When Drive mode is selected, the motor duty cycle is defined by this register and TAG\_L, TAG\_H registers.

*WDT[5:0]: WatchDog Timeout duration setting*

WDT[5:0]=00h: Detection time 1.6 ms

WDT[5:0]=x: Detection time 1.6 \* (1 + x) ms

WDT[5:0]=3Fh: Detection time 102.4 ms

Writing 00h to register MRRST(Address = 0300h) resets the watchdog timer. When the watchdog timer reaches its end detection time, a watchdog error is issued.

**MRCONF8 (Default: 00h)**

| ADDR  | Data Name | D[7]    | D[6] | D[5]  | D[4]  | D[3]  | D[2]  | D[1]  | D[0]    |
|-------|-----------|---------|------|-------|-------|-------|-------|-------|---------|
| 0108h | MRCONF8   | VCLVPEN | CPEN | THWEN | THPEN | FSPEN | OVPEN | OCPEN | DIAGSEL |

*xEN: Error and warning mask*

VCLVPEN: VCc Low Voltage Protection ENable.

CPEN: Constrained movement Protection ENable.

THWEN: THERmal Warning ENable.

THPEN: THERmal Protection ENable.

FSPEN: Fet Short Protection ENable

OVPEN: OverVoltage Protection ENable.

OCPEN: OverCurrent Protection ENable.

The higher seven bits in this register allows enabling and disabling of various errors and warnings. Setting xEN=1 masks the error, setting xEN=0 activates the error.

*DIAGSEL: DIAG polarity SELECTION*

DIAGSEL=0: The DIAG pin is active low.

DIAGSEL=1: The DIAG pin is active high.

This bit selects the polarity of the DIAG signal.

The DIAG pin is OPEN drain.

**MRCONF9 (Default: 00h)**

| ADDR  | Data Name | D[7]       | D[6] | D[5]        | D[4] | D[3] | D[2]  | D[1]  | D[0] |
|-------|-----------|------------|------|-------------|------|------|-------|-------|------|
| 0109h | MRCONF9   | RCVTM[1:0] |      | WDTSEL[1:0] |      | CPLT | FSPLT | OCPLT | DLTO |

*RCVTM[1:0]: ReCoVery TiMe setting*

RCVTM[1:0]=0h: Recovery time 0 s

RCVTM[1:0]=1h: Recovery time 5 s

RCVTM[1:0]=2h: Recovery time 10 s

RCVTM[1:0]=3h: Recovery time 20 s

IC will restart (after an abnormal rotational speed change is detected) when this recovery time elapses.

*WDTSEL[1:0]: WatchDog Target duty SELECTION*

*2bit [1:0] of WDTSEL[2:0] register*

See MRCONF7 register.

*xPLT: Protection LaTch selection*

CPLT=0: Auto recover after constrained movement detection.

CPLT=1: Latch the IC off after constrained movement detection.

FSPLT=0: Auto recover after FET short detection.

FSPLT=1: Latch the IC off after FET short detection.

OCPLT=0: Auto recover after overcurrent detection.

OCPLT=1: Latch the IC off after overcurrent detection.

Motor constraint, FET short, and overcurrent can cause intolerable large-current flow in the application. To prevent repeated current flow during retry attempts, it is possible to latch these errors.

*DLTO: Diagnostics output Latched Transitions Only*

DLTO=0: Trigger DIAG for any non-masked error or warning.

DLTO=1: Trigger DIAG only for latched errors as defined by above xPLTs.

**MRCONF10 (Default: 00h)**

| ADDR  | Data Name | D[7]     | D[6]   | D[5]   | D[4]      | D[3]    | D[2]    | D[1]       | D[0] |
|-------|-----------|----------|--------|--------|-----------|---------|---------|------------|------|
| 010Ah | MRCONF10  | VDHOVPEN | OOPOEN | CLDOEN | FGERACCEN | RCSMPMD | RCSMPEN | OPDTM[1:0] |      |

*xEN: Error and warning mask*

VDHOVPEN: VDH OverVoltage Protection ENable.

OOPOEN: Open cOnnector Protection Output ENable.

CLDOEN: Current Limit Detection Output ENable.

The higher three bits in this register allow enabling and disabling of various errors and warnings. Setting xEN=1 masks the error, setting xEN=0 activates the error.

*FGERACCEN: Frequeny Generator ERrordetection during ACCeleration ENabled*

FGERACCEN=0: FG error detection at acceleration is disabled.

FGERACCEN=1: FG error detection at acceleration is enabled

*RCSMPMD: Register CheckSuM error then Power Motor Down*

RCSMPMD=0: Keep motor running after checksum error detection.

RCSMPMD=1: Power down motor after checksum error detection.

Register checksum error information is always output to DIAG when RCSMEN register is set, and it is independent of RCSMPMD setting.

*RCSMPEN: Register CheckSuM Periodical at running motor ENable*

RCSMPEN=0: Register checksum calculation is done at following timing.

- Device startup
- Writing OTP
- OTP download by writing MRODL=00h

RCSMPEN=1: Register checksum calculation is done at following timing.

- Device startup
- Writing OTP
- OTP download by writing MRODL=00h
- 1 ms periodically at motor running

*OPDTM[1:0]: OPen connector Detection TiMe selection*

OPDTM[1:0]=0h: Detection time 160 μs

OPDTM[1:0]=1h: Detection time 320 μs

OPDTM[1:0]=2h: Detection time 640 μs

OPDTM[1:0]=3h: Detection time 1280 μs

When the motor cannot be started for a certain period of time and it is in the startup mode, this IC flows current to each coil, then determines IC is in a constraint state when current flows, or an open state when no current flows. The detection time for the current to flow can be selected by OPDTM.

**MRCONF11 (Default: 00h)**

| ADDR  | Data Name | D[7]        | D[6]     | D[5]         | D[4]          | D[3]      | D[2] | D[1]     | D[0]     |
|-------|-----------|-------------|----------|--------------|---------------|-----------|------|----------|----------|
| 010Bh | MRCONF11  | INIODUT YMD | INITAGMD | CLREFEN _ROT | CLREFEN _STOP | ATSYNCOFF | 0    | STSYNCEN | SPIINSEL |

*INIODUTYMD: INItial Output DUTY cycle MoDe (soft start function)*

INIODUTYMD=0: Input PWM duty

INIODUTYMD=1: Ramp up from 0%

*INITAGMD: INItial max. TArGet output duty cycle MoDe*

INITAGMD=0: Input PWM duty

INITAGMD=1: PDTSEL setting

*CLREFEN\_ROT: Current Limit REFErence ENable (free ROTating status)*

CLREFEN\_ROT=0: Disable current ramp (soft start) in free-run status.

CLREFEN\_ROT=1: Enable current ramp (soft start) in free-run status.

*CLREFEN\_STOP: Current Limit REFErence ENable (STOP status)*

CLREFEN\_STOP=0: Disable disable current ramp (soft start) in stop status.

CLREFEN\_STOP=1: Enable current ramp (soft start) in stop status.

*ATSYNCOFF: AuTomatic SYNChronous rectification OFF (active low)*

This bit activates the automatic disabling of synchronous rectification.

ATSYNCOFF=0: Automatic synchronous rectification off function is enabled.

ATSYNCOFF=1: Automatic synchronous rectification off function is disabled.

*STSYNCEN: SofiStArt SYNChronous rectification ENable (active low)*

STSYNCEN=0: Synchronous rectification at soft start depends on SYNCEN.

STSYNCEN=1: Synchronous rectification at soft start is forced off.

*SPIINSEL: duty cycle through SPI INput SELECTION*

SPIINSEL=0: Input duty from pin. (HVPIN/LVPIN)

SPIINSEL=1: Input duty from PWMDTIN register (concatenation of MRCTL1[1:0] and MRCTLO[7:0]).

**MRCONF12 (Default: 00h)**

| ADDR  | Data Name | D[7]      | D[6]         | D[5] | D[4] | D[3]         | D[2] | D[1] | D[0] |
|-------|-----------|-----------|--------------|------|------|--------------|------|------|------|
| 010Ch | MRCONF12  | FGERDECEN | FGERDEC[2:0] |      |      | FGERACC[3:0] |      |      |      |

*FGERDECEN: Frequency Generator Error detection during DEceleration ENable*

FGERDECEN=0: FG error detection at deceleration is disabled.

FGERDECEN=1: FG error detection at deceleration is enabled

*FGERDEC[2:0]: Frequency Generator Error detection during DEceleration setting*

FGERDEC[2:0]=0h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 1.25.

FGERDEC[2:0]=1h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 1.5.

FGERDEC[2:0]=2h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 1.75.

FGERDEC[2:0]=3h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 2.

FGERDEC[2:0]=4h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 3.

FGERDEC[2:0]=5h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 4.

FGERDEC[2:0]=6h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 6.

FGERDEC[2:0]=7h: Limit of zero-cross detection time is (previous 60 electrical degrees period) \* 8.

*FGERACC[3:0]: Frequency Generator Error detection during ACceleration setting*

FGERACC[3:0]=0h: 1 time detecting zero-cross of BEMF when the moment the Mask signal is opened.

FGERACC[3:0]=x: (1 + x) consecutive time detecting zero-cross of BEMF when the moment the Mask signal is opened.

FGERACC[3:0]=Fh: 16 consecutive time detecting zero-cross of BEMF when the moment the Mask signal is opened.

**MRCONF13 (Default: 00h)**

| ADDR  | Data Name | D[7] | D[6]   | D[5]        | D[4] | D[3]        | D[2] | D[1]         | D[0] |
|-------|-----------|------|--------|-------------|------|-------------|------|--------------|------|
| 010Dh | MRCONF13  | 0    | DWNSET | PDTSEL[1:0] |      | FSPDTM[1:0] |      | OVPMASK[1:0] |      |

*DWNSET: slowDoWN SETting*

DWNSET=0: Normal mode

DWNSET=1: Synchronous rectification OFF mode

During speed control mode, motor deceleration can lead to energy recuperation and temporary voltage spikes. DWNSET allows for various degrees of energy recuperation:

- Normal Mode

Results in a tightest control and maximum energy recuperation. The application circuit has to be able to absorb the energy generated.

- Synchronous rectification OFF Mode

The motor is essentially not driven until it has reached the target speed. This does not feed any energy back into the supply, but may take a long time if motor inertia is high and losses are low.

*PDTSEL[1:0]: Pending Detection of a Transition SElection*

PDTSEL[1:0]=0h: Motor duty cycle 25%

PDTSEL[1:0]=1h: Motor duty cycle 50%

PDTSEL[1:0]=2h: Motor duty cycle 75%

PDTSEL[1:0]=3h: Motor duty cycle 100%

If PDTC is set, the motor is driven with the duty cycle programmed into PDTSEL, as soon as EN is high.

This feature is bridging the initial 200 ms of operation until a valid PWM duty cycle can be decoded.

*FSPDTM[1:0]: Fet Short Protection Debounce Time setting*

FSPDTM[1:0]=0h: Debounce time 1.6 μs

FSPDTM[1:0]=1h: Debounce time 3.2 μs

FSPDTM[1:0]=2h: Debounce time 4.8 μs

FSPDTM[1:0]=3h: Debounce time 6.4 μs

*OVPMASK[1:0]: OverVoltage Protection MASKing time*

The time to detect overvoltage condition on VS and VDH can be set by OVPMASK.

OVPMASK[1:0]=0h: Detection time 0.8 μs

OVPMASK[1:0]=1h: Detection time 1.6 μs

OVPMASK[1:0]=2h: Detection time 3.2 μs

OVPMASK[1:0]=3h: Detection time 6.4 μs

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## MRCONF14 (Default: 00h)

| ADDR  | Data Name | D[7]       | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------------|------|------|------|------|------|------|------|
| 010Eh | MRCONF14  | RCSM [7:0] |      |      |      |      |      |      |      |

*RCSM[7:0]: Register CheckSum*

This register is the data downloaded from OTP memory ORCONF34. Basically, users don't need to care of it.

## MRCONF15 (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4]   | D[3]        | D[2] | D[1]         | D[0] |
|-------|-----------|------|------|------|--------|-------------|------|--------------|------|
| 010Fh | MRCONF15  | 0    | 0    | 0    | SSCGEN | SSCGCN[1:0] |      | Internal use |      |

*SSCGEN: Spread Spectrum Charge pump Generation Enable*

SSCGEN=0: Spread spectrum is OFF.

SSCGEN=1: Spread spectrum is ON.

The Charge pump may have radiation noise issues due to switching at 52.1 kHz(typ). By activating SSCG it is possible to disperse frequency components of the charge pump switching frequency.

SSCGCN[1:0]=0h: Change CPCLK frequency every 1 clock.

SSCGCN[1:0]=1h: Change CPCLK frequency every 2 clocks.

SSCGCN[1:0]=2h: Change CPCLK frequency every 4 clocks.

SSCGCN[1:0]=3h: Change CPCLK frequency every 8 clocks.

*SSCGCN[1:0]: Spread Spectrum Charge pump Generation Clock Number*

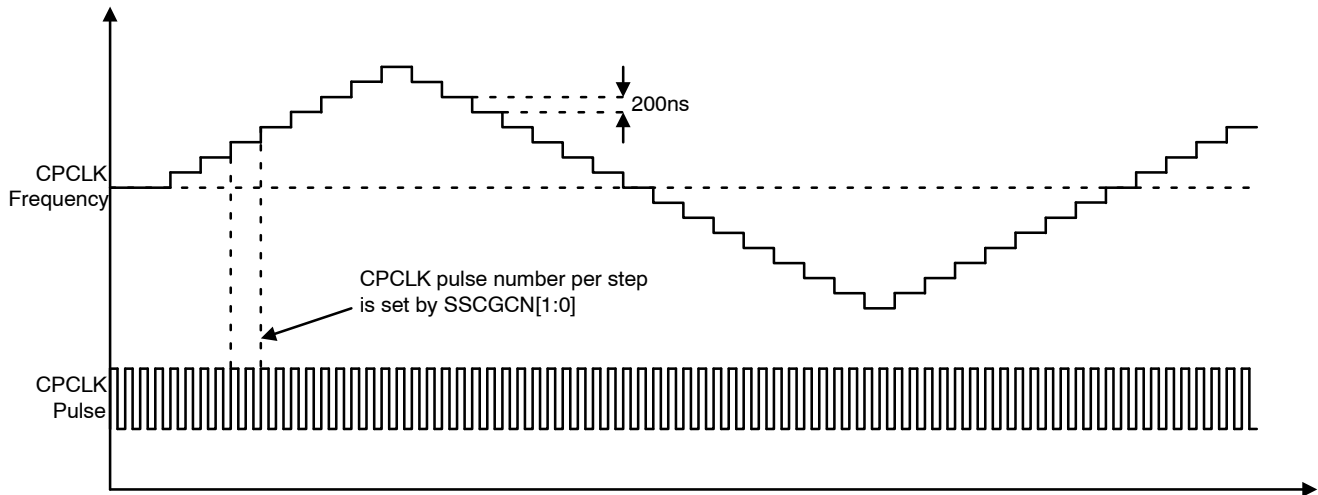


Figure 21.

SYSTEM DIAGNOSTICS AND TEST REGISTER OVERVIEW

| Write Enable | Limitation by OBSY | ADDR  | Data Name | D[7]  | D[6]   | D[5]    | D[4]     | D[3]         | D[2]    | D[1]         | D[0]     |  |
|--------------|--------------------|-------|-----------|---|--------|---------|----------|--------------|---------|--------------|----------|--|
| Read-Only    | Read-Only          | 0200h | MRACS     | 0   | 0      | 0       | 0        | 0            | RCSM EN | OSAE NB      | MSAE NB  |  |
|              |                    | 0201h | MRDIAG0   | CPO   | THPO   | FSPO    | VGLLV PO | CHPLV PO     | VSOV PO | VSLVPO       | OCPO     |  |
|              |                    | 0202h | MRDIAG1   | PWMPO   | VCLVPO | RCSM PO | OOPO     | CLDO         | WDTPO   | THSPO        | THWPO    |  |
|              |                    | 0203h | MRDIAG2   | 0   | 0      | OTPAZ   | REGAZ    | FGER PO      | SPCO    | STUPO        | VDHO VPO |  |
|              |                    | 0204h | MRDIAG3   | 0   | 0      | 0       | 0        | 0            | 0       | CHPO VPO     | CRDT O   |  |
|              |                    | 0205h | MRSTAT0   | STATUS[7:0]   |        |         |          |              |         |              |          |  |
|              |                    | 0206h | MRSTAT1   | STATUS[15:8]  |        |         |          |              |         |              |          |  |
|              |                    | 0207h | MRSTAT2   | STATUS[23:16]   |        |         |          |              |         |              |          |  |
| Always OK    | Always OK          | 0300h | MRRST     | Write 00h: Reset WDT / Write 55h Reset Register Checksum Error / Write FFh: Reset latch off |        |         |          |              |         |              |          |  |
|              |                    | 0301h | MRCTL0    | PWMDTIN[7:0]  |        |         |          |              |         |              |          |  |
|              |                    | 0302h | MRCTL1    | BRK   | 0      | 0       | 0        | 0            | 0       | PWMDTIN[9:8] |          |  |
|              |                    | 0303h | MRCTL2    | Internal use  |        |         |          |              |         |              |          |  |
|              |                    | 0304h | MRCTL3    | Internal use  |        |         |          |              |         |              |          |  |
|              |                    | 0305h | MRCTL4    | 0   | 0      | 0       | 0        | 0            | 0       | Internal use |          |  |
|              |                    | 0306h | MRCTL5    | 0   | 0      | 0       | 0        | STATSEL[3:0] |         |              |          |  |
|              |                    | 0307h | MRCTL6    | BAREG[7:0]  |        |         |          |              |         |              |          |  |
|              |                    | 0308h | MRCTL7    | BAREG[15:8]   |        |         |          |              |         |              |          |  |
| EN=L         | OBSY=L             | 0400h | MRODL     | Write 00h: Execute OTP data download, Write FFh: Execute register checksum calculation      |        |         |          |              |         |              |          |  |
|              |                    | 0401h | MRORB     | 0   | 0      | 0       | 0        | 0            | 0       | ORBEN        | ORBLV    |  |

MRACKS

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2]   | D[1]   | D[0]   |
|-------|-----------|------|------|------|------|------|--------|--------|--------|
| 0200h | MRACS     | 0    | 0    | 0    | 0    | 0    | RCSMEN | OSAENB | MSAENB |

This data, which is a read-only register, is downloaded from OTP memory ORCONF33.

<BR>

*RCSMEN: Register CheckSum ENable*

RCSMEN=0: Register checksum diagnostic function is disabled.

RCSMEN=1: Register checksum diagnostic function is enabled

*OSAENB: Otp registers Spi Access ENable Bar (Disable)*

OSAENB=0: Write access permitted.

OSAENB=1: Write access denied.

OSAENB controls write access to the OTP registers.

*MSAENB: Main registers Spi Access ENable Bar (Disable)*

MSAENB=0: Write access permitted.

MSAENB=1: Write access denied.

MSAENB controls write access to the main registers.

MRDIAG0

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4]    | D[3]    | D[2]   | D[1]   | D[0] |
|-------|-----------|------|------|------|---------|---------|--------|--------|------|
| 0201h | MRDIAG0   | CPO  | THPO | FSPO | VGLLVPO | CHPLVPO | VSOVPO | VSLVPO | OCPO |

*CPO: Constrained movement Protection Output*

CPO=0: Normal

CPO=1: Detect locked rotor error

No BEMF was detected during the entire open-loop startup time as programmed in CPTM. Either the rotor is blocked, or startup parameters are not correct. The drivers are disabled.

**THPO: fet Thermal Protection Output**

THPO=0: Normal  
 THPO=1: Detect FET thermal error

**FSPO: Fet Short Protection Output**

FSPO=0: Normal  
 FSPO=1: Detect FET short error

The drain–source voltage threshold across one of the external power FETs has been exceeded during operation. The threshold voltage is programmed in register FSCDL. Errors are suppressed for a blanking time as programmed in register FSCDT, both in register MRCONF5.

For the high–side FETs this voltage is measured between pin VS and the corresponding phase connection UOUT, VOUT, WOUT. For the low–side FETs it is measured between the phase connection and the pins SUL, SVL and SWL. Make sure to minimize potential voltage drops in the sense paths.

**VGLLVPO: VGL Low Voltage Protection Output**

VGLLVPO=0: Normal  
 VGLLVPO=1: Detect VGL undervoltage error

The voltage at VGL has dropped below 5.5 V (max). The drivers are disabled to protect against low gate enhancement.

**CHPLVPO: CHarge Pump Low Voltage Protection Output**

CHPLVPO=0: Normal  
 CHPLVPO=1: Detect CHP low voltage error

The voltage between VS and VCP has dropped below 5.5 V (max). The drivers are disabled to protect against low gate enhancement.

**VSOVPO: VS OverVoltage Protection Output**

VSOVPO=0: Normal  
 VSOVPO=1: Detect VS over voltage error

The voltage at VS has exceeded 28 V (min). The driver stage and the charge pump are disabled to protect against overvoltage at the charge pump.

**VSLVPO: VS Low Voltage Protection Output**

VSLVPO=0: Normal  
 VSLVPO=1: Detect VS undervoltage error

The voltage at VS has fallen below 5.1 V (max). The driver stage is disabled to protect against internal threshold issues.

**OCPO: OverCurrent Protection Output**

OCPO=0: Normal  
 OCPO=1: Detect overcurrent error

The voltage between current sense pins RFSENS and RF has exceeded overcurrent threshold voltage for longer than the overcurrent limit mask time programmed in register OCMASK in MRCONF3. The driver stage is disabled to protect against damage.

**MRDIAG1**

| ADDR  | Data Name | D[7]  | D[6]   | D[5]   | D[4] | D[3] | D[2]  | D[1]  | D[0]  |
|-------|-----------|-------|--------|--------|------|------|-------|-------|-------|
| 0202h | MRDIAG1   | PWMPO | VCLVPO | RCSMPO | OOPO | CLDO | WDTPO | THSPO | THWPO |

**PWMPO: PWM input abnormal Protection Output**

PWMPO=0: Normal  
 PWMPO=1: Detect PWM input error

The PWM input does not oscillate with the appropriate frequency or is steady high (100%) or low (0%). Depending on the settings FLSEL, ZPSEL in MRCONF1, the driver stage will turn off, or operate at a predefined duty cycle (emergency mode).

**VCLVPO: VCc Low Voltage Protection Output**

VCLVPO=0: Normal  
 VCLVPO=1: Detect VCC undervoltage error

VCC undervoltage error. Depending on the setting of REGSEL in MRCONF0, VCC is either 5 V (typ) or 3.3 V (typ). Undervoltage is flagged if VCC falls below 4.2 V (max) or 2.7 V (max) respectively.

**RCSMPO: Register CheckSum Protection Output**

RCSMPO=0: Normal  
 RCSMPO=1: Detect register checksum error  
 RCSMPO is set when EN=1, RCSMEN=1, RCSMPEN=1 and register checksum error is detected. If RCSMPMD is set, the driver stage will be off.  
 RCSMPO is cleared by writing 55h to register MRRST.

**OOPO: Open cOnnector Protection Output**

OOPO=0: Normal  
 OOPO=1: Detect open connector

**CLDO: Current Limit Detection Output**

CLDO=0: Normal  
 CLDO=1: Detect current limitation

**WDTPO: WatchDog Timer Protection Output**

WDTPO=0: Normal  
 WDTPO=1: Detect WDT error

The watchdog has timed out. This flag will be high if the watchdog was not reset during the time defined by register WDT in MRCONF7. If the watchdog is enabled the driver stage will either be off or run in emergency mode with the settings defined by register WDTSEL in MRCONF7, MRCONF9.

Flag WDTPO is high even if the watchdog is disabled.

**THSPO: Thermal Shutdown Protection Output**

THSPO=0: Normal  
 THSPO=1: Detect thermal shutdown error

The IC temperature is too high and the drivers are shut off. The overtemperature shutoff level is defined by TSTS in MRCONF6 to be either 150°C (min.) or 175°C (min.).



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### THWPO: Thermal Warning Protection Output

THWPO=0: Normal  
 THWPO=1: Detect thermal warning error

The IC temperature has exceeded the warning level. The overtemperature warning level is defined by TSTS in MRCONF6 to be either 125°C (min.) or 150°C (min.).

### MRDIAG2

| ADDR  | Data Name | D[7] | D[6] | D[5]  | D[4]  | D[3]   | D[2] | D[1]  | D[0]    |
|-------|-----------|------|------|-------|-------|--------|------|-------|---------|
| 0203h | MRDIAG2   | 0    | 0    | OTPAZ | REGAZ | FGERPO | SPCO | STUPO | VDHOVPO |

#### OTPAZ: OTP All bits Zero

OTPAZ=0: OTP contains at least one zapped bit.  
 OTPAZ=1: Detect that OTP output is all 0.

#### REGAZ: otp REGISTER All bits Zero

REGAZ=0: Registers which data is downloaded from OTP contains at least 1-bit one.  
 REGAZ=1: Detect that registers which data is downloaded from OTP is all 0.

#### FGERPO: Frequency Generator Error Protection Output

FGERPO=0: The absolute value of the speed error is not detected under FGERACC/FGERRDEC conditions.  
 FGERPO=1: The absolute value of the speed error is detected under FGERACC/FGERRDEC conditions.

#### SPCO: Speed Control error Output

SPCO=0: The absolute value of the speed error is equal to or less than target \* 1/16.  
 SPCO=1: The absolute value of the speed error is greater than target \* 1/16.

#### STUPO: bEMF-less StartUp Period Output

STUPO=0: BEMF has been detected.  
 STUPO=1: No BEMF has been detected, yet. This flag indicates open-loop startup operation.

#### VDHOVPO: VDH OverVoltage Protection Output

VDHOVPO=0: Normal  
 VDHOVPO=1: Detect VDH over voltage error

### MRDIAG3

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1]    | D[0]  |
|-------|-----------|------|------|------|------|------|------|---------|-------|
| 0204h | MRDIAG3   | 0    | 0    | 0    | 0    | 0    | 0    | CHPOVPO | CRDTO |

#### CHPOVPO: CHarge Pump OverVoltage Protection Output

CHPOVPO=0: Normal  
 CHPOVPO=1: Detect charge pump overvoltage error

#### CRDTO: Current Reversed Detection Output

CRDTO=0: Normal  
 CRDTO=1: Detect reverse current

### MRSTAT0 (Default: 00h)

| ADDR  | Data Name | D[7]        | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|-------------|------|------|------|------|------|------|------|
| 0205h | MRSTAT0   | STATUS[7:0] |      |      |      |      |      |      |      |

### MRSTAT1 (Default: 00h)

| ADDR  | Data Name | D[7]         | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|--------------|------|------|------|------|------|------|------|
| 0206h | MRSTAT1   | STATUS[15:8] |      |      |      |      |      |      |      |

### MRSTAT2 (Default: 00h)

| ADDR  | Data Name | D[7]          | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|---------------|------|------|------|------|------|------|------|
| 0207h | MRSTAT2   | STATUS[23:16] |      |      |      |      |      |      |      |

#### STATUS[23:0]: internal STATUS output

Output of STATUS register is selected by STATSEL register in MRCTL5.

2nd and 3rd bytes are hold at temporary register when 1st byte is read to keep simultaneity of status data.

**MRCMSD**

| ADDR  | Data Name | D[7]        | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|-------------|------|------|------|------|------|------|------|
| 0208h | MRCMSD    | RCSMSD[7:0] |      |      |      |      |      |      |      |

*RCSMSD[7:0]: Register CheckSuM Seed*

This register gives checksum code of the hidden registers whose data are downloaded from OTP memory. This register value will be used as a calculation seed of checksum (ORCONF34) for user area of OTP memory, to include both

hidden and user area of the OTP memory. How to activate the register checksum feature as well as the usage of this register RCSMSD is described in the section “[Register Checksum Feature](#)”.

**MRRST**

| ADDR  | Data Name | D[7]  | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|---|------|------|------|------|------|------|------|
| 0300h | MRRST     | Write 00h: Reset WDT / Write 55h Reset register checksum error / Write FFh: Reset latch off |      |      |      |      |      |      |      |

*MRRST[7:0]: Reset for WDT and latch off by protection*

Write MRRST[7:0]=00h: Reset WDT  
Write MRRST[7:0]=55h: Reset driver off by register checksum error

Write MRRST[7:0]=FFh: Reset latch off

Write MRRST[7:0]=others: No operation

**MRCTL0 (Default: 00h)**

| ADDR  | Data Name | D[7]         | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|--------------|------|------|------|------|------|------|------|
| 0301h | MRCTL0    | PWMDTIN[7:0] |      |      |      |      |      |      |      |

**MRCTL1 (Default: 00h)**

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1]         | D[0] |
|-------|-----------|------|------|------|------|------|------|--------------|------|
| 0302h | MRCTL1    | BRK  | 0    | 0    | 0    | 0    | 0    | PWMDTIN[9:8] |      |

*BRK: short BRaKe enable*

BRK=0: Short brake is disabled.  
BRK=1: Short brake is enabled.

Note that when short brake is executed, an overcurrent flows due to the electromotive force generated when the motor rotates.

*PWMDTIN[9:0]: PWM DuTy cycle INput register*

PWMDTIN[9:0]=000h: Duty cycle 0% to 0.098%  
PWMDTIN[9:0]=x: Duty cycle  $(x * 100 / 1024) \%$  to  $((x+1) * 100 / 1024) \%$   
PWMDTIN[9:0]=3FFh: Duty cycle 99.9% to 100%

**MRCTL5 (Default: 00h)**

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3]         | D[2] | D[1] | D[0] |
|-------|-----------|------|------|------|------|--------------|------|------|------|
| 0306h | MRCTL5    | 0    | 0    | 0    | 0    | STATSEL[3:0] |      |      |      |

*STATSEL[3:0]: STATus data SELECTION*

STATSEL selects status data output to STATUS[23:0] (concatenation of MRSTAT2[7:0], MRSTAT1[7:0] and MRSTAT0[7:0]).

STATUS[23:8] are latched when STATUS[7:0] is read.

If STATSEL is changed before reading STATUS[23:8], they hold value which is indicated by previous STATSEL until STATUS[7:0] will be read.

If STATUS[23:8] is read soon after reset, they returns 0000h.

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### STATUS Register Description

Users can know various operation status, such as rotation period/frequency, input duty cycle, PWM output period, lead angle control etc. by reading out the register STATUS[23:0] which is divided into three bytes and stored in the address 0205h to 0207h. The register STATSEL[3:0] stored in the address 0306h determines which status

parameter is allocated to the STATUS register. When read access to the address 0205h (first byte of STATUS [23:0]) was initiated, the register data in the following address 0206h and 0207h will not change during the sequential read access to these addresses so that the simultaneity of three bytes which form STATSEL[23:0] is secured.

### STATUS REGISTER DESCRIPTION

| ADDR  | Data Name | D[7]          | D[6] | D[5] | D[4] | D[3]         | D[2] | D[1] | D[0] |
|-------|-----------|---------------|------|------|------|--------------|------|------|------|
| 0205h | MRSTAT0   | STATUS[7:0]   |      |      |      |              |      |      |      |
| 0206h | MRSTAT1   | STATUS[15:8]  |      |      |      |              |      |      |      |
| 0207h | MRSTAT2   | STATUS[23:16] |      |      |      |              |      |      |      |
| 0306h | MRCTL5    | 0             | 0    | 0    | 0    | STATSEL[3:0] |      |      |      |

### STATUS Register Map

All data which can be read from STATUS register are assigned as following table.

### STATUS REGISTER DESCRIPTION

| STATSEL[3:0] |         | D[7]              | D[6]         | D[5]               | D[4]        | D[3]          | D[2]   | D[1]             | D[0]   |
|--------------|---------|-------------------|--------------|--------------------|-------------|---------------|--------|------------------|--------|
| 0h           | MRSTAT0 | PROT_T[7:0]       |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | PROT_T[15:8]      |              |                    |             |               |        |                  |        |
|              | MRSTAT2 | 0                 | 0            | 0                  | 0           | PROT_T[19:16] |        |                  |        |
| 1h           | MRSTAT0 | PROT_F[7:0]       |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | 0                 | PROT_F[14:8] |                    |             |               |        |                  |        |
| 2h           | MRSTAT0 | IDUTY_IDUTY[7:0]  |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | 0                 | 0            | 0                  | 0           | 0             | 0      | IDUTY_IDUTY[9:8] |        |
| 3h           | MRSTAT0 | PWMP CNT_LT[7:0]  |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | PWMP CNT_LT[15:8] |              |                    |             |               |        |                  |        |
|              | MRSTAT2 | 0                 | 0            | PWMP CNT_LT[21:16] |             |               |        |                  |        |
| 4h           | MRSTAT0 | PWMP CNT_LT[7:0]  |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | PWMP CNT_LT[15:8] |              |                    |             |               |        |                  |        |
|              | MRSTAT2 | 0                 | 0            | PWMP CNT_LT[21:16] |             |               |        |                  |        |
| 5h           | MRSTAT0 | TAG1[7:0]         |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | 0                 | TAG1[14:8]   |                    |             |               |        |                  |        |
| 6h           | MRSTAT0 | PIDOLT[7:0]       |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | 0                 | 0            | 0                  | 0           | 0             | 0      | PIDOLT[9:8]      |        |
| 7h           | MRSTAT0 | LACTL_EPOS[7:0]   |              |                    |             |               |        |                  |        |
| 8h           | MRSTAT0 | 0                 | 0            | 0                  | 0           | NO_OPEN       | OPEN_W | OPEN_V           | OPEN_U |
| 9h           | MRSTAT0 | REGCRC_RSLT[7:0]  |              |                    |             |               |        |                  |        |
| Ah           | MRSTAT0 | ODUTYMAX[7:0]     |              |                    |             |               |        |                  |        |
|              | MRSTAT1 | 0                 | 0            | 0                  | 0           | 0             | 0      | ODUTYMAX[9:8]    |        |
| Bh           | MRSTAT0 | 0                 | 0            | 0                  | LANUM0[4:0] |               |        |                  |        |
| Ch           | MRSTAT0 | 0                 | 0            | 0                  | LANUM1[4:0] |               |        |                  |        |

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## STATUS REGISTER DESCRIPTION

| STATSEL[3:0] |         | D[7]        | D[6]       | D[5] | D[4] | D[3] | D[2]           | D[1]   | D[0]  |
|--------------|---------|-------------|------------|------|------|------|----------------|--------|-------|
| Dh           | MRSTAT0 | 0           | 0          | 0    | 0    | 0    | WNDCH<br>NG_EN | BEMFEN | HIZON |
| Eh           | MRSTAT0 | TAG0[7:0]   |            |      |      |      |                |        |       |
|              | MRSTAT1 | OPENLX<br>0 | TAG0[14:8] |      |      |      |                |        |       |

### STATSEL = 0h

| STATUS           | D[7]         | D[6] | D[5] | D[4] | D[3]          | D[2] | D[1] | D[0] |
|------------------|--------------|------|------|------|---------------|------|------|------|
| [7:0]: MRSTAT0   | PROT_T[7:0]  |      |      |      |               |      |      |      |
| [15:8]: MRSTAT1  | PROT_T[15:8] |      |      |      |               |      |      |      |
| [23:16]: MRSTAT2 | 0            | 0    | 0    | 0    | PROT_T[19:16] |      |      |      |

### STATSEL = 1h

| STATUS[23:0]     | D[7]        | D[6]         | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|------------------|-------------|--------------|------|------|------|------|------|------|
| [7:0]: MRSTAT0   | PROT_F[7:0] |              |      |      |      |      |      |      |
| [15:8]: MRSTAT1  | 0           | PROT_F[14:8] |      |      |      |      |      |      |
| [23:16]: MRSTAT2 | 0           | 0            | 0    | 0    | 0    | 0    | 0    | 0    |

*PROT\_T[19:0]: Period of ROTation (Time)*

*PROT\_F[15:0]: Period of ROTation (Frequency)*

These registers offer speed feedback for use in an external speed control loop.

$$\begin{aligned} \text{Rotation Period T (sec)} &= \text{PROT\_T} \times \frac{1}{500 \text{ kHz}} \times 2 = \\ &= \frac{60}{\text{PROT\_F (Hz)}} \end{aligned}$$

Example 1)

PROT\_T = 625 → PROT\_F = 24000 (RPM, upper limit)

Example 2)

PROT\_T = 768432 → PROT\_F = 19 (RPM)

### STATSEL = 2h

| STATUS[23:0]     | D[7]             | D[6] | D[5] | D[4] | D[3] | D[2] | D[1]             | D[0] |
|------------------|------------------|------|------|------|------|------|------------------|------|
| [7:0]: MRSTAT0   | IDUTY_IDUTY[7:0] |      |      |      |      |      |                  |      |
| [15:8]: MRSTAT1  | 0                | 0    | 0    | 0    | 0    | 0    | IDUTY_IDUTY[9:8] |      |
| [23:16]: MRSTAT2 | 0                | 0    | 0    | 0    | 0    | 0    | 0                | 0    |

*IDUTY\_IDUTY[9:0]: Input DUTY cycle*

IDUTY\_IDUTY[9:0] = 000h: Input duty cycle = 1/1024

IDUTY\_IDUTY[9:0] = 3FFh: Input duty cycle = 1024/1024 (100%)

### STATSEL = 3h

| STATUS[23:0]     | D[7]             | D[6] | D[5]              | D[4] | D[3] | D[2] | D[1] | D[0] |
|------------------|------------------|------|-------------------|------|------|------|------|------|
| [7:0]: MRSTAT0   | PWMPCNT_LT[7:0]  |      |                   |      |      |      |      |      |
| [15:8]: MRSTAT1  | PWMPCNT_LT[15:8] |      |                   |      |      |      |      |      |
| [23:16]: MRSTAT2 | 0                | 0    | PWMPCNT_LT[21:16] |      |      |      |      |      |

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### STATSEL = 4h

| STATUS[23:0]     | D[7]             | D[6] | D[5]              | D[4] | D[3] | D[2] | D[1] | D[0] |
|------------------|------------------|------|-------------------|------|------|------|------|------|
| [7:0]: MRSTAT0   | PWMHCNT_LT[7:0]  |      |                   |      |      |      |      |      |
| [15:8]: MRSTAT1  | PWMHCNT_LT[15:8] |      |                   |      |      |      |      |      |
| [23:16]: MRSTAT2 | 0                | 0    | PWMHCNT_LT[21:16] |      |      |      |      |      |

*PWMHCNT\_LT[21:0]: PWM input High CouNT (LaTched)*

*PWMPCNT\_LT[21:0]: PWM input Period CouNT (LaTched)*

$$IDUTY\_IDUTY = \frac{PWMHCNT\_LT}{PWMPCNT\_LT} \times 1024$$

### STATSEL = 5h

| STATUS[23:0]     | D[7]      | D[6]       | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|------------------|-----------|------------|------|------|------|------|------|------|
| [7:0]: MRSTAT0   | TAG1[7:0] |            |      |      |      |      |      |      |
| [15:8]: MRSTAT1  | 0         | TAG1[14:8] |      |      |      |      |      |      |
| [23:16]: MRSTAT2 | 0         | 0          | 0    | 0    | 0    | 0    | 0    | 0    |

*TAG1[14:0]: TARGet speed/output duty cycle 1 (control input)*

TAG1[14:0] = 7FFh: Output duty cycle = MAX (Target speed limit)

TAG1[14:0] = 0000h: Output duty cycle = 0% (Target speed = 0 RPM)

### STATSEL = 6h

| STATUS[23:0]     | D[7]        | D[6] | D[5] | D[4] | D[3] | D[2] | D[1]        | D[0] |
|------------------|-------------|------|------|------|------|------|-------------|------|
| [7:0]: MRSTAT0   | PIDOLT[7:0] |      |      |      |      |      |             |      |
| [15:8]: MRSTAT1  | 0           | 0    | 0    | 0    | 0    | 0    | PIDOLT[9:8] |      |
| [23:16]: MRSTAT2 | 0           | 0    | 0    | 0    | 0    | 0    | 0           | 0    |

*PIDOLT[9:0]: PI calculated Duty cycle Output resuLT*  
 PIDOLT[9:0] = 000h: Output PWM duty cycle = 0%

PIDOLT[9:0] = 3FFh: Output PWM duty cycle = 100%

### STATSEL = 7h

| STATUS[23:0]     | D[7]            | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|------------------|-----------------|------|------|------|------|------|------|------|
| [7:0]: MRSTAT0   | LACTL_EPOS[7:0] |      |      |      |      |      |      |      |
| [15:8]: MRSTAT1  | 0               | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| [23:16]: MRSTAT2 | 0               | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

*LACTL\_EPOS[7:0]: Lead Angle ConTrol Energizing POSition*

*(00h ≤ LACTL\_EPOS[7:0] ≤ BFh)*

LACTL\_EPOS[7:0] = 00h: Energizing position = 0 deg

LACTL\_EPOS[7:0] = x: Energizing position = (x \* 1.875) deg

LACTL\_EPOS[7:0] = BFh: Energizing position = 358.125 deg

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## STATSEL = 8h

| STATUS[23:0]     | D[7] | D[6] | D[5] | D[4] | D[3]    | D[2]   | D[1]   | D[0]   |
|------------------|------|------|------|------|---------|--------|--------|--------|
| [7:0]: MRSTAT0   | 0    | 0    | 0    | 0    | NO_OPEN | OPEN_W | OPEN_V | OPEN_U |
| [15:8]: MRSTAT1  | 0    | 0    | 0    | 0    | 0       | 0      | 0      | 0      |
| [23:16]: MRSTAT2 | 0    | 0    | 0    | 0    | 0       | 0      | 0      | 0      |

*NO\_OPEN: NO OPEN phases detected*

NO\_OPEN = 0: At least one open phase connector

NO\_OPEN = 1: All phase connectors are connected

*OPEN\_V: OPEN V phase (active low)*

OPEN\_V = 0: V phase connector is open

OPEN\_V = 1: V phase connector is connected

*OPEN\_W: OPEN W phase (active low)*

OPEN\_W = 0: W phase connector is open

OPEN\_W = 1: W phase connector is connected

*OPEN\_U: OPEN U phase (active low)*

OPEN\_U = 0: U phase connector is open

OPEN\_U = 1: U phase connector is connected

## STATSEL = 9h

| STATUS[23:0]     | D[7]             | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|------------------|------------------|------|------|------|------|------|------|------|
| [7:0]: MRSTAT0   | REGCRC_RSLT[7:0] |      |      |      |      |      |      |      |
| [15:8]: MRSTAT1  | 0                | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| [23:16]: MRSTAT2 | 0                | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

*REGCRC\_RSLT: REGister CRC ReSuLT*

The remainder of CRC calculation performed on the OTP registers is stored in REGCRC\_RSLT [7:0].

## STATSEL = Ah

| STATUS[23:0]     | D[7]          | D[6] | D[5] | D[4] | D[3] | D[2] | D[1]          | D[0] |
|------------------|---------------|------|------|------|------|------|---------------|------|
| [7:0]: MRSTAT0   | ODUTYMAX[7:0] |      |      |      |      |      |               |      |
| [15:8]: MRSTAT1  | 0             | 0    | 0    | 0    | 0    | 0    | ODUTYMAX[9:8] |      |
| [23:16]: MRSTAT2 | 0             | 0    | 0    | 0    | 0    | 0    | 0             | 0    |

*ODUTYMAX[9:0]: Output DUTY cycle MAXimum*

ODUTYMAX[9:0] = 000h: Duty = 0 %

ODUTYMAX[9:0] = x: Maximum output duty = 0.09766 \* x %

ODUTYMAX[9:0] = 3Fh: Maximum output duty = 99.902 %

ODUTYMAX limits the duty range of U/V/W output.

## STATSEL = Bh

| STATUS[23:0]     | D[7] | D[6] | D[5] | D[4]        | D[3] | D[2] | D[1] | D[0] |
|------------------|------|------|------|-------------|------|------|------|------|
| [7:0]: MRSTAT0   | 0    | 0    | 0    | LANUM0[4:0] |      |      |      |      |
| [15:8]: MRSTAT1  | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 0    |
| [23:16]: MRSTAT2 | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 0    |

*LANUM0[4:0]: Lead Angle Number 0 (output monitor)*

LANUM0[4:0] = 00h: Duty = 0 deg

LANUM0[4:0] = x: Maximum output duty = 1.875 \* x deg

LANUM0[4:0] = 1Fh: Maximum output duty = 58.125 deg

LANUM0 is the actual lead angle based on the output duty cycle.

**STATSEL = Ch**

| STATUS[23:0]     | D[7] | D[6] | D[5] | D[4]        | D[3] | D[2] | D[1] | D[0] |
|------------------|------|------|------|-------------|------|------|------|------|
| [7:0]: MRSTAT0   | 0    | 0    | 0    | LANUM1[4:0] |      |      |      |      |
| [15:8]: MRSTAT1  | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 0    |
| [23:16]: MRSTAT2 | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 0    |

*LANUM1[4:0]: Lead Angle Number 1 (control input)*

LANUM1[4:0] = 00h: Duty = 0 deg

LANUM1[4:0] = x: Maximum output duty = 1.875 \* x deg

LANUM1[4:0] = 1Fh: Maximum output duty = 58.125 deg

LANUM1 is the target lead angle value which characteristics are determined based on the output duty cycle and the setting of LASET\_L, LASET\_H, and LASET\_LIM.

**STATSEL = Dh**

| STATUS[23:0]     | D[7] | D[6] | D[5] | D[4] | D[3] | D[2]       | D[1]   | D[0]  |
|------------------|------|------|------|------|------|------------|--------|-------|
| [7:0]: MRSTAT0   | 0    | 0    | 0    | 0    | 0    | WNDCHNG_EN | BEMFEN | HIZON |
| [15:8]: MRSTAT1  | 0    | 0    | 0    | 0    | 0    | 0          | 0      | 0     |
| [23:16]: MRSTAT2 | 0    | 0    | 0    | 0    | 0    | 0          | 0      | 0     |

*WNDCHNG\_EN: WiNdoW mode CHaNGe ENabled*

WNDCHNG\_EN = 0: Window selection according to WINDSEL is disabled

WNDCHNG\_EN = 1: Window selection according to WINDSEL is enabled

WNDCHNG\_EN is the internal state monitor which indicates whether window number change is enabled or not.

*BEMFEN: BEMF detection ENabled*

BEMFEN = 0: BEMF zero-cross detection is disabled

BEMFEN = 1: BEMF zero-cross detection is enabled

BEMFEN is the internal state monitor which indicates whether BEMF zero-cross detection is enabled or not.

*HIZON: High Z state ON (active)*

HIZON = 0: Not in High Z window

HIZON = 1: In High Z window

HIZON is the internal state monitor which indicates whether now in the High Z state or not.

**STATSEL = Eh**

| STATUS[23:0]     | D[7]      | D[6]       | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|------------------|-----------|------------|------|------|------|------|------|------|
| [7:0]: MRSTAT0   | TAG0[7:0] |            |      |      |      |      |      |      |
| [15:8]: MRSTAT1  | OPENLX0   | TAG0[14:8] |      |      |      |      |      |      |
| [23:16]: MRSTAT2 | 0         | 0          | 0    | 0    | 0    | 0    | 0    | 0    |

*TAG0[7:0]: TARGet speed/output duty cycle 0 (output monitor)*

TAG0[14:0] = 0000h: Output duty = 0% (Target speed = 0 RPM)

TAG0[14:0] = 7FFFh: Output duty = MAX (Target speed limit)

*OPENLX0: OPEN Loop condition for tag0 (active low)*

OPENLX0 = 0: TAG0 is generated under Open-loop condition

OPENLX0 = 1: TAG0 is generated under Closed-loop condition

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### MRCTL6 (Default: 00h)

| ADDR  | Data Name | D[7]       | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------------|------|------|------|------|------|------|------|
| 0307h | MRCTL6    | BAREG[7:0] |      |      |      |      |      |      |      |

### MRCTL7 (Default: 00h)

| ADDR  | Data Name | D[7]        | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|-------------|------|------|------|------|------|------|------|
| 0308h | MRCTL7    | BAREG[15:8] |      |      |      |      |      |      |      |

*BAREG[15:0]: Base Address REGISTER (short format access)*

This register value is used as register address when BASEL[3:0] field of SPI format is set to Fh.

### MRODL

| ADDR  | Data Name | D[7]  | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|---|------|------|------|------|------|------|------|
| 0400h | MRODL     | ODL[7:0] Write 00h: Execute OTP data download, Write FFh: Execute Register checksum calculation |      |      |      |      |      |      |      |

*ODL[7:0]: Otp DownLoad and checksum*

Write ODL[7:0]=others: No operation

Write ODL[7:0]=00h: Execute OTP data download

A write access of 00h to this register initiates a copy operation of OTP data to the main register. This register is blocked if OBSY is high.

Write ODL[7:0]=FFh: Execute register checksum calculation

### MRORB (Default: 00h)

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1]  | D[0]  |
|-------|-----------|------|------|------|------|------|------|-------|-------|
| 0401h | MRORB     | 0    | 0    | 0    | 0    | 0    | 0    | ORBEN | ORBLV |

*ORBEN: Otp Read Bias check ENable*

ORBEN=0: Normal mode

ORBEN=1: OTP bias read mode (Margin read mode)

*ORBLV: Otp Read Bias check LeVel*

ORBLV=0: OTP low bias read mode (low level margin check) at ORBEN=1

ORBLV=1: OTP high bias read mode (high level margin check) at ORBEN=1

This register modifies the OTP readout threshold. After programming the OTP registers should be verified by reading them with the readout thresholds set low and high to detect false zeros and ones

OTP Register

The OTP Registers contain the default values of the system registers. These registers are always readable via SPI in either Standby or Normal modes. During device startup these default values are copied from the OTP bank (SPI addresses 1000h to 1022h) to the main register bank (SPI addresses 0000h to 0401h). The OTP registers should only be programmed once during IC initialization, during normal operation only the main registers are accessed and modified. It is possible to block programming of the OTP section by setting the OSAENB bit in the ORCONF33 Register of the OTP. For detailed information on the content of the OTP, see the corresponding main register descriptions in the previous section.

### ORCONF0 – ORCONF4 (assigned to OTP bank 0)

| ADDR  | Data Name | D[7]        | D[6]      | D[5] | D[4]       | D[3]        | D[2] | D[1]  | D[0]     |  |
|-------|-----------|-------------|-----------|------|------------|-------------|------|-------|----------|--|
| 1000h | ORCONF0   | FRMD        | FRREN     | SCEN | PWMF       | REGSEL      | VCEN | SPCFG | PWMINSEL |  |
| 1001h | ORCONF1   | FLSEL[2:0]  |           |      | ZPSEL[2:0] |             |      | PDTC  | PWMON    |  |
| 1002h | ORCONF2   | FGSTBLMD    | FGOF[1:0] |      | FDTI[4:0]  |             |      |       |          |  |
| 1003h | ORCONF3   | CLMASK[3:0] |           |      |            | OCMASK[3:0] |      |       |          |  |
| 1004h | ORCONF4   | SROFFT[3:0] |           |      |            | CRMASK[3:0] |      |       |          |  |

OTP write is start when ORCONF4 is written.

Other register value are hold by temporary registers.

These temporary registers are common for all banks.

When ORCONF\* register is read, OTP read data without internal DFF is directly output to SPI read data.



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### ORCONF5 – ORCONF9 (assigned to OTP bank 1)

| ADDR  | Data Name | D[7]       | D[6]      | D[5]        | D[4]  | D[3]       | D[2]  | D[1]  | D[0]    |
|-------|-----------|------------|-----------|-------------|-------|------------|-------|-------|---------|
| 1005h | ORCONF5   | SYNCEN     | PPDOSEL   | FSCDT[1:0]  |       | FSCDL[3:0] |       |       |         |
| 1006h | ORCONF6   | SSCGEN     | CPTM[3:0] |             |       | THTH[1:0]  |       | TSTS  |         |
| 1007h | ORCONF7   | WDTEN      | WDTSEL[2] | WDT[5:0]    |       |            |       |       |         |
| 1008h | ORCONF8   | VCLVPEN    | CPEN      | THWEN       | THPEN | FSPEN      | OVPEN | OCPEN | DIAGSEL |
| 1009h | ORCONF9   | RCVTM[1:0] |           | WDTSEL[1:0] |       | CPLT       | FSPLT | OCPLT | DLTO    |

OTP write is start when ORCONF9 is written.

### ORCONF10 – ORCONF14 (assigned to OTP bank 2)

| ADDR  | Data Name | D[7]           | D[6]         | D[5]            | D[4]             | D[3]         | D[2]         | D[1]         | D[0]     |
|-------|-----------|----------------|--------------|-----------------|------------------|--------------|--------------|--------------|----------|
| 100Ah | ORCONF10  | VDHOVP<br>EN   | OOPOEN       | CLDOEN          | FGERAC<br>CEN    | RCSMPMD      | RCSMPEN      | OPDTM[1:0]   |          |
| 100Bh | ORCONF11  | INIODUT<br>YMD | INITAGMD     | CLREFEN<br>_ROT | CLREFEN<br>_STOP | ATSYN<br>OFF | Internal use | STSYN<br>EN  | SPIINSEL |
| 100Ch | ORCONF12  | FGERDE<br>CEN  | FGERDEC[2:0] |                 |                  | FGERACC[3:0] |              |              |          |
| 100Dh | ORCONF13  | 0              | DWNSET       | PDTSEL[1:0]     |                  | FSPDTM[1:0]  |              | OVPMASK[1:0] |          |
| 100Eh | ORCONF14  | LASET_LIM[4:3] |              | SSTT[5:0]       |                  |              |              |              |          |

OTP write is start when ORCONF14 is written.

### ORCONF15 – ORCONF19 (assigned to OTP bank 3)

| ADDR  | Data Name | D[7]                | D[6]    | D[5] | D[4]         | D[3]                | D[2]    | D[1] | D[0] |  |
|-------|-----------|---------------------|---------|------|--------------|---------------------|---------|------|------|--|
| 100Fh | ORCONF15  | STOSC[7:0]          |         |      |              |                     |         |      |      |  |
| 1010h | ORCONF16  | LASET_LIM[2:0]      |         |      | LASET_L[4:0] |                     |         |      |      |  |
| 1011h | ORCONF17  | MSKRSTNUM0_SIX[3:0] |         |      |              | MSKRSTNUM1_SIX[3:0] |         |      |      |  |
| 1012h | ORCONF18  | CLMSPD[0]           | PX[2:0] |      |              | Internal use        | PG[2:0] |      |      |  |
| 1013h | ORCONF19  | IX[3:0]             |         |      |              | SSCGCN[0]           | IG[2:0] |      |      |  |

OTP write is start when ORCONF19 is written.

### ORCONF20 – ORCONF24 (assigned to OTP bank 4)

| ADDR  | Data Name | D[7]        | D[6]          | D[5] | D[4] | D[3]          | D[2] | D[1]          | D[0] |
|-------|-----------|-------------|---------------|------|------|---------------|------|---------------|------|
| 1014h | ORCONF20  | CLMSPD[1]   | CLSEL         | 0    | 0    | SSCGCN[1]     | 0    | 0             | 0    |
| 1015h | ORCONF21  | OCSEL[0]    | DDUTYSEL[2:0] |      |      | USTEPSEL[1:0] |      | DSTEPSEL[1:0] |      |
| 1016h | ORCONF22  | DUTY_L[7:0] |               |      |      |               |      |               |      |
| 1017h | ORCONF23  | DUTY_H[7:0] |               |      |      |               |      |               |      |
| 1018h | ORCONF24  | TAG_L[7:0]  |               |      |      |               |      |               |      |

OTP write is start when ORCONF24 is written. SSCGCN [1], [0] are separated by ADDR 1013h, 1014h.

### ORCONF25 – ORCONF29 (assigned to OTP bank 5)

| ADDR  | Data Name | D[7]       | D[6]        | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|------------|-------------|------|------|------|------|------|------|
| 1019h | ORCONF25  | OCSEL[1]   | TAG_L[14:8] |      |      |      |      |      |      |
| 101Ah | ORCONF26  | TAG_H[7:0] |             |      |      |      |      |      |      |

**ORCONF25 – ORCONF29 (assigned to OTP bank 5)**

| ADDR  | Data Name | D[7]                | D[6]        | D[5]     | D[4]         | D[3]                | D[2] | D[1] | D[0] |
|-------|-----------|---------------------|-------------|----------|--------------|---------------------|------|------|------|
| 101Bh | ORCONF27  | SLMD                | TAG_H[14:8] |          |              |                     |      |      |      |
| 101Ch | ORCONF28  | WINDSEL[1:0]        |             | CLDWNOFF | LASET_H[4:0] |                     |      |      |      |
| 101Dh | ORCONF29  | MSKRSTNUM0_INI[3:0] |             |          |              | MSKRSTNUM1_INI[3:0] |      |      |      |

OTP write is start when ORCONF29 is written.  
OCSEL[1], [0] are separated by ADDR 1015h, 1019h.

**ORCONF30 – ORCONF34 (assigned to OTP bank 6)**

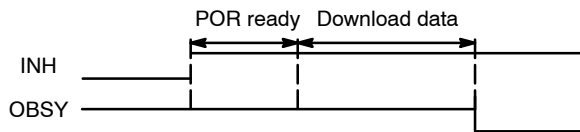
| ADDR  | Data Name | D[7]                | D[6] | D[5] | D[4] | D[3]                | D[2]   | D[1]   | D[0]   |
|-------|-----------|---------------------|------|------|------|---------------------|--------|--------|--------|
| 101Eh | ORCONF30  | MSKRSTNUM0_THR[3:0] |      |      |      | MSKRSTNUM1_THR[3:0] |        |        |        |
| 101Fh | ORCONF31  | MSKRSTNUM0_TWO[3:0] |      |      |      | MSKRSTNUM1_TWO[3:0] |        |        |        |
| 1020h | ORCONF32  | MSKRSTNUM0_ONE[3:0] |      |      |      | MSKRSTNUM1_ONE[3:0] |        |        |        |
| 1021h | ORCONF33  | ORCONF33[7:4]       |      |      |      | RBSEL               | RCSMEN | OSAENB | MSAENB |
| 1022h | ORCONF34  | RCSM[7:0]           |      |      |      |                     |        |        |        |

OTP write is start when ORCONF34 is written.

ORCONF33[7:4] has no register to download, but OTP output is used for checksum calculation.

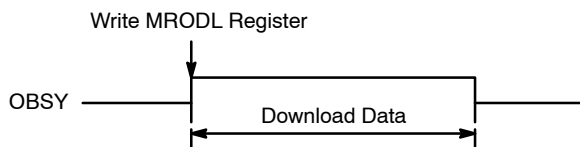
*OTP Data Download*

The OTP register data is typically transferred into the main registers at device startup (From sleep to standby transition). This operation takes up to 340 μs. A high OBSY flag in the first returned byte during a SPI transaction indicates this.



**Figure 22. OTP Data Download Timing at Startup**

An OTP download can also actively be initiated by writing 00h to register MRODL. This command requires monitoring the OBSY flag. Don't perform specific register access (MRCONF, MRSPCT, ORCONF) until the OBSY flag is cleared.



**Figure 23. OTP Data Download Timing after an MRODL Command**

*OTP Programming Overall*

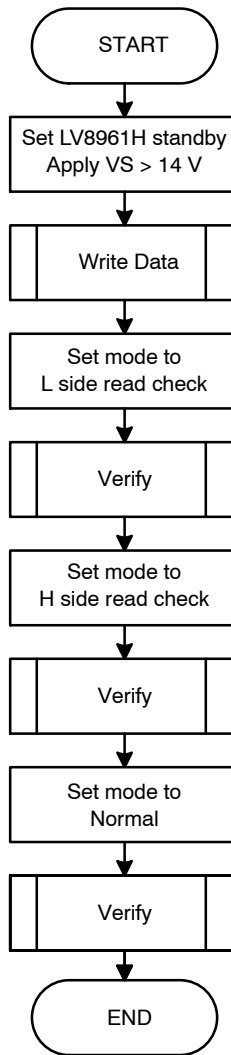
Figure 24 shows overall of the OTP memory write and verify flow. It consists of preparation, write and three times of data integrity verification.

*OTP Programming*

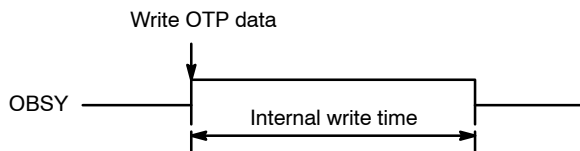
The OTP registers can be programmed in Standby mode only while the write lock bit OSAENB is set 0. And, the supply voltage at pin VS must be more than 1.4 V. The actual write operation to the OTP memory will be done, when the state change from 0 to 1 is commanded. Once the bit state is changed to 1, it cannot be change back to 0. The number of writing is limited to one per bit.

The OTP memory consists of five memory banks. The bank contains five register bytes. The bank is filled by five SPI write transactions. When the last address register in each bank is received, the busy-flag OBSY will be set and those five bytes will be programmed permanently into the corresponding OTP bank. The OBSY flag will be reset at the end of the write cycle. OBSY is in GSDAT register. To get GSDAT, SPI accesses to the register MRACK is recommended. MRACK doesn't interfere with the programming operation. MRCONF, MRSPCT, ORCONF registers cannot be accessed during an OTP write cycle.

MRCONF, MRSPCT, ORCONF, ORSPCT, ORACS registers cannot be accessed during an OTP write cycle.

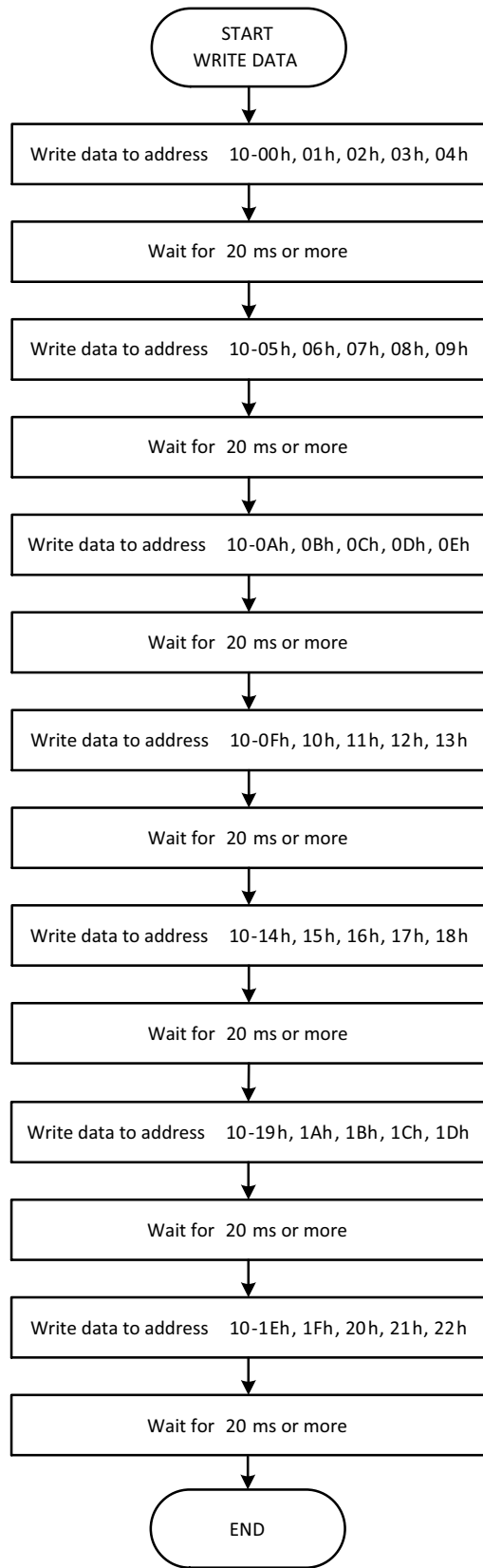


**Figure 24. OTP Memory Write and Verify Flow**



**Figure 25. OTP Programming Timing**

The programming takes 20 ms maximum. To simplify operation, a waiting for 20 ms plus margin can be applicable instead of a polling of the flag OBSY. (Figure 26)



**Figure 26. OTP Memory Write Operation**

*OTP Data Integrity Verification*

In order to verify that the OTP programming operation was successful. It is strongly recommended to do an OTP margin check: To do this, the OTP registers are downloaded into the main register bank with minimum and maximum readout thresholds. This OTP download is forced by writing 00h to register MRODL. The readout threshold is set in register MRORB.

OTP Margin read check sequence after programmed:

1. Set OTP readout threshold “low” by setting ORBEN = 1 and ORBLV = 0 in register MRORB
2. Execute OTP download command by writing 00h to MRODL
3. Verify that the main register contents are consistent with the programmed OTP data
4. Set OTP readout threshold “high” by setting ORBEN = 1 and ORBLV = 1 in register MRORB
5. Execute OTP download command by writing 00h to MRODL

6. Verify that the main register contents are consistent with the programmed OTP data
7. Return OTP threshold to normal by setting ORBEN = 0 and ORBLV = 0
8. Execute OTP download command
9. Verify that the main register contents are consistent with the programmed OTP data

*Locking OTP Register Contents*

MSAENB bit and OSAENB bit of ORCONF33 register are used in order to prevent write-access of the main registers and the OTP registers respectively.

**CAUTION:** Inadvertent writing of these bits will permanently lock the corresponding register blocks from any further write access. Should only be set at end of development cycles.

**ORCONF33**

| ADDR  | Data Name | D[7] | D[6] | D[5] | D[4] | D[3]  | D[2]   | D[1]   | D[0]   |
|-------|-----------|------|------|------|------|-------|--------|--------|--------|
| 1021h | ORCONF33  | 0    | 0    | 0    | 0    | RBSEL | RCSMEN | OSAENB | MSAENB |

*RBSEL: Reverse detection Brake SElection*

RBSEL=0: Short brake is disabled when reverse rotation is detected.

RBSEL=1: Short brake is enabled when reverse rotation is detected.

If RBSEL is set, short brake (all low-side FET are ON) is done until the rotation stops after reverse rotation is detected.

*RCSMEN: Register CheckSuM ENable*

RCSMEN=0: Register checksum diagnostic function is disabled.

RCSMEN=1: Register checksum diagnostic function is enabled.

This register is used in order to permanently prevent write access to the OTP and/or the main registers. This register data is transferred into MRACS register.

*OSAENB: Otp registers Spi Access ENable Bar (Disable)*

- OSAENB = 0: Write access permitted
  - OSAENB = 1: Write access denied
- OSAENB controls write access to the OTP registers.

*MSAENB: Main registers Spi Access ENable Bar (Disable)*

- MSAENB = 0: Write access permitted
  - MSAENB = 1: Write access denied
- MSAENB controls write access to the main registers.

## ORCONF34

| ADDR  | Data Name | D[7]      | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|-------|-----------|-----------|------|------|------|------|------|------|------|
| 1022h | ORCONF34  | RCSM[7:0] |      |      |      |      |      |      |      |

*RCSM: Register CheckSum*

The checksum of whole OTP memory data except this register ORCONF34 needs to be written when the data integrity diagnostic function is enabled. This checksum is a cyclic redundancy check (CRC) which is calculated by the following generator polynomial.

$$x^8 + x^6 + x^3 + x^2 + 1$$

The read out value of the register RCSMSD must be applied to the CRC calculation as a seed. An example CRC calculation program in C language is shown below.

```
// x8 + x6 + x3 + x2 + 1
#define MSB_CRC8      (0x4D)

unsigned char crc_table[256];
unsigned char crc_seed;

static unsigned char GetCRC8_2( unsigned char seed, const void *buff, size_t size )
{
    unsigned char *p = (unsigned char *)buff;
    unsigned char crc8;
    int i;

    for ( crc8 = seed ; size != 0 ; size-- ){
        crc8 ^= *p++;

        for ( i = 0 ; i < CHAR_BIT ; i++ ){
            if ( crc8 & 0x80 ){
                crc8 <<= 1; crc8 ^= MSB_CRC8;
            }
            else{
                crc8 <<= 1;
            }
        }
    }
    return crc8;
}
```

This program is used in the following procedure.

1. Set ORCONF0 through 33 to `crc_table`
2. Set CRC code read from the register RCSMSD to `crc_seed`
3. Call `GetCRC8_2(crc_seed, crc_table, 34)`
4. Use return value for ORCONF34

*Register Checksum Feature*

To activate the register checksum feature, the following register bits must be provided before OTP programming operation.

1. Determine the periodical checksum verify function to be enabled or not, which is specified by the bit RCSMPEN

2. Determine the operation at the checksum error detection: A motor is kept running or stopped, which is specified by the bit RCSMPMD
3. The bit RCSMEN must be set 1 to enable this feature
4. Read out the checksum code (CRC) of the OTP memory reserved area from the register RCSMSD[7:0] whose value may be different by part
5. Letting the RCSMSD be a seed for the CRC calculation, prepare the total checksum (CRC) from ORCON0 to ORCON33, which will be used for the register RCSM[7:0] at ORCONF34

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The following table shows related register bits to this checksum feature.

**Table 14.**

| Register Name | Data Name | Address | Description  |
|---------------|-----------|---------|--|
| RCSMPEN       | ORCONF10  | 100Ah   | Enable the periodical checksum verification while a motor is running   |
| RCSMPMD       | ORCONF10  | 100Ah   | Selection of motor running or stop when the checksum error is detected   |
| RCSMEN        | ORCON33   | 1021h   | Enable the register checksum function  |
| RCSM          | ORCONF34  | 1022h   | Checksum to be written with OTP memory data together, which must be calculated by user, applying the code of RCSMSD as a seed of CRC   |
| RCSMSD        | MRCMSD    | 0208h   | Seed of the register checksum  |
| RCSM          | MRCONF14  | 010Eh   | Calculated checksum which is automatically calculated on this device<br>Code of this register will be compared with the preprogrammed checksum code in the register RCSM at ORCONF34 OTP memory. |
| RCSMPO        | MRDIAG1   | 0202h   | Checksum error flag  |
| RCSMPEN       | MRCONF10  | 010Ah   | Enable the periodical checksum verification while a motor is running.<br>This value will be copied from OTP memory at the device reset or the download operation.                                |
| RCSMPMD       | MRCONF10  | 010Ah   | Selection of motor running or stop when the checksum error is detected<br>This value will be copied from OTP memory at the device reset or the download operation.                               |

**Table 15.**

| Symbol       | Symbol Name Explanation                               |
|--------------|---|
| ATSYNCOFF    | AuTomatic SYNChronous rectification OFF (active low)  |
| BAREG        | Base Address REGister (short format access)           |
| BASEL        | Base Address SELECTION                                |
| BEMFEN       | BEMF detection ENabled                                |
| BRK          | short BRaKe enable                                    |
| CHPLVPO      | CHarge Pump Low Voltage Protection Output             |
| CHPOVPO      | CHarge Pump OverVoltage Protection Output             |
| CLDO         | Current Limit Detection Output                        |
| CLDOEN       | Current Limit Detection Output ENable                 |
| CLDWNOFF     | Current Limit semi-powerDoWN OFF                      |
| CLMASK       | Current Limit MASKing time                            |
| CLMSPD       | Current LiMit Semi-PowerDown level                    |
| CLREFEN_ROT  | Current Limit REFerence ENable (free ROTating status) |
| CLREFEN_STOP | Current Limit REFerence ENable (STOP status)          |
| CLSEL        | Current Limit threshold SELECTION                     |
| CPEN         | Constrained movement Protection ENable                |
| CPLT         | Constrained movement Protection LaTch selection       |
| CPO          | Constrained movement Protection Output                |
| CPTM         | Constrained movement Protection TiMe                  |
| CRDTO        | Current Reversed Detection Output                     |
| CRMASK       | Current Reversed MASKing time                         |
| DDUTYSEL     | Detection level of DUTY output changes SELECTION      |

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**Table 15.** (continued)

| Symbol      | Symbol Name Explanation                                       |
|-------------|---|
| DIAGS       | DIAG Status   |
| DIAGSEL     | DIAG polarity SElection                                       |
| DLTO        | Diagnostics output Latched Transitions Only                   |
| DSTEPSEL    | DownSpeed Transition stEP SElection                           |
| DUTY_H      | input pwm DUTY cycle High limit                               |
| DUTY_L      | input pwm DUTY cycle Low limit                                |
| DWNSET      | slowDoWN SETting  |
| FDTI        | Fet Dead Time   |
| FGERACC     | Frequeny Generator ERrordetection during ACCeleration setting |
| FGERACCEN   | Frequeny Generator ERrordetection during ACCeleration ENable  |
| FGERDEC     | Frequeny Generator ERrordetection during DECeleration setting |
| FGERDECEN   | Frequeny Generator ERrordetection during DECeleration ENable  |
| FGERPO      | Frequency Generator ERror Protection Output                   |
| FGOF        | Frequency Generator Output Frequency (= rotation speed)       |
| FGSTBLMD    | Frequency Generator STaBLe MoDe                               |
| FLSEL       | Full Load fallback level SElection (PWM input 100% duty mode) |
| FRMD        | Forward/Reverse MoDe  |
| FRREN       | FRee Running ENable   |
| FSCDL       | Fet Short-Circuit Detection Level                             |
| FSCDT       | Fet Short-Circuit Detection Time                              |
| FSPDTM      | Fet Short Protection Debounce TiMe setting                    |
| FSPEN       | Fet Short Protection ENable                                   |
| FSPLT       | Fet Short Protection LaTch selection                          |
| FSPO        | Fet Short Protection Output                                   |
| GSDAT       | General Status DATA   |
| HIZON       | Hlgh Z state ON (active)                                      |
| IDUTY_IDUTY | Input DUTYcycle   |
| IG          | Integral Gain   |
| INIODUTYMD  | INItial Output DUTY cycle MoDe (soft start function)          |
| INITAGMD    | INItial max. TARGet output duty cycle MoDe                    |
| IX          | Integral gain eXponent  |
| LACTL_EPOS  | Lead Angle ConTrol Energizing POSition                        |
| LANUM0      | Lead Angle Number 0 (output monitor)                          |
| LANUM1      | Lead Angle Number 1 (control input)                           |
| LASET_H     | Lead Angle SETting at High output duty cycle (100%)           |
| LASET_L     | Lead Angle SETting at Low output duty cycle (0%)              |
| LASET_LIM   | Lead Angle SETting max. LIMit                                 |
| LATCH       | LATCHed shutdown status                                       |
| MRACK       | Main Register Access Check                                    |
| MRACS       | Main Register ACcess Setting                                  |
| MRCONF      | Main Register CONFiguration                                   |
| MRDIAG      | Main Register DIAGnostics                                     |

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**Table 15.** (continued)

| Symbol         | Symbol Name Explanation  |
|----------------|--|
| MRODL          | Main Register Otp DownLoad   |
| MRORB          | Main Register Otp Read Bias check                                  |
| MRRST          | Main Register ReSeT  |
| MRSPT          | Main Register SPeed ConTrol  |
| MSAENB         | Main registers Spi Access ENable Bar (Disable)                     |
| MSKRSTNUM0_INI | same for startup 6–window mode                                     |
| MSKRSTNUM0_ONE | MaSK Rate SeTting for bemf observation NUMber 0, for 1–window mode |
| MSKRSTNUM0_SIX | same for 6–window mode   |
| MSKRSTNUM0_THR | same for 3–window mode   |
| MSKRSTNUM0_TWO | same for 2–window mode   |
| MSKRSTNUM1_INI | same for startup 6–window mode                                     |
| MSKRSTNUM1_ONE | MaSK Rate SeTting for bemf observation NUMber 1, for 1–window mode |
| MSKRSTNUM1_SIX | same for 6–window mode   |
| MSKRSTNUM1_THR | same for 3–window mode   |
| MSKRSTNUM1_TWO | same for 2–window mode   |
| NO_OPEN        | NO OPEN phases detected  |
| OBSY           | Otp BuSY   |
| OCMASK         | OverCurrent MASKing time   |
| OCPEN          | OverCurrent Protection ENable                                      |
| OCPLT          | OverCurrent Protection LaTch selection                             |
| OCPO           | OverCurrent Protection Output                                      |
| OCSEL          | OverCurrent threshold SElection                                    |
| ODL            | Otp DownLoad and checksum  |
| ODUTYMAX       | Output DUTYcycle MAXimum   |
| OOPO           | Open cOnnector Protection Output                                   |
| OOPOEN         | Open cOnnector Protection Output ENable                            |
| OPDTM          | OPen connector Detection TiMe selection                            |
| OPEN_U         | OPEN U phase (active low)  |
| OPEN_V         | OPEN V phase (active low)  |
| OPEN_W         | OPEN W phase (active low)  |
| OPENLX0        | OPEN Loop condition for tag0 (active low)                          |
| ORBEN          | Otp Read Bias check ENable   |
| ORBLV          | Otp Read Bias check LeVel  |
| OSAENB         | Otp registers Spi Access ENable Bar (Disable)                      |
| OTPAZ          | OTP All bits Zero  |
| OVPEN          | OverVoltage Protection ENable                                      |
| OVPMASK        | OverVoltage Protection MASKing time                                |
| PDTC           | Pending Detection of a Transition Control                          |
| PDTSEL         | Pending Detection of a Transition SElection                        |
| PG             | Proportional Gain  |
| PIDOLT         | PI calculated Duty cycle Output resuLT                             |
| PPDOSEL        | Pwm Problem Diagnostics Output SElection                           |



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**Table 15.** (continued)

| Symbol      | Symbol Name Explanation                                |
|-------------|--|
| PROT_F      | Period of ROTation (Frequency)                         |
| PROT_T      | Period of ROTation (Time)                              |
| PWMDTIN     | PWM DuTycycle INput register                           |
| PWMF        | PWM input Frequency selection                          |
| PWMHCNT_LT  | PWM input High CouNT (LaTched)                         |
| PWMINSEL    | PWM INput pin SELECTION                                |
| PWMON       | PWM ON polarity  |
| PWMPCNT_LT  | PWM input Period CouNT (LaTched)                       |
| PWMPO       | PWM input abnormal Protection Output                   |
| PX          | Proportional gain eXponent                             |
| RBSEL       | Reverse detection Brake SELECTION                      |
| RCSM        | Register CheckSuM                                      |
| RCSMEN      | Register CheckSuM ENable                               |
| RCSMPEN     | Register CheckSuM Periodical at running motor ENable   |
| RCSMPMD     | Register CheckSuM error then Power Motor Down          |
| RCSMPO      | Register CheckSuM Protection Output                    |
| RCSMSD      | Register CheckSuM SeeD                                 |
| RCVTM       | ReCoVery TiMe setting                                  |
| RECALC      | RECALCulate target speed from input pwm control table  |
| REGAZ       | otp REGister All bits Zero                             |
| REGCRC_RSLT | REGister CRC ReSuLT                                    |
| REGSEL      | Vcc REGulator SELECTION                                |
| SACF        | Spi ACcess Failed                                      |
| SCEN        | external Speed Control ENable                          |
| SLMD        | SinusoidaL Mode Driving                                |
| SMOD        | Status MODE  |
| SPCFG       | Speed feedback loop calculation Period ConFiGuration   |
| SPCO        | SPEed Control error Output                             |
| SPIINSEL    | duty cycle through SPI INput SELECTION                 |
| SROFFT      | Synchronous Rectification OFF Time                     |
| SSCGCN      | Spread Spectrum Charge pump Generation Clock Number    |
| SSCGEN      | Spread Spectrum Charge pump Generation ENable          |
| SSTT        | Soft STart Time  |
| STATSEL     | STATus data SELECTION                                  |
| STATUS      | internal STATUS output                                 |
| STOSC       | STartup OSCillator                                     |
| STSYNCEN    | sofSTart SYNChronous rectification ENable (active low) |
| STUPO       | bemf-less STartUp Period Output                        |
| SYNCEN      | SYNChronous rectification ENable (active low)          |
| TAG_H       | TARGet speed High                                      |
| TAG_L       | TARGet speed Low                                       |
| TAG0        | TARGet speed/output duty cycle 0 (output monitor)      |

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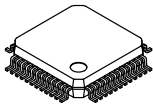
**Table 15.** (continued)

| Symbol     | Symbol Name Explanation                                      |
|------------|--|
| TAG1       | TArGet speed/output duty cycle 1 (control input)             |
| THPEN      | THeRmal Protection ENable                                    |
| THPO       | fet THeRmal Protection Output                                |
| THSPO      | THeRmal Shutdown Protection Output                           |
| THTH       | THeRmal THreshold of THeRmometer                             |
| THWEN      | THeRmal Warning ENable                                       |
| THWPO      | THeRmal Warning Protection Output                            |
| TSTS       | THeRmal Shutdown Temperature Setting                         |
| USTEPSEL   | UpSpeed Transition stEP SELECTION                            |
| VCEN       | VCc Regulator ENable   |
| VCLVPEN    | VCc Low Voltage Protection ENable                            |
| VCLVPO     | VCc Low Voltage Protection Output                            |
| VDHOVPEN   | VDH OverVoltage Protection ENable                            |
| VDHOVPO    | VDH OverVoltage Protection Output                            |
| VGLLVPO    | VGL Low Voltage Protection Output                            |
| VSLVPO     | VS Low Voltage Protection Output                             |
| VSOVPO     | VS OverVoltage Protection Output                             |
| WDT        | WatchDog Timeout duration setting                            |
| WDTEN      | WatchDog Timeout Enable                                      |
| WDTP       | WatchDog Timeout Protection mode selection                   |
| WDTPO      | WatchDog Timer Protection Output                             |
| WDTSEL     | WatchDog Target-duty SELECTION                               |
| WNDCHNG_EN | WiNDoW mode CHaNGe ENabled                                   |
| WINDSEL    | bemf WiNDoW mode SELECTION                                   |
| ZPSEL      | Zero Power fallback level SELECTION (PWM input 0% duty mode) |

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

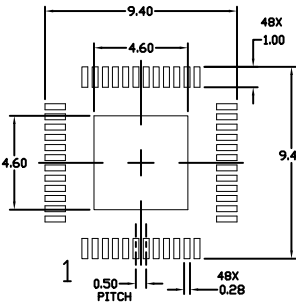
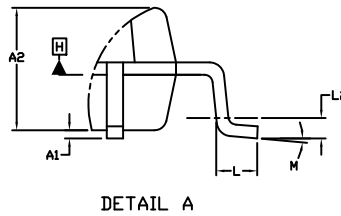
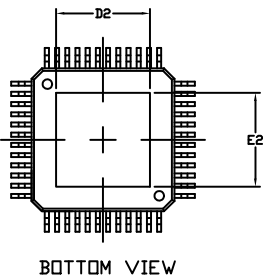
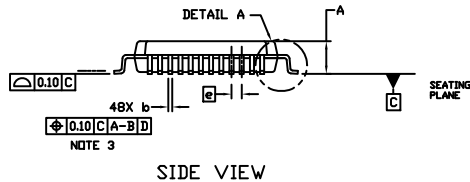
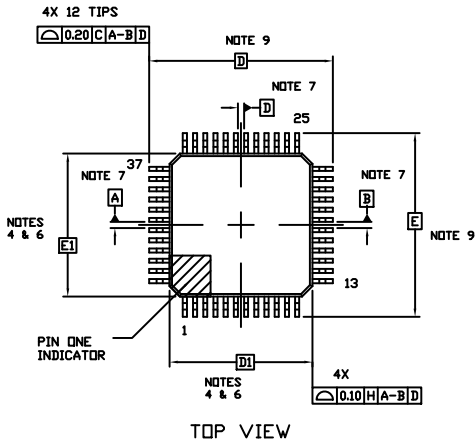


### SPQFP48 7x7 / SQFP48K

#### CASE 131AN

#### ISSUE A

DATE 08 NOV 2013



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN.        | MAX. |
| A   | ---         | 1.70 |
| A1  | 0.00        | 0.15 |
| A2  | 1.50        | REF  |
| b   | 0.15        | 0.26 |
| D   | 9.00        | BSC  |
| D1  | 7.00        | BSC  |
| D2  | 4.60        | REF  |
| E   | 9.00        | BSC  |
| E1  | 7.00        | BSC  |
| E2  | 4.60        | REF  |
| e   | 0.50        | BSC  |
| L   | 0.30        | 0.70 |
| L2  | 0.25        | BSC  |
| M   | 0*          | 10*  |

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