

# 500 mA USB Compatible Single Cell Li-Lon Linear Charger with “Power Back” Capability



ON Semiconductor®

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## FAN54120

The FAN54120 is a small, low-cost, fully integrated single-cell charger which supports dead battery revival, pre-charge, fast charge, and float charge states.

Fast charging current ( $I_{FAST}$ ) is set with an external resistor. Pre-charge ( $I_{PRE}$ ) and charge complete ( $I_{CHGEND}$ ) currents are factory set at  $I_{FAST}/5.2$  and  $I_{FAST}/10$ , respectively.

The FAN54120 is specifically designed for ease-of-use as a stand-alone charger. It requires no user interaction or active supervision.

An open-drain  $\overline{STAT}$  pin provides charge and/or fault status indication.

“Power Back” capability to source accessories from the battery.

The FAN54120 is available in a 2x2 DFN package or a 1.36x0.76 mm WLCSP.

### Features

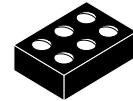
- Fully Integrated Charger for Single Cell Li-Ion or Li-Polymer Batteries
- Factory Configured Charge Voltage (Ordering Option)
- $\pm 0.5\%$  Charge Voltage Accuracy
- User Determined Fast Charge Current Via External Resistor
- $\pm 4\%$  Charge Current Accuracy
- 28 V Maximum Input Voltage, 6 V Operating
- Ultra-low Battery Discharge Current ( $<120$  nA)
- True Reverse Current Blocking
- Adaptive Thermal Regulation
- Supports JEITA Safe-to-Charge Operation with an External NTC
- “Power Back Functionality to Power Accessories from the Battery

### Application

- IoT Devices
- E-Cigs / Vapes
- Personal Mobile Devices (Games, Camera, etc.)
- Toys
- Point-of-Sale Instruments

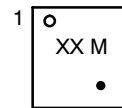


DFN6 2x2, 0.65P  
CASE 506DQ



WLCSP6 1.36x0.76  
CASE 567XQ

### MARKING DIAGRAM



XX = 20, Specific Device Number  
M = One Digit Date Code  
● = Pb Free

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

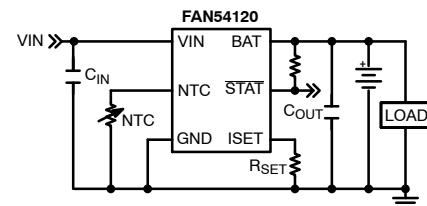


Figure 1. Typical Application

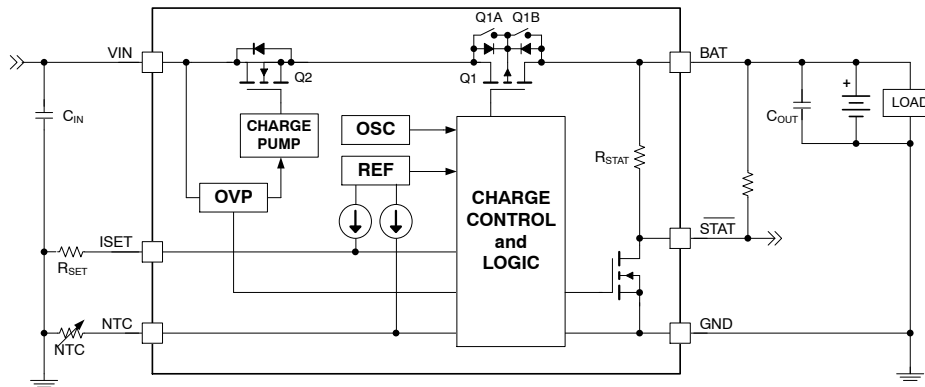
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**Table 1. ORDERING INFORMATION**

Part Number	V <sub>FLOAT</sub> (V)	Package	Packing Method <sup>†</sup>
FAN54120MP420X	4.20	DFN6, 2x2 mm (Pb Free)	3000 / Tape & Reel
FAN54120MP425X	4.25		
FAN54120MP435X	4.35		
FAN54120UC420X	4.20	WLCSP-6, 1.36x0.76 mm (Pb Free)	3000 / Tape & Reel
FAN54120UC425X	4.25		
FAN54120UC435X	4.35		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## BLOCK DIAGRAM



**Figure 2. Simplified Block Diagram**

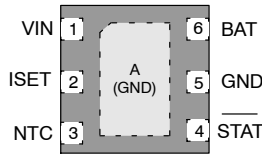
**Table 2. RECOMMENDED EXTERNAL COMPONENTS**

Component	Description	Supplier	Parametr	Unit	Typ.
C <sub>IN</sub>	1.0 μF, 25 V, 10%, X5R, 0603	Murata GRM188R61E105KAAD	C	μF	1.0 (Note 2)
C <sub>OUT</sub> (Note 1)	1.0 μF, 10 V, 10%, X5R, 0402	Murata GRM155R61A105KE15	C	μF	1.0 (Note 2)
NTC	10 KΩ, 1%, B <sub>25/85</sub> = 3380, 0402	Murata NCP15XH103F03RC	R <sub>25</sub>	KΩ	10

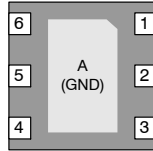
1. The minimum required C<sub>OUT</sub> value is shown. The expected bypass capacitance range is 1 μF to 10 μF. For applications with large dynamic pulsed loads, additional C<sub>OUT</sub> may be necessary to constraint voltage deviations.
2. The typical (face) value does not include the effects of applied voltage or temperature de-rating.

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## PIN CONNECTIONS



Top View



Bottom View

Figure 3. DFN Package

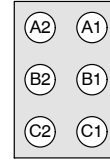
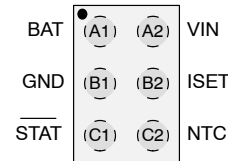


Figure 4. WLCSP Package

Table 3. PIN DEFINITIONS

DFN Pin	WLCSP Pin	Pin Name	Description
1	A2	VIN	Input Voltage. Connect $C_{IN}$ bypass directly to VIN and GND pins on top layer.
2	B2	ISET	Set Charge Current. Connect $R_{SET}$ directly to GND to set the maximum input/charging current ( $I_{FAST}$ ).
3	C2	NTC	NTC input. Connect to battery pack NTC to provide JEITA "safe-charging" functionality. See "NTC Pin" applications section for additional usage information.
4	C1	STAT	Status. Open-drain output used to indicate charge and/or fault status. Internally, there is a weak pull-up ( $R_{STAT}$ ) to BAT. This pin is also used to enable Power Back operation.
5, A	B1	GND	Ground. Connect to system GND plane. $C_{IN}$ and $C_{OUT}$ also connect directly to this pin on top layer.
6	A1	BAT	Output. Connect to system load and positive terminal of battery. Bypass with $C_{OUT}$ , connected directly to BAT and GND pins on top layer.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
$V_{IN}$	Voltage on VIN Pin	-1.2	28.0	V
$V_{IN\_SLEW}$	VIN Rise Time, $V_{IN} > 6$ V		10	V/ $\mu$ sec
$V_{BAT}$	Voltage on BAT Pin	-0.3	6.3	V
$V_X$	Voltage on All Other Pins	-0.3	(Note 3)	V
ESD	Electrostatic Discharge Protection Level, HBM per JESD22-A114		1500	V
	Electrostatic Discharge Protection Level, CDM per JESD22-C101		2000	V
LU	Latch Up per JESD78, Class I, 25°C		$\pm 100$	mA
$T_J$	Junction Temperature	-40	+150	°C
$T_{STG}$	Storage Temperature	-65	+150	°C
$T_{LS}$	Lead Soldering Temperature, 10 Seconds		+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Lesser of 6.3 V or the higher of  $V_{IN} + 0.3$  V or  $V_{BAT} + 0.3$  V.

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**Table 5. RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IN</sub>	Voltage on VIN Pin	4	6	V
V <sub>BAT</sub>	Battery Voltage	2.5	4.5	V
T <sub>A</sub>	Ambient Temperature	-30	+85	°C
T <sub>J</sub>	Junction Temperature	-30	+120	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOTE: The Recommended Operating Conditions table defines the conditions for actual device operation using the circuit of Figure 1, with the Recommended External Components shown in Table 2. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. On Semiconductor does not recommend exceeding them or designing to the Absolute Maximum Ratings.

**Table 6. THERMAL PROPERTIES**

Symbol	Parameter		Typical	Unit
θ <sub>JA</sub>	Thermal Resistance, Junction to Ambient	DFN-6	75	°C/W
		CSP-6	140	
θ <sub>JB</sub>	Thermal Resistance, Junction to Board (Note 4)	DFN-6	50	°C/W
		CSP-6	70	

NOTE: Thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance with JEDEC standard JESD51. Special attention must be paid to not exceed junction temperature T<sub>J(max)</sub> at a given ambient temperature T<sub>A</sub>.

4. θ<sub>JB</sub> measured using On Semiconductor evaluation board.

**Table 7. ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, circuit of Figure 1 with V<sub>IN</sub> = 5.0 V, V<sub>FLOAT</sub> = 4.2 V, V<sub>BAT</sub> = 3.9 V, R<sub>SET</sub> = 1.0 kΩ, over recommended T<sub>A</sub> operating temperature range. Typical values are at 25°C.)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
<b>POWER SOURCES</b>						
V <sub>IN(RISE)</sub>	V <sub>IN</sub> Rising UVLO Threshold	V <sub>BAT</sub> ≤ 3.9 V	4.25	4.40	4.55	V
V <sub>IN(FALL)</sub>	V <sub>IN</sub> Falling UVLO Threshold	V <sub>BAT</sub> ≤ 2.9 V	3.00	3.15	3.30	V
V <sub>SLP_R</sub>	Sleep Comparator Threshold	V <sub>IN</sub> - V <sub>BAT</sub> Rising		80		mV
V <sub>SLP_F</sub>		V <sub>IN</sub> - V <sub>BAT</sub> Falling		30		mV
t <sub>IN_VALID</sub>	VIN Validation Time (Note 7)	V <sub>IN</sub> > V <sub>IN(RISE)</sub>		32		msec
R <sub>IN_VALID</sub>	VIN Validation Load			100		Ω
V <sub>VAL_HYST</sub>	VIN Validation Hysteresis	V <sub>IN</sub> Drop, from V <sub>IN(RISE)</sub> , During Validation		200		mV
I <sub>IN_Q</sub>	VIN Quiescent Current	5.0 V <sub>IN</sub> , I <sub>BAT</sub> = 0, NTC = GND, R <sub>SET</sub> = 10 kΩ		600	720	μA
V <sub>DROP</sub>	Drop-Out Voltage (V <sub>IN</sub> - V <sub>BAT</sub> )	V <sub>IN</sub> = 4.75 V, R <sub>SET</sub> = 1 kΩ		280	450	mV
I <sub>BAT_LKG</sub>	Battery Discharge Current, Sleep Mode	V <sub>BAT</sub> = 4.2 V, VIN Open		120	300	nA
I <sub>VIN_LKG</sub>	BAT-to-VIN Leakage Current	V <sub>BAT</sub> = 4.2 V, V <sub>IN</sub> = 0 V			300	nA
V <sub>IN_OVP</sub>	VIN Over-Voltage Protection Threshold	Rising V <sub>IN</sub>	6.0	6.3	6.6	V
<b>CHARGER VOLTAGE REGULATION</b>						
V <sub>FLOAT</sub>	Float Voltage Range, V <sub>BAT</sub>	Fixed Factory Set-point, 50 mV Increments	4.20		4.35	V
	Float Voltage Accuracy, V <sub>BAT</sub> (Note 7)	0 ≤ T <sub>J</sub> ≤ +50°C	-0.5		0.5	%
		-10 ≤ T <sub>J</sub> ≤ +85°C	-1.2		+1.0	%
		-30 ≤ T <sub>J</sub> ≤ +120°C	-1.5		+1.0	%
V <sub>BATMIN</sub>	Pre-to-Fast Charge Threshold	Rising V <sub>BAT</sub>	2.9	3.1	3.3	V
V <sub>RCH</sub>	Battery Recharge Indicator Threshold	V <sub>BAT</sub> Falling Below V <sub>FLOAT</sub> - V <sub>RCH</sub>		120		mV
V <sub>SHORT</sub>	Battery Short Circuit Threshold	Rising V <sub>BAT</sub>	2.1	2.2	2.3	V

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**Table 7. ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, circuit of Figure 1 with  $V_{IN} = 5.0\text{ V}$ ,  $V_{FLOAT} = 4.2\text{ V}$ ,  $V_{BAT} = 3.9\text{ V}$ ,  $R_{SET} = 1.0\text{ k}\Omega$ , over recommended  $T_A$  operating temperature range. Typical values are at  $25^\circ\text{C}$ .) (continued)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
<b>CHARGER VOLTAGE REGULATION</b>						
$V_{SC\_HYST}$	Battery Short Circuit Hysteresis	Falling $V_{BAT}$		100		mV
<b>CHARGER CURRENT REGULATION</b>						
$I_{FAST}$	Fast Charge Current Range	$10\text{ k}\Omega \geq R_{SET} \geq 1.0\text{ k}\Omega$	50		500	mA
	Fast Charge Current Accuracy (Note 5)	$R_{SET} = 1.0\text{ k}\Omega$	460	480	500	mA
		$R_{SET} = 2.5\text{ k}\Omega$	180	192	205	mA
		$R_{SET} = 10\text{ k}\Omega$	40	48	56	mA
$I_{PRE}$	Pre-Charge Current	$V_{SHORT} < V_{BAT} < V_{BATMIN}$		$I_{FAST} / 5.2$		mA
	Pre-Charge Current Accuracy (Note 5) (Note 6)	$R_{SET} = 1.0\text{ k}\Omega$	-6		+6	%
		$R_{SET} = 2.5\text{ k}\Omega$	-8		+8	%
		$R_{SET} = 10\text{ k}\Omega$	-10		+10	%
$I_{CHGEND}$	Charge Complete Current			$I_{FAST} / 10$		mA
	Charge Complete Current (Note 5) (Note 6)	$R_{SET} = 1.0\text{ k}\Omega$	-8		+8	%
		$R_{SET} = 2.5\text{ k}\Omega$	-10		+10	%
		$R_{SET} = 10\text{ k}\Omega$	-15		+15	%
$t_{CHGENE}$	Charge Complete Qualification Time (Note 7)	Operating in $V_{FLOAT}$ Mode		32		msec
$R_{SET\_SC}$	Minimum $R_{SET}$ Value	$R_{SET} \leq R_{SET\_SC}$ Results in Output Fault State			900	$\Omega$
$T_{RSET\_SC}$	Shorted $R_{SET}$ Qualification Time (Note 7)			1		msec
<b>STAT PIN</b>						
$I_{STAT(HI)}$	$\overline{STAT}$ Pin Leakage	$V_{STAT} = 4.5\text{ V}$			100	nA
$V_{STAT(LO)}$	$\overline{STAT}$ Sink Capability	$I_{STAT} = 5\text{ mA}$			0.4	V
$R_{STAT}$	$\overline{STAT}$ Internal Pull-Up			1		M $\Omega$
<b>NTC PIN</b>						
$I_{NTC}$	Source Current	$V_{IN}$ Valid, $100\text{ mV} < V_{NTC} < 2.0\text{ V}$	48	50	52	$\mu\text{A}$
		NTC = GND		Off		
$T_{0C}$	Cold Non-Charging Threshold	Rising $V_{NTC}$ , Charging Ceases	1225	1255	1285	mV
$T_{45C}$	Warm Charging Threshold	Falling $V_{NTC}$ , Charge Reduction ( $T_{JEITA}$ , $I_{JEITA}$ )	255	270	280	mV
$T_{60C}$	Hot Non-Charging Threshold	Falling $V_{NTC}$ , Charging Ceases	160	170	180	mV
$t_{NTC}$	NTC pin Sampling Interval (Note 7)	$100\text{ mV} < V_{NTC} < 2.0\text{ V}$		1		sec
$T_{JEITA}$	$V_{FLOAT}$ Reduction	$T_{45C} \geq V_{NTC} \geq T_{60C}$		200		mV
$I_{JEITA}$	$I_{FAST}$ Reduction	$T_{45C} \geq V_{NTC} \geq T_{60C}$		20		%
<b>THERMAL PROTECTION</b>						
$T_{REG}$	Thermal Regulation Threshold (Note 7) (Note 8)	$T_J$ Rising	109	120	130	$^\circ\text{C}$
$T_{REG\_HYST}$	Thermal Regulation Hysteresis (Note 7)	$T_J$ Falling		20		$^\circ\text{C}$
$I_{TREG}$	Adaptive Thermal Regulation Foldback (Note 7)		40		80	% $I_{FAST}$
$T_{SDOWN}$	Thermal Shutdown Threshold (Note 7) (Note 8)	$T_J$ Rising	130	145	160	$^\circ\text{C}$
	Hysteresis (Note 7)	$T_J$ Falling		$T_{REG}$		$^\circ\text{C}$
$t_{TSD\_QUAL}$	Thermal Shutdown Qualification Time (Note 7)	$T_J$ Rising		1		msec
$t_{DIE\_T}$	Die Temperature Sampling Rate (Note 7)			32		msec

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**Table 7. ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, circuit of Figure 1 with  $V_{IN} = 5.0\text{ V}$ ,  $V_{FLOAT} = 4.2\text{ V}$ ,  $V_{BAT} = 3.9\text{ V}$ ,  $R_{SET} = 1.0\text{ k}\Omega$ , over recommended  $T_A$  operating temperature range. Typical values are at  $25^\circ\text{C}$ .) (continued)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
<b>TIMERS</b>						
$t_{PRE\_SC}$	Pre-Charge Fault Timer (Note 7)			32		msec
$t_{OSC}$	Internal Oscillator Accuracy	Applies to All Timers/Counters	-15		+15	%
$t_{IN\_REVAL}$	Input Re-Validation Attempt Period (Note 7)			2		sec
<b>POWER BACK</b>						
$V_{STAT\_IN(HI)}$	$\overline{STAT}$ Pin Input Logic HIGH Threshold	No $V_{IN}$ Applied, $V_{BAT} > V_{BATMIN}$	1.2			V
$V_{STAT\_IN(LO)}$	$\overline{STAT}$ Pin Input Logic LOW Threshold	No $V_{IN}$ Applied, $V_{BAT} > V_{BATMIN}$			0.4	V
$V_{PBAK(UVLO)}$	Power Back UVLO Threshold	Not Start if $V_{BAT} < V_{BATMIN}$		$V_{BATMIN}$		V
$t_{PBACK(ST)}$	Power Back Start Delay (Note 7)	Falling $\overline{STAT}$ until $V_{IN}$ Rise Commences		2.7		msec
$I_{PBACK(ST)}$	Power Back Start-Up Inrush (Note 7)	$3.9 V_{BAT}$ , No $V_{IN}$ Load		180		mA
$I_{Q\_PBACK}$	Power Back Quiescent Current			100	150	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Current accuracies are specified with minimum 50 mV overhead ( $V_{IN} - V_{BAT}$ )
6. Specified accuracy relative to actual/nominal  $I_{FAST}$  level.
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Not tested in production.
8. Power Back mode uses  $T_{REG}$  as thermal shutdown threshold.

TYPICAL CHARACTERISTIC

Unless otherwise specified, circuit of Figure 1 with  $V_{IN} = 5.0\text{ V}$ ,  $V_{FLOAT} = 4.2\text{ V}$ ,  $V_{BAT} = 3.8\text{ V}$ ,  $R_{SET} = 1.0\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ .

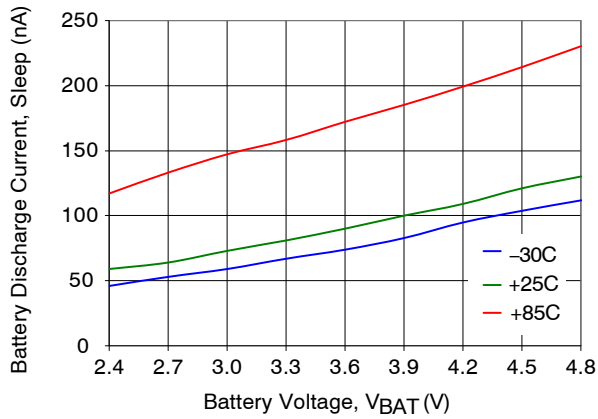


Figure 5. Sleep Mode Discharge Current

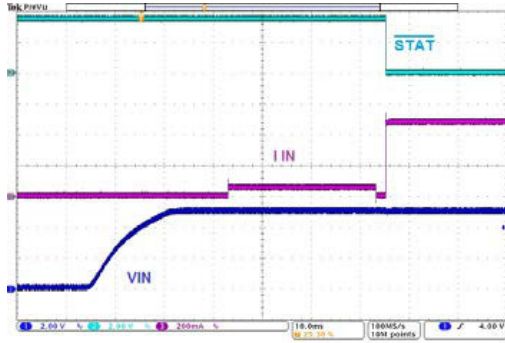


Figure 6. Start-Up VIN Insertion,  $V_{BAT} = 3.8\text{ V}$

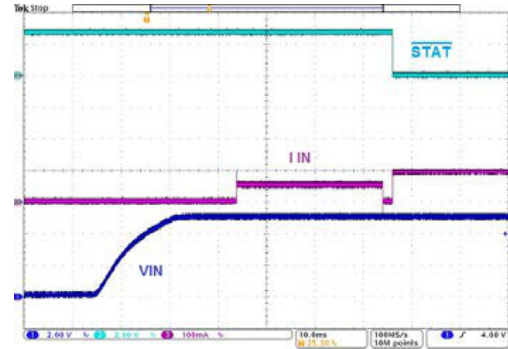


Figure 7. Start-Up at VIN Insertion,  $V_{BAT} = 2.9\text{ v}$

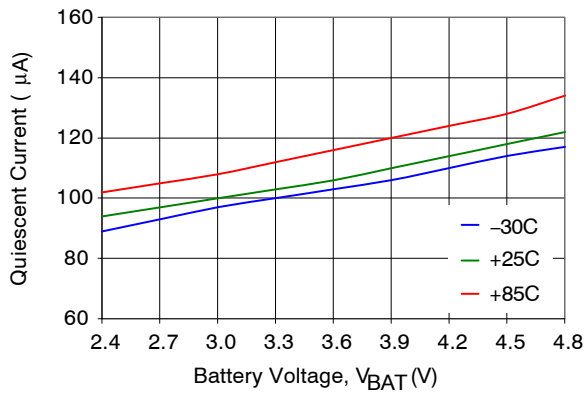


Figure 8. Power Back Mode Quiescent Current

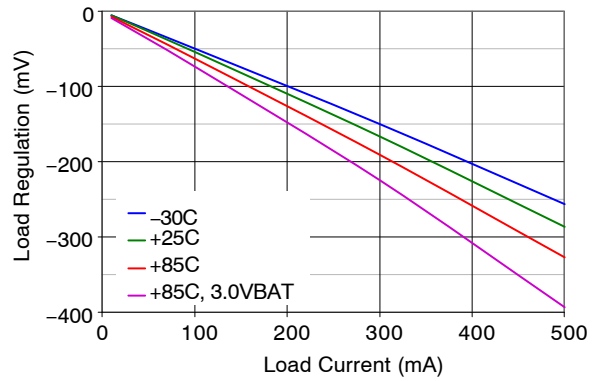


Figure 9. Power Back Mode Output Regulation

## OPERATION / APPLICATION INFORMATION

### ISET Pin – Setting the Charge Current ( $I_{FAST}$ )

$R_{SET}$ , connected to the ISET pin, is used to establish the maximum charging current ( $I_{FAST}$ ). Input current will be slightly higher due to the quiescent current of the device flowing to GND.

$$I_{FAST}(mA) = 500 \div R_{SET(k\Omega)}$$

valid  $R_{SET}$  range:  $1.0\text{ k}\Omega \leq R_{SET} \leq 10\text{ k}\Omega$

The accuracy/tolerance of the chosen  $R_{SET}$  will directly influence the tolerance/accuracy of  $I_{FAST}$ .

Selecting an  $R_{SET}$  value outside the specified range can result in a non-charging state.

An open ISET pin will set  $I_{FAST} \sim 0$ , resulting in battery discharge into the prevailing system load, even though the IC may attempt to regulate  $V_{FLOAT}$ .

Selecting  $R_{SET} \leq R_{SET\_SC}$  also results in a non-charging state. In this case, the IC will enter the Output Fault State, where it is latched off until the input power ( $V_{IN}$ ) is recycled.

### STAT Pin

In Charge mode, the  $\overline{STAT}$  pin, when asserted LOW, indicates that the battery is being actively charged.  $\overline{STAT}$  will remain HIGH during non-charging or fault states.

The  $\overline{STAT}$  pin asserts LOW when:

- Charging ( $I_{PRE}$  or  $I_{FAST}$ )
- Thermal regulation
- Re-charge, battery drops below  $V_{FLOAT} - V_{RCH}$  with a valid  $V_{IN}$  present
- $T_{45C} \leq V_{NTC} \leq T_{60C}$  (warm charging, JEITA reduction)

The  $\overline{STAT}$  pin is HIGH during:

- Absence of a validated  $V_{IN}$
- Charge done ( $I_{BAT} \leq I_{CHGEN}$ )
- Thermal shutdown
- Input Over-Voltage ( $V_{IN\_OVP}$ ) state
- Output Fault state ( $V_{BAT} \leq V_{SHORT}$ )
- $V_{NTC} \geq T_{0C}$  (cold non-charging threshold)
- $V_{NTC} \leq T_{60C}$  (hot non-charging threshold)

The  $\overline{STAT}$  pin is also used to enable Power Back Mode (see Power Back Operation section).

### NTC Pin – JEITA Functionality

The FAN54120 supports the JEITA Safe-to-Charge profile using the battery pack internal NTC device or a discrete NTC placed in close proximity to the battery.

The fixed threshold voltages are designed consistent with  $I_{NTC}$  sourcing a nominal NTC value of  $10\text{ k}\Omega$ , 1% and  $B_{25/85} = 3380$ . Other NTC devices can be used, although the corresponding threshold temperatures may shift.

At temperatures below the cold threshold ( $< T_{0C}$ ) or above the hot threshold ( $> T_{60C}$ ), charging is suspended and the pin tri-states.

At temperatures between the warm threshold ( $> T_{45C}$ ) and hot threshold ( $< T_{60C}$ ),  $V_{FLOAT}$  is internally reduced by  $V_{JEITA}$  and  $I_{FAST}$  is internally reduced by  $I_{JEITA}$  to prevent an unsafe charging condition. The  $\overline{STAT}$  pin remains asserted low.

For applications where the NTC device is undesired or not available, using a fixed  $10\text{ k}\Omega$   $R_{SET}$  will allow full charging without JEITA limitations.  $I_{NTC}$  remains on.

Similarly, connecting the NTC pin to GND will result in  $I_{NTC}$  being turned off and the JEITA thresholds disabled.

Leaving the NTC pin open/floating will result in a non-charging state.

*It is the system designer's responsibility to ensure a safe charging environment, particularly when the JEITA feature is not utilized.*

### Input Power Connection and Validation

With no  $V_{IN}$  present (sleep state), Q2 and Q1 are off and the Q1A body switch is open.

Once  $V_{IN}$  rises above  $V_{IN(RISE)}$ , Q2 is gradually enhanced. Q1 remains off until Input Validation completes. If  $V_{IN} \geq V_{IN\_OVB}$  Q1 remains off until  $V_{IN}$  falls below  $V_{IN\_OVHYS}$  and Input Validation occurs.

After Q2 is enhanced for  $\sim 16\text{ms}$ , Input Validation occurs. A load ( $R_{IN\_VALID}$ ) is applied to the input for  $t_{IN\_VALID}$ .  $V_{IN}$  must remain above the  $V_{VAL\_HYST}$  threshold for successful validation. If  $V_{IN}$  does not remain above  $V_{VAL\_HYST}$ ,  $R_{IN\_VALID}$  is suspended and validation fails. If Input Validation fails, periodic validation attempts will be repeated at a rate of  $t_{IN\_REVAL}$  while  $V_{IN}$  remains above the higher of  $V_{IN(FALL)}$  or  $V_{BAT} + V_{SLP}$ .

### CHARGING

Charging does not commence until the Input Validation, cycle completes. Q1 remains disabled and the  $\overline{STAT}$  pin is open-drain until charging starts.

### Charging States

Figure 10 illustrates a common Li+ charging profile, starting with a depleted battery:

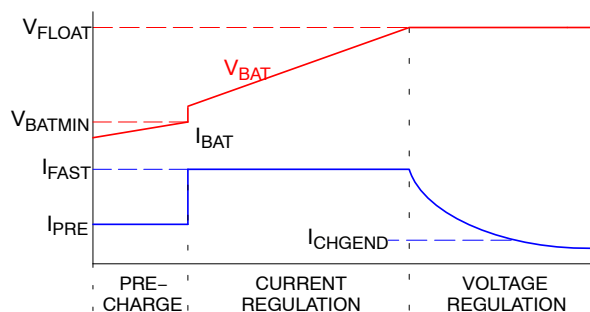


Figure 10. Typical Charging Profile



During the pre-conditioning stage (Pre-Charge), a constant current  $I_{PRE}$  ( $I_{FAST}/5.2$ ) is applied until the battery voltage reaches  $V_{BATMIN}$ .

Once  $V_{BAT} \geq V_{BATMIN}$ , the fast charging current ( $I_{FAST}$ ) is applied.  $I_{FAST}$  is set with a discrete resistor ( $R_{SET}$ ) at the ISET pin. The instantaneous jump of  $V_{BAT}$  at  $V_{BATMIN}$ , is representative of the charging current increase across the series resistance of the battery path. The Current Regulation stage is maintained until  $V_{BAT}$  reaches  $V_{FLOAT}$ .

During the Voltage Regulation stage, charge current diminishes as the actual battery cell voltage approaches  $V_{FLOAT}$ .  $I_{BAT}$  is continuously monitored and, when it decreases to the charge complete ( $I_{CHGEND}$ ) threshold ( $I_{FAST}/10$ ), the battery is considered fully charged. Prior to entering the charge complete state,  $V_{FLOAT}$  control must be maintained, uninterrupted, for  $t_{CHGEND}$ . The IC continues  $V_{FLOAT}$  operation to support the load.

Once End-of-Charge is established, the  $\overline{STAT}$  pin tri-states until a new or re-charge cycle starts. A re-charge cycle is entered when  $V_{BAT} \leq V_{FLOAT} - V_{RCH}$ , where the  $\overline{STAT}$  pin re-asserts LOW until END-of-Charge is reached.

#### Output Fault State

This state is entered whenever  $V_{BAT} \leq V_{SHORT}$  after charging commences or  $R_{SET} \leq R_{SET\_SC}$  during start-up to prevent potentially destructive currents in the device.

An Output Fault State will result in Q1, Q1A, and Q2 being latched off until input power ( $V_{IN}$ ) is fully recycled.

Output Fault state is also entered at commencement of charging if  $I_{PRE}$  fails to charge  $V_{BAT} > V_{SHORT}$  before the  $t_{PRE\_SC}$  timer expires.

#### Input Disconnect/Detach

Upon removal of the input voltage source, as  $V_{IN}$  falls below the higher of  $V_{IN(FALL)}$  or  $V_{BAT} + V_{SLB}$ , Q1 opens and  $R_{IN\_VALID}$  is applied to discharge input caps. If  $V_{IN}$  remains below the  $V_{IN(FALL)}$  level, sleep state is entered. Otherwise, periodic re-validation attempts occur.

#### Input Over-Voltage Protection

When rising  $V_{IN}$  reaches the input over-voltage threshold ( $V_{IN\_OVP}$ ), Q1 turns off, charging stops, and the  $\overline{STAT}$  pin becomes open drain. Automatic re-start occurs, with soft-start, once  $V_{IN}$  falls below  $V_{IN\_OVHYS}$  and is re-validated.

#### Thermal Regulation

The FAN54120 autonomously reduces power dissipation upon reaching the thermal regulation temperature threshold ( $T_J \geq T_{REG}$ ). It employs an adaptive scheme ( $I_{TREG}$ ), which incrementally reduces charge current to nullify excessive temperature rise. It results in a higher average charging current being maintained than more traditional methods, for instance, reducing the charge current by half until the device cools.

While in the thermal regulation state, charge current is modulated to maintain device temperature between the  $T_{REG}$  and  $T_{REG\_HYS}$  thresholds and  $\overline{STAT}$  remains asserted.

#### Thermal Shutdown

To prevent potentially catastrophic device failure, a 2<sup>nd</sup> level of thermal protection is provided. If  $T_J$  reaches the thermal shutdown threshold ( $T_{SDOWN}$ ), charging will be stopped until the device cools to  $T_{REG}$ . During this time, the  $\overline{STAT}$  pin will be open-drain.

#### Disable

FAN54120 does not have a dedicated Enable/Disable pin. With a valid  $V_{IN}$  present, the system can disable charging by forcing the NTC pin higher than 1.5 V or creating an open circuit on the NTC pin. Although charging will cease, the device does not fully enter the low power sleep state. Battery discharge current will remain minimal due to device  $I_Q$  being drawn from  $V_{IN}$ .

#### POWER BACK OPERATION

Power Back provides an un-regulated output on the VIN pin to power peripheral accessories, using the battery as the power source. For a given battery voltage ( $V_{BAT}$ ), the output will exhibit a finite output impedance equivalent to FAN54120  $R_{DS}$  plus battery and protection switch ESR.

Power Back operation is initiated by forcing a transition of the  $\overline{STAT}$  pin from HIGH to below  $V_{STAT(LO)}$ . The IC ignores this input signal if  $V_{IN}$  is present,  $V_{BAT} \leq V_{PBAK(UVLO)}$ , or if  $V_{STAT}$  was never greater than  $V_{STAT(HI)}$  prior to forcing it LOW. The normal  $\overline{STAT}$  pin functionality, associated with charging, is disabled during Power Back operation.

A soft-start feature is employed to limit inrush current from the battery to charge potentially large accessory input capacitors, parallel to  $C_{IN}$ .

During Power Back operation, the thermal shutdown protection threshold is  $T_{REG}$ . Thermal shutdown will result in latching open the current path between the BAT and VIN pins. To restore Power Back operation, the  $\overline{STAT}$  pin must be recycled HIGH, then back LOW.

In the event that a charging source is applied at the VIN pin while in Power Back mode, Power Back operation is automatically disabled, momentarily forcing the device into Sleep State during the Charging Validation Cycle.

PCB Layout Guideline

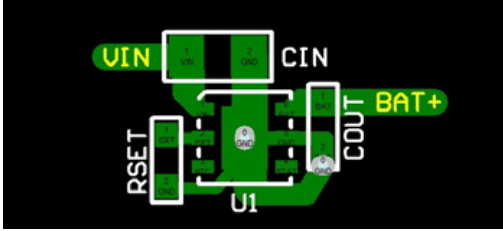


Figure 11. Example Layout, FAN54120MP (DFN)

Place  $C_{IN}$  and  $C_{OUT}$  as close possible to the IC. Connect the capacitors directly to the appropriate IC pins on the top layer. Reference the circuit to the system GND plane, typically on an inner layer, using a via in the IC DAP and/or at the GND side of  $C_{OUT}$ .

The GND side of  $R_{SET}$  should be routed with a trace directly to IC GND, rather than using a via to the GND plane. This prevents transient currents in GND plane from influencing the IC's current regulation.

The same practices should be applied to the WLCSP version. Due to the lack of a DAP on the CSP, the GND side of  $C_{IN}$  should be connected by via to the system GND plane.

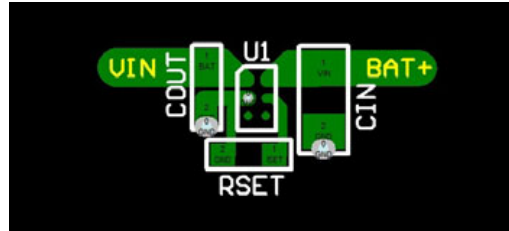
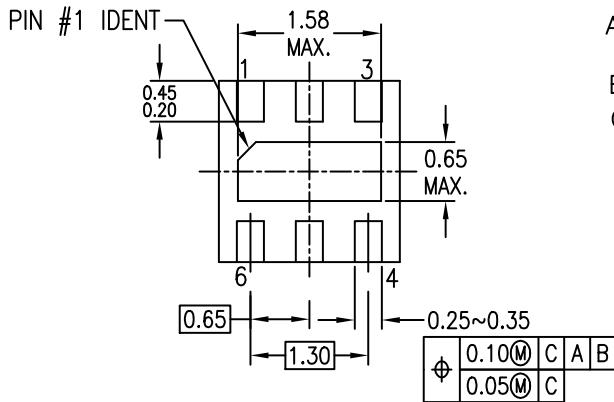
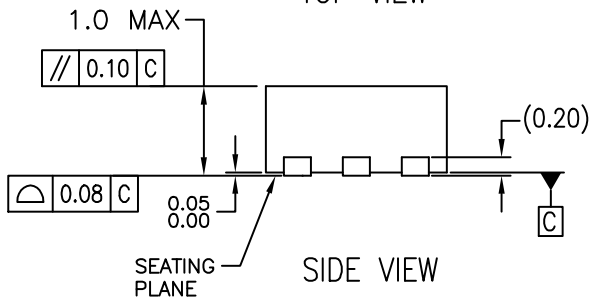
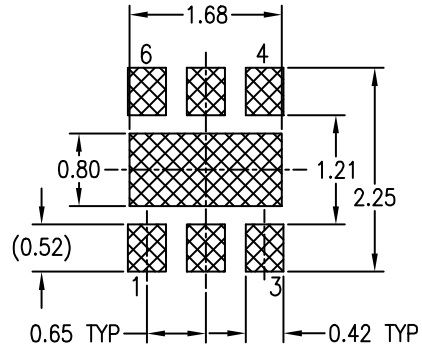
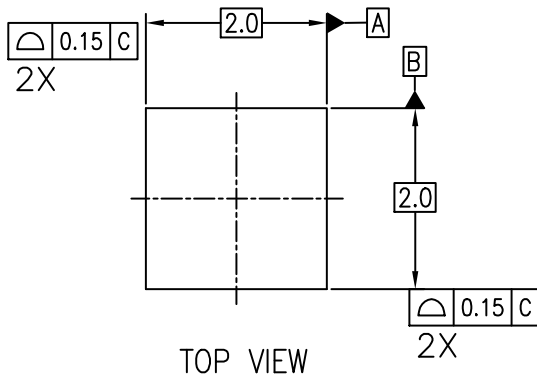


Figure 12. Example Layout, FAN54120UC (CSP)

**DFN6 2x2, 0.65P**  
CASE 506DQ  
ISSUE O

DATE 31 AUG 2016



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC, DATED 11/2001
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

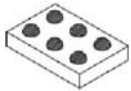
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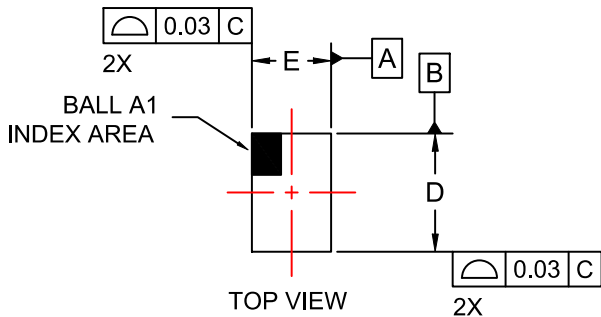
## PACKAGE DIMENSIONS

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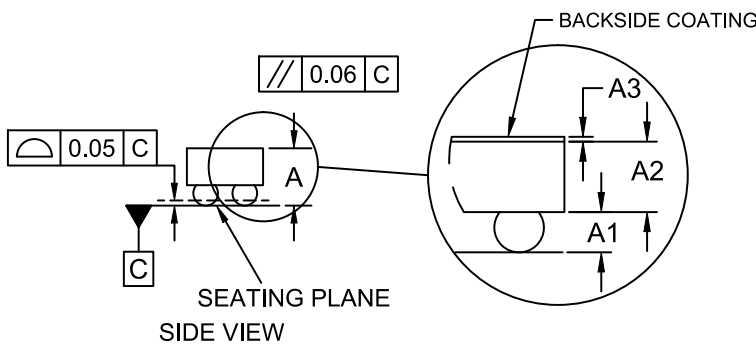
**WLCSP6 1.36x0.76x0.581**  
**CASE 567XQ**  
**ISSUE O**

DATE 03 APR 2019

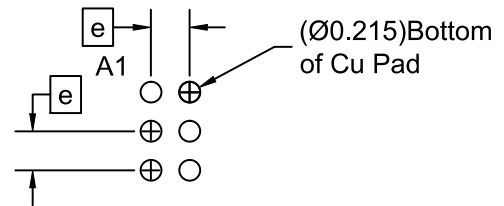
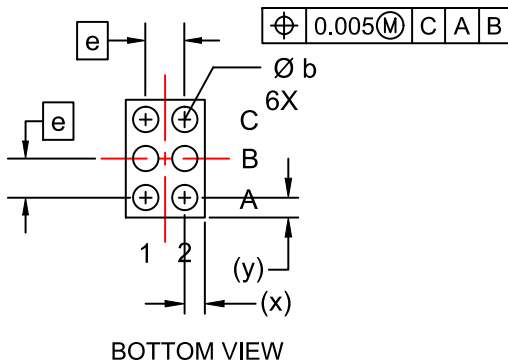


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.540	0.581	0.622
A1	0.183	0.203	0.223
A2	0.335	0.353	0.371
A3	0.022	0.025	0.028
b	0.240	0.260	0.280
D	1.33	1.36	1.39
E	0.73	0.76	0.79
e	0.40 BSC		
x	0.150	0.165	0.180
y	0.250	0.265	0.280



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